Improved PRBS31 testing

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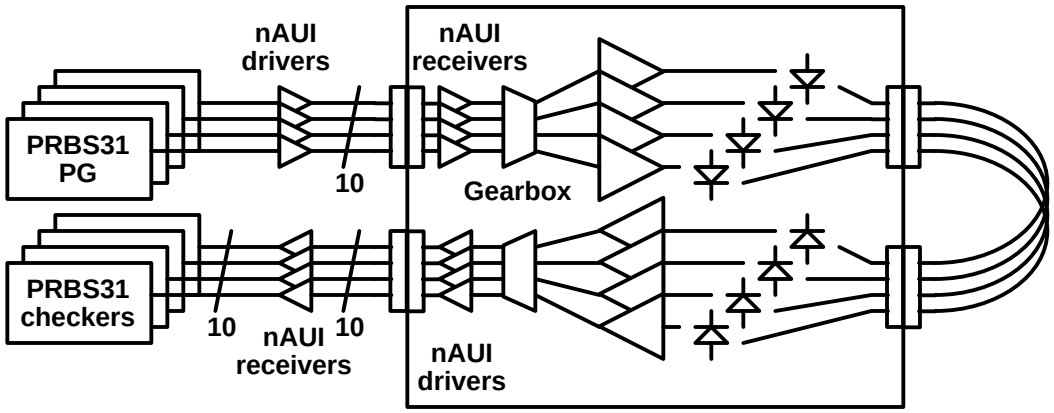
Relates to D2.0 comment 57

Module testing

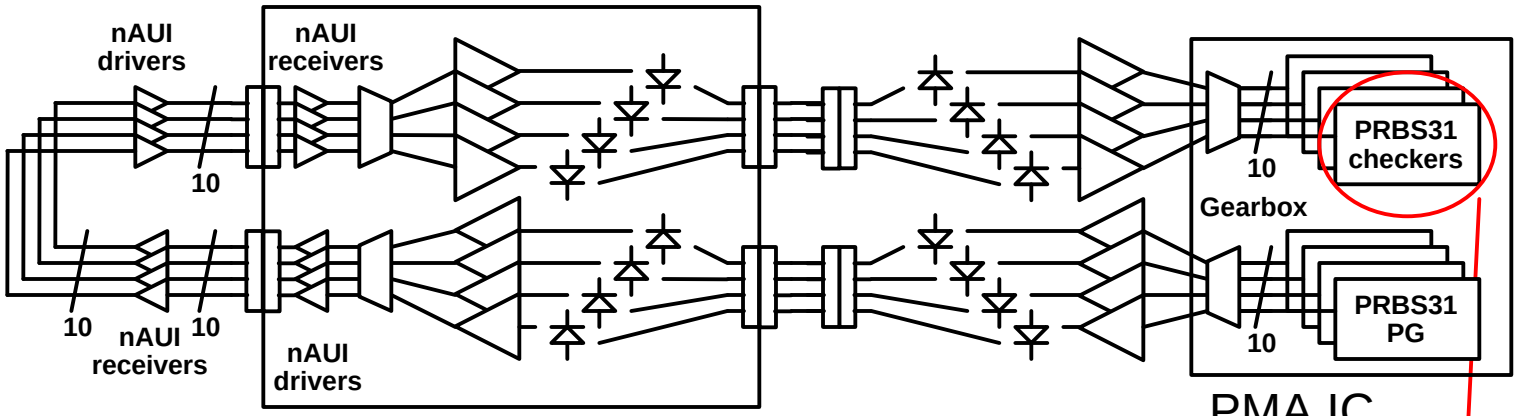


Example 1

100G module tested from electrical side

Example 2

100G module tested from optical side

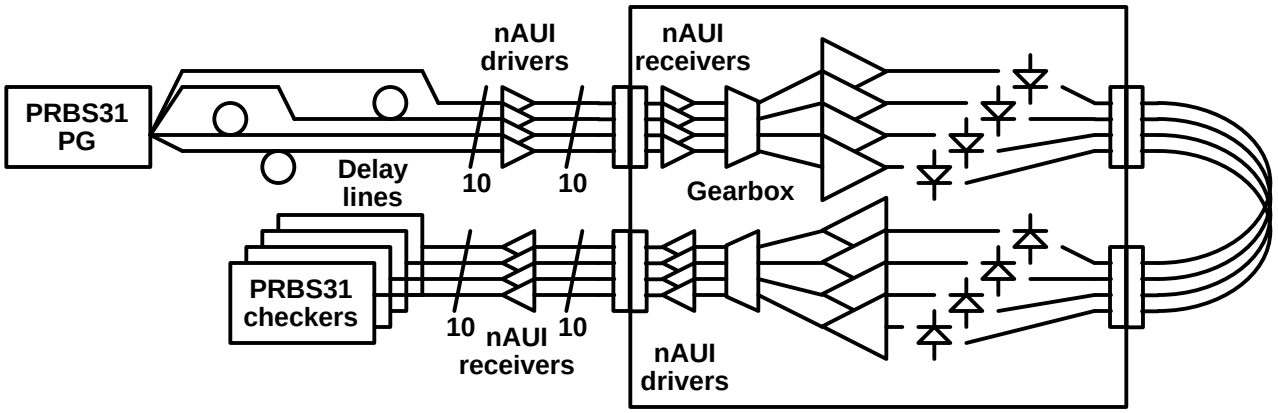


PMA IC used as a tester

See later

- Want to test WHOLE module
  - without assuming that its internal ICs are working perfectly
  - May expect Ethernet switch to check out a new module as in example 1

Module testing cont.

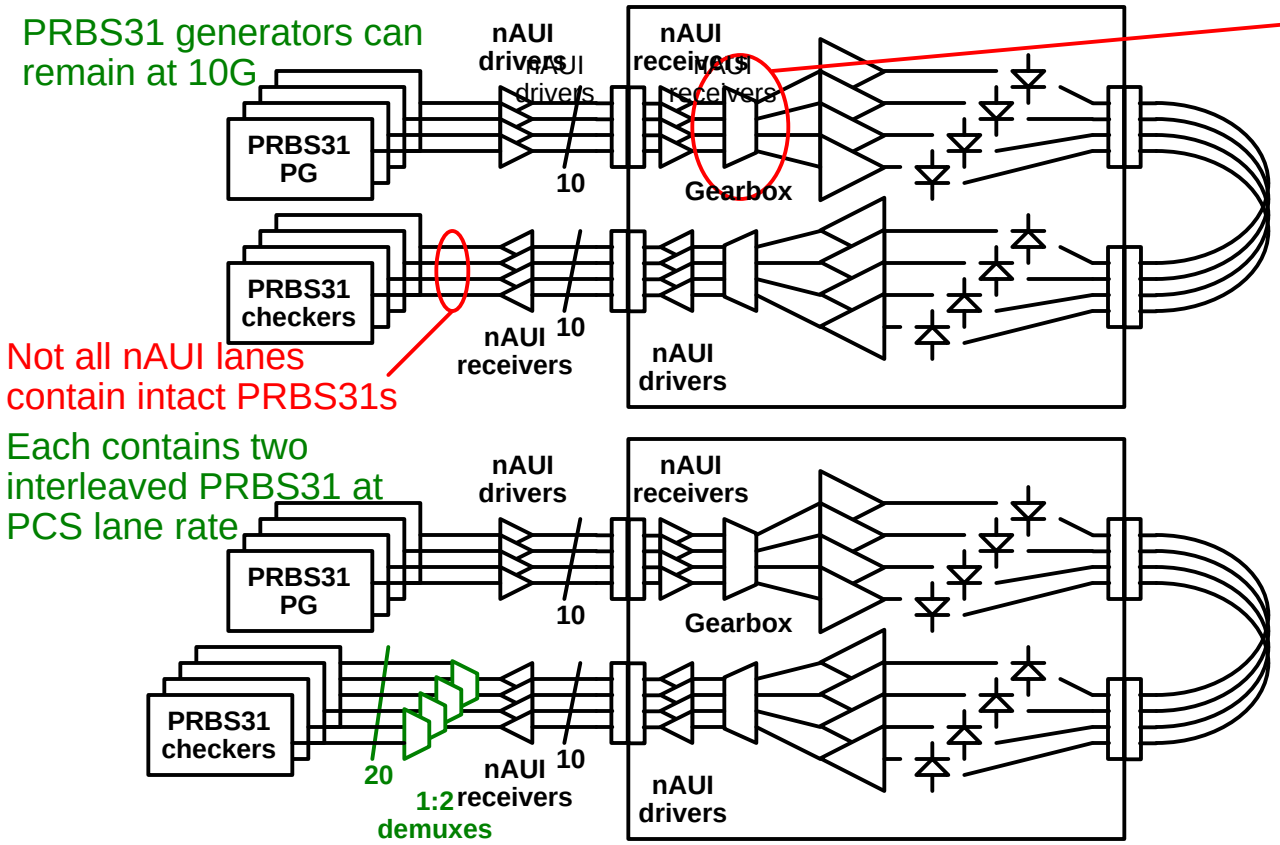


Example 3

Module tested from electrical side, single PRBS generator

- Want to keep test costs down
- Existing 10G test equipment much cheaper than new or 25 G test equipment

Problem and solution



- Hypothetical "serial" error checkers shown
- In practice, signal inside IC would be more parallel than this (<5G per lane) anyway
- Therefore VERY few extra gates needed

Choices

1. Check PRBS31 per nAUI lane, report errors per nAUI lane
   - As D2.0
2. Check PRBS31 per PCS lane, report errors per nAUI lane (add pairs of error counts together)
   - "Backwards compatible" with D1.2
     - Both the patterns it can check and the registers that report the error count are backwards compatible
3. Check PRBS31 per PCS lane, report errors per PCS lane
   - Might allow more thorough error tracing in rare cases?
   - Still can check PRBS31 generated per nAUI lane, 10 more counter registers

- PMA test pattern generation and detection is optional
- If PMA check Rx PRBS31 implemented, propose implementer can use options 1 or 2 as above
- Rx side checkers only or Rx side and Tx side?
  - Don't see much use for Tx side error checking after 4:10 gearbox

A separate issue

- Counting all the errors at very high BER is onerous and pointless
  - Needs very high speed circuitry that's almost never used
- Counting all the errors in bursts is onerous
  - Should say that there's no need to report BER accurately if it is above some amount, and have a sensible maximum increment rate for Clause 30
    - Maybe 10^-3
- This separate issue applies to any PRBS checker, with or without the improvement recommended by this presentation

Proposed change to D2.0 (comment 57)

83.5.10 PMA test patterns (optional)

When check Rx PRBS31 test pattern mode is enabled by bits 1.19.7 and 1.19.0 (see 45.2.1.12b), the PMA expects to find ~~the~~ one or (optionally) two interleaved PRBS31 pattern(s) on each of the lanes received from the PMA server via the *PMAserver*_UNITDATA.indication*x* primitive. Where there are 10 PMA lanes and no errors, there are always two bit-interleaved PRBS31 patterns, one per PCS lane. In many situations, each PMA lane can also be seen as carrying a single PRBS31. The Rx test pattern error counters in registers 1.30 through 1.39 (see 45.2.1.12d) count, per PMA lane, errors in detecting the PRBS31 patterns on the lanes from the PMA server. If the 20 bit-interleaved PRBS31 patterns are checked, the errors are summed for each PMA lane. While in check Rx PRBS31 test pattern mode, the PMA_SIGNAL.indication primitive does not indicate a valid signal. When check Rx PRBS31 test pattern is disabled, the PMA returns to normal operation performing bit multiplexing as described in 83.5.2.

Summary

- D1.2 PRBS31 error checkers in PCS are not as useful as they should be
  - Can't always parse a 10G lane after a 100G gearbox
    - No problem for 40G
  - Solution is to check PRBS31 at the 5G (PCS lane) level rather than 10G (nAUI lane)
    - No need to modify PRBS generators
  - Modify text in 83.5.10. Make the improvement optional
  - Report error count by nAUI lane (still 10 counters, no need to change 45.2.1.12d)
    - If want to report all 20 PCS lane error counts, modify 45.2.1.12d