

Refinement to XLAUI/CAUI Electrical Specifications

IEEE Quebec City

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Summary

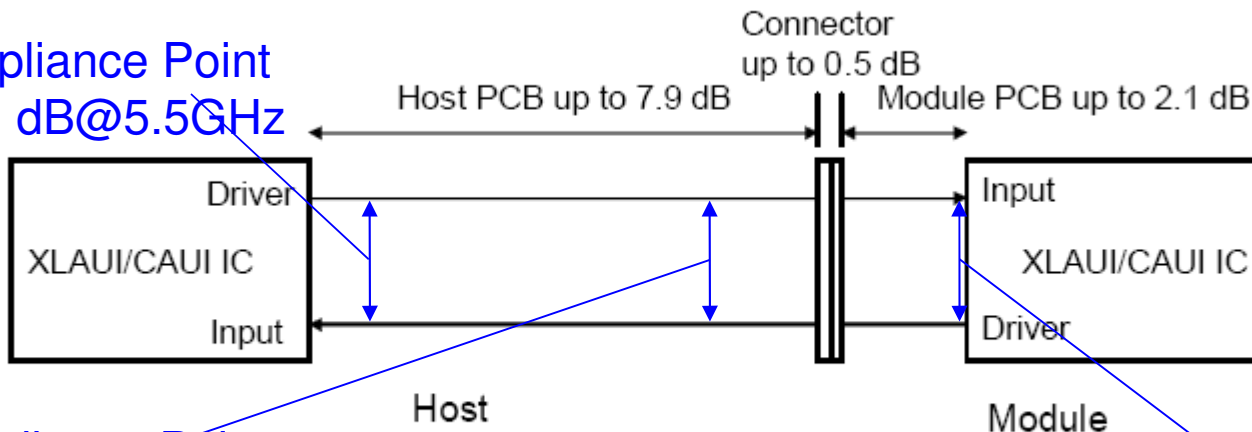
- **Update to nAUI channel SDD21**
- **Defining nAUI compliance point**
- **Updating module and host return loss based cascaded effect of connector and chip**
- **Shifting nAUI compliance from chip ball to 1 dB loss point**
- **Shifting nAUI compliance from the module by the MCB loss**
- **Verifying far end compliance for several corner cases**

Addressing comments: 405, 407, 408, 409, 410, 411, 412, 419, 420

Where should MCB and HCB Measurement Point be?

- Where should HCB reference point be?
 - Naturally it can be at the end of module PCB With 2.1 dB of loss
- Where should MCB reference point be?
 - At end of 7.9 dB channel
 - A short circuit at connector will have RL of 15.8 dB!
 - At minimum loss from the connector but physically implementable
 - Propose 1 dB at 5.5 GHz

Chip Compliance Point
Propose 1 dB@5.5GHz



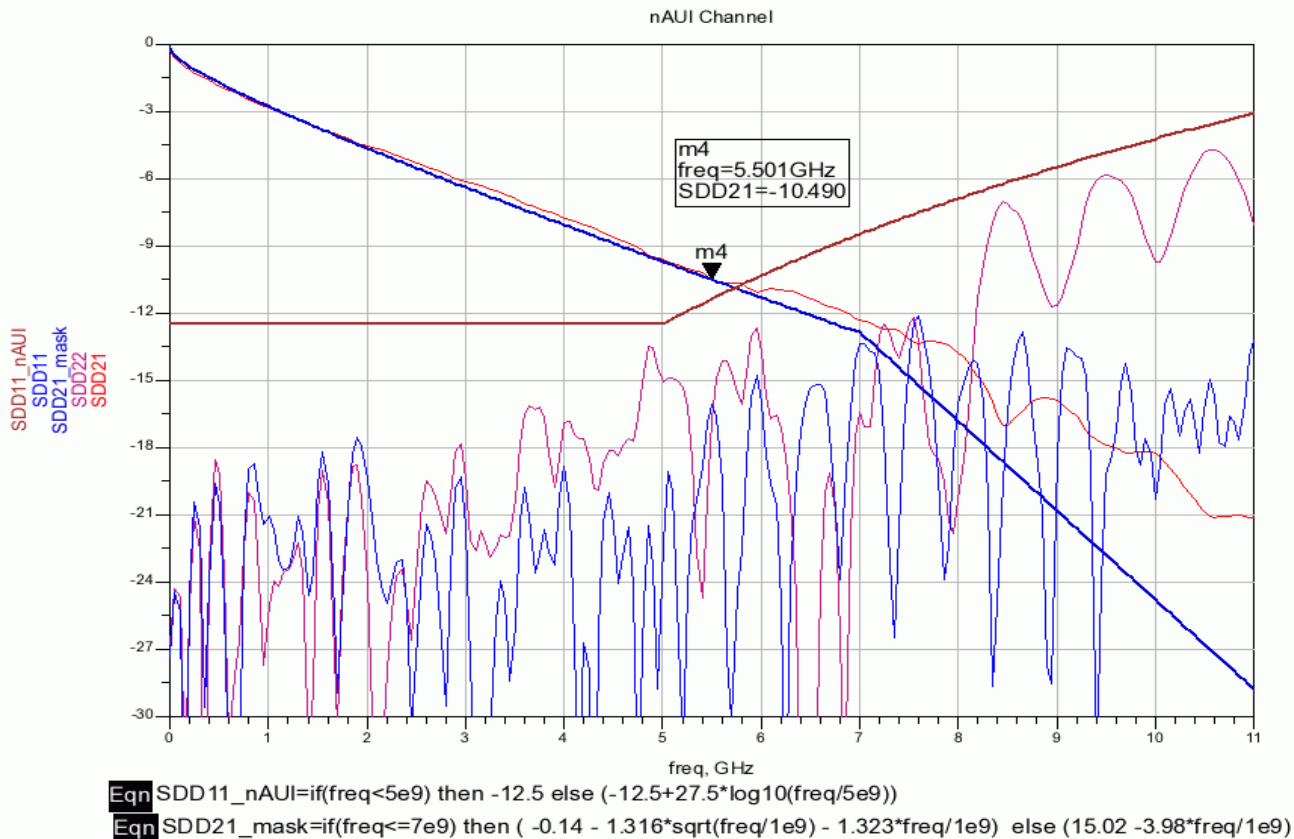
MCB Compliance Point
Propose 1dB@5.5 GHz

Figure 83B-1—Chip-module loss budget

HCB Compliance Point
Propose 2.1 dB@5.5GHz

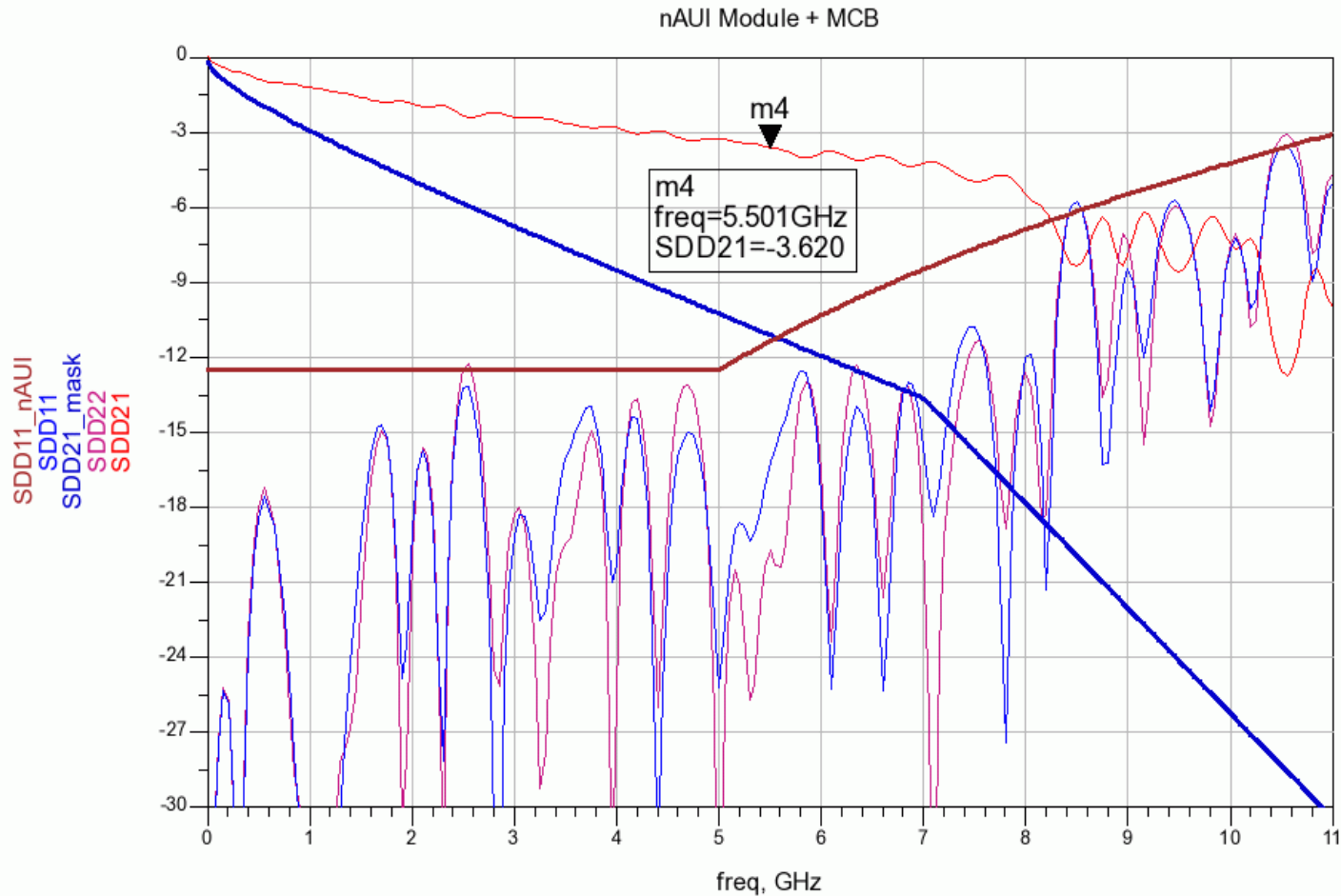
XLAUI/CAUI Channel with 10.5 dB Loss

- This is an improved version over ghiasi_01_0708 which had some undesirable ripple and available from the <http://www.ieee802.org/3/ba/public/channel.html>
 - The 10.5 dB channel was created by cascading 2 dB loss PCB at Nyquist with the 8" Fr4-8 channel.



nAUI Module MCB with 3.6 dB Loss

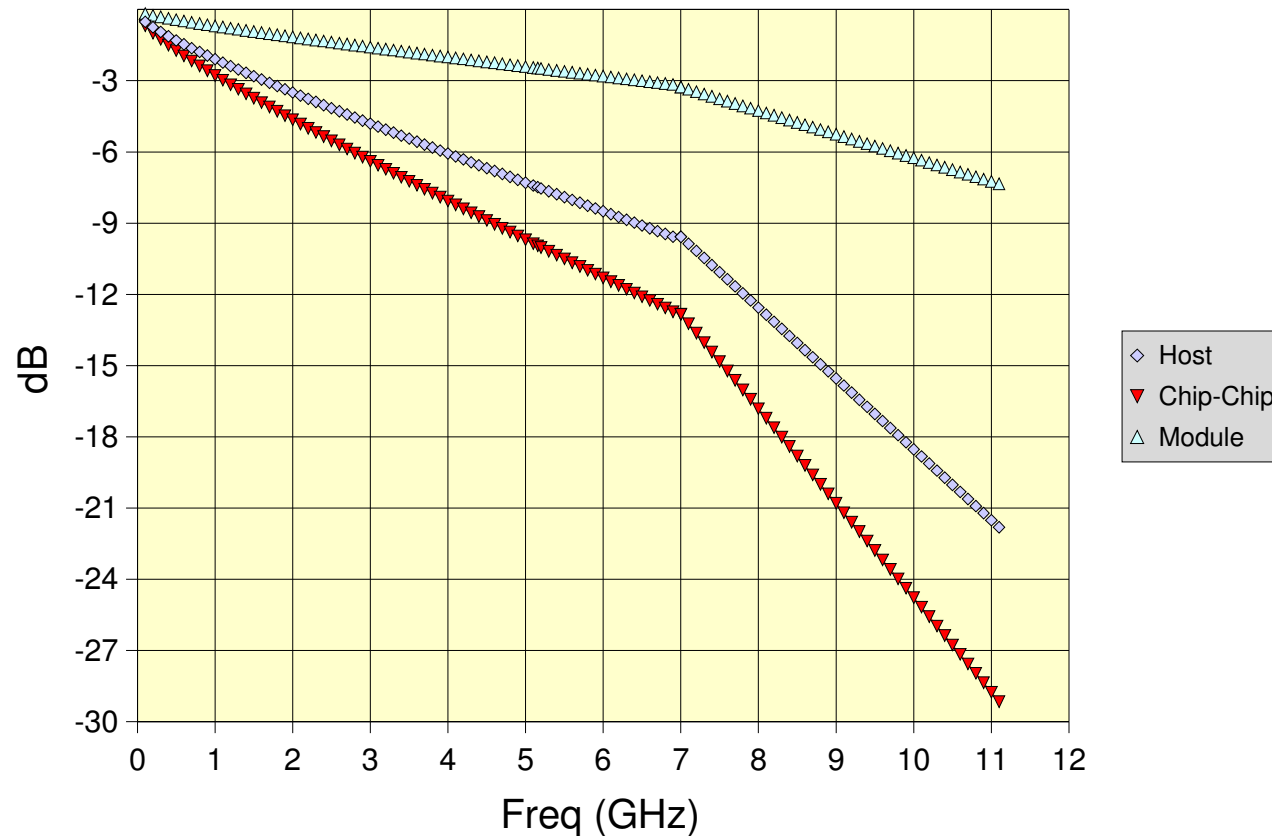
- S-parameters available from <http://www.ieee802.org/3/ba/public/channel.html>



Eqn SDD11_nAUI=if(freq<5e9) then -12.5 else (-12.5+27.5*log10(freq/5e9))

Bringing nAUI Channel Loss in Sync

- Proposed SDD21 masks will make CL83A and CL83B in sync

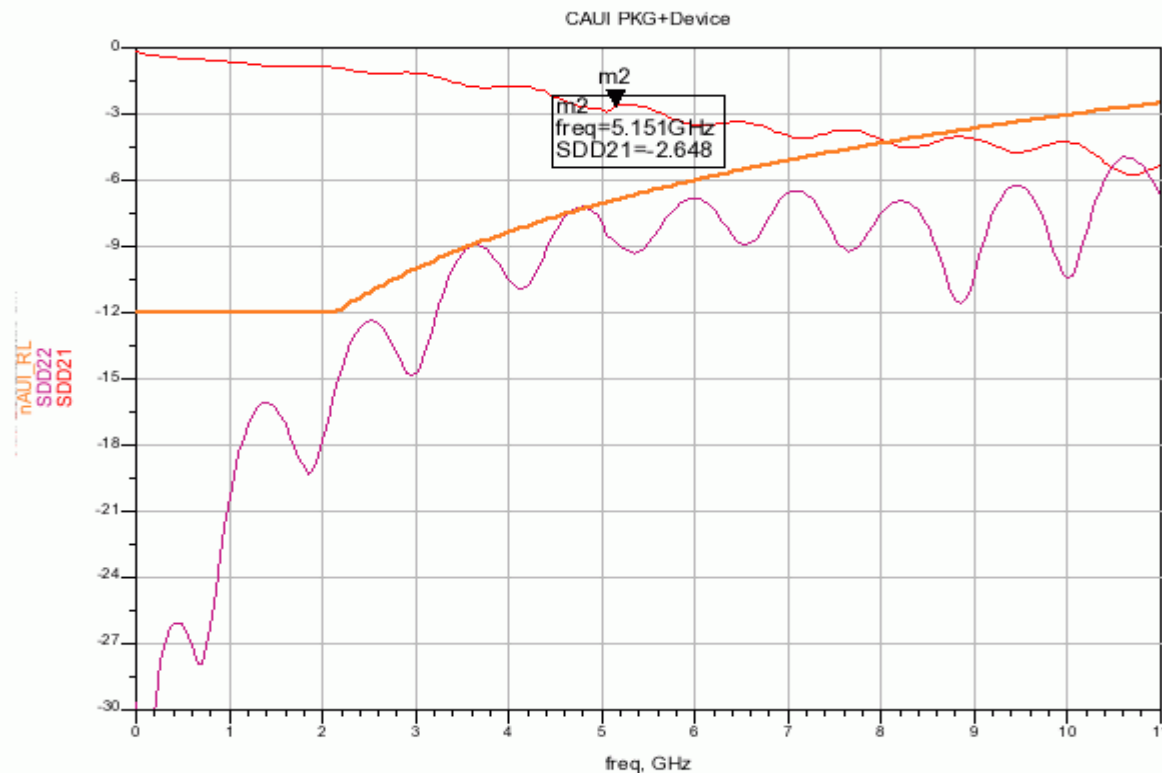


nAUI SDD21 Channel Loss cont.

- **Chip to chip loss SDD21=10.5 dB@5.5 GHz (already in D2.0)**
 - SDD21(dB)= $-0.140 - 1.32*\sqrt{f} - 1.32*f$ from 0.25 to 7 GHz
 - SDD21(dB) = $15.02 - 3.98 * f$ from 7 to 11.1 Ghz
- **Chip to module channel SDD21=7.9 dB@5.5 GHz (detail missing)**
 - SDD21(dB) = $-0.11 - 0.99*\sqrt{f} - 1.00*f$ from 0.25 to 7 GHz
 - SDD21(dB) = $11.32 - 2.99 * f$ from 7 to 11.1 Ghz
- **Module PCB channel SDD21=2.1 dB@5.5 GHz (detail missing)**
 - SDD21(dB) = $-0.04 - 0.33*\sqrt{f} - 0.32*f$ from 0.25 to 7 GHz
 - SDD21(dB) = $3.72 - f$ from 7 to 11.1 Ghz

Creating nAUI Compliance Output

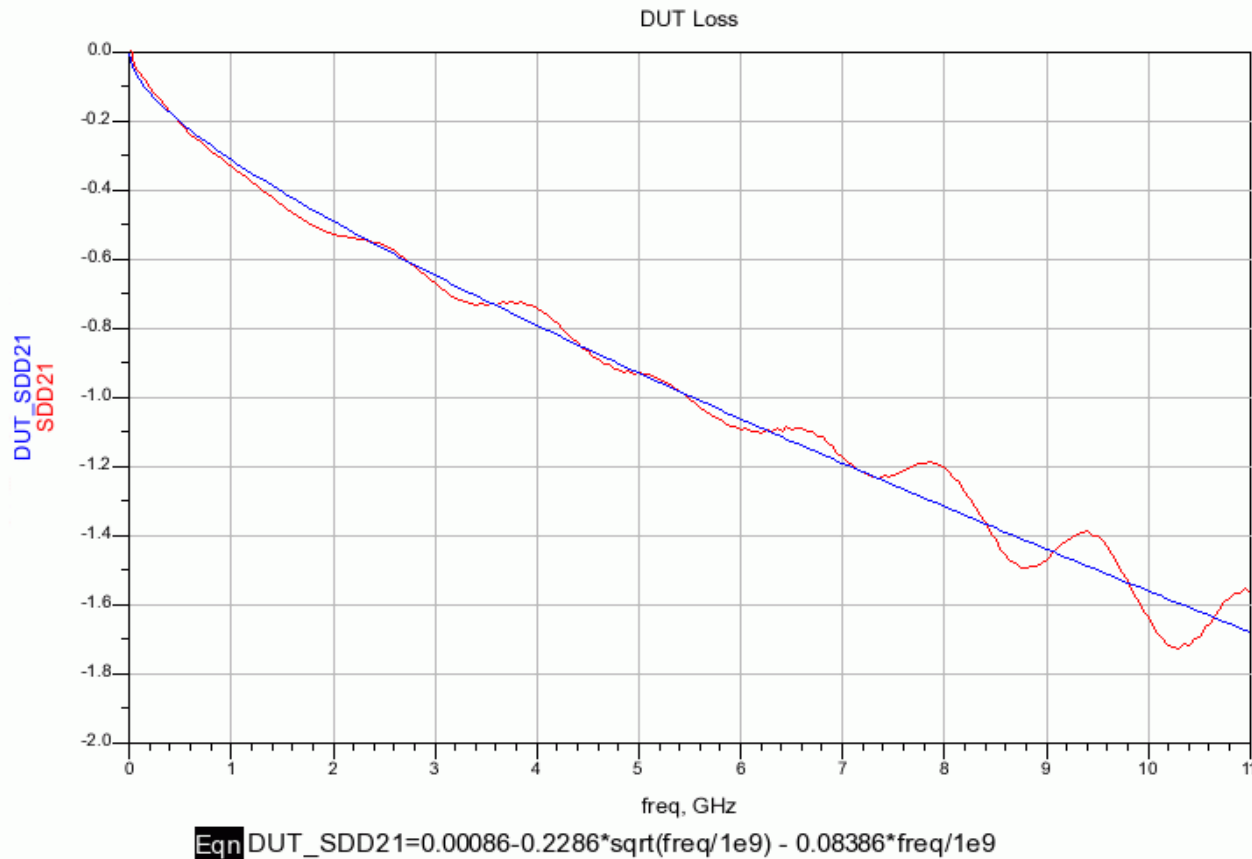
- SerDes with worst case return loss + channel with 1 dB loss at Nyquist
 - No need to make any changes to the host chip RL



$$\text{Eqn } \text{nAUI_RL} = \text{if}(\text{freq} < 2.125\text{e}9) \text{ then } (-12) \text{ else } (-6.5 + 13.33 * \log_{10}(\text{freq}/5.5\text{e}9))$$

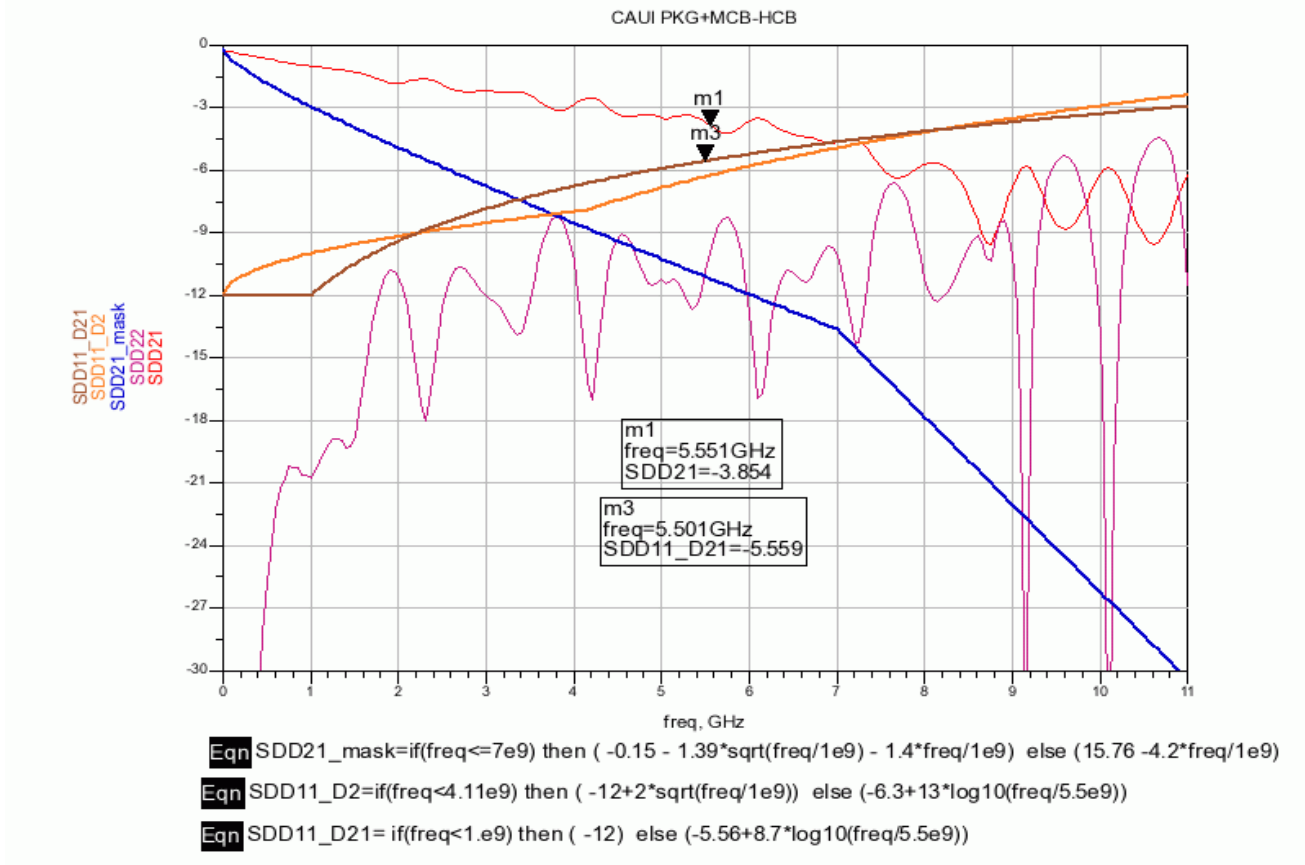
Loss from Chip Ball to Chip Compliance Point

- Current value in the draft are 0.7 dB, this was scaled to 1 dB at 5.5 GHz for easier PCB routing and channel availability



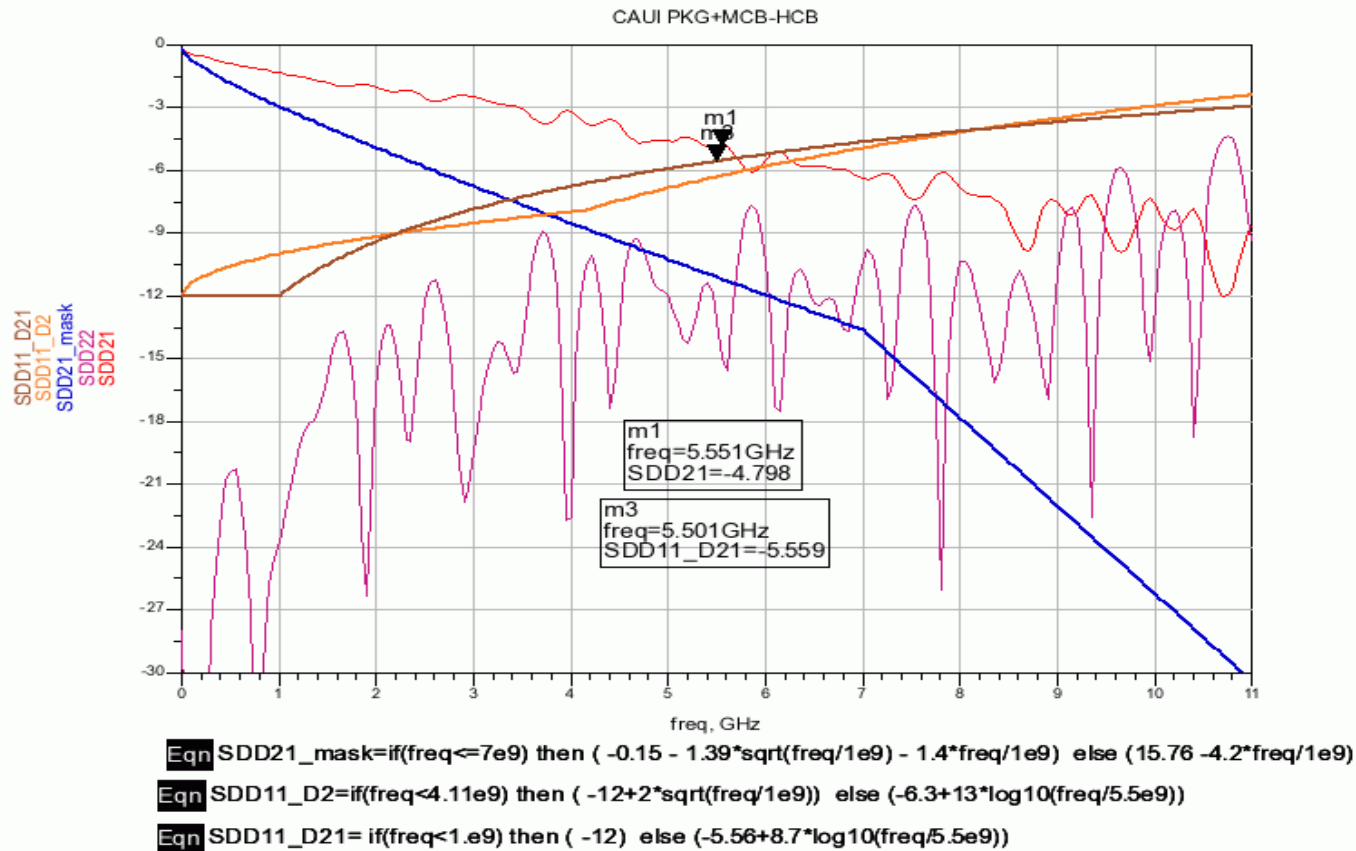
Module Return Loss

- Current host & module limits from SFP+ limits are based on SerDes RL 2 dB better!
 - Current mask limit (SDD11_D2) almost touches the mask, propose limit is SDD11_D21
 - Assumes 0.5 dB PCB loss @5.5 Ghz and 1 dB for the MCB



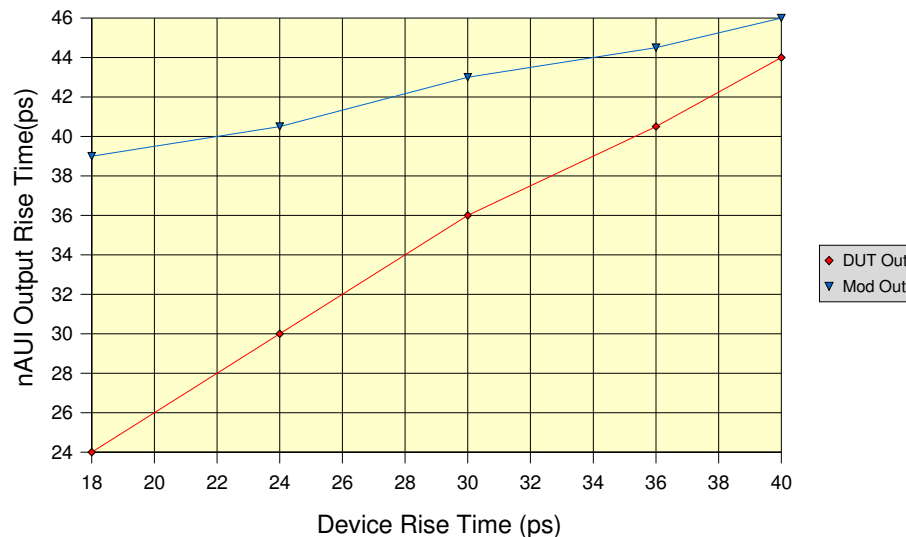
Host Return Loss

- Current host & module limits from SFP+ limits are based on SerDes RL 2 dB better!
 - Current mask limit (SDD11_D2) not optimum for host mask, propose limit is SDD11_D21
 - Assumes min PCB loss of 0.5 dB@5.5 Ghz and 2 dB loss @5.5 Ghz for the HCB



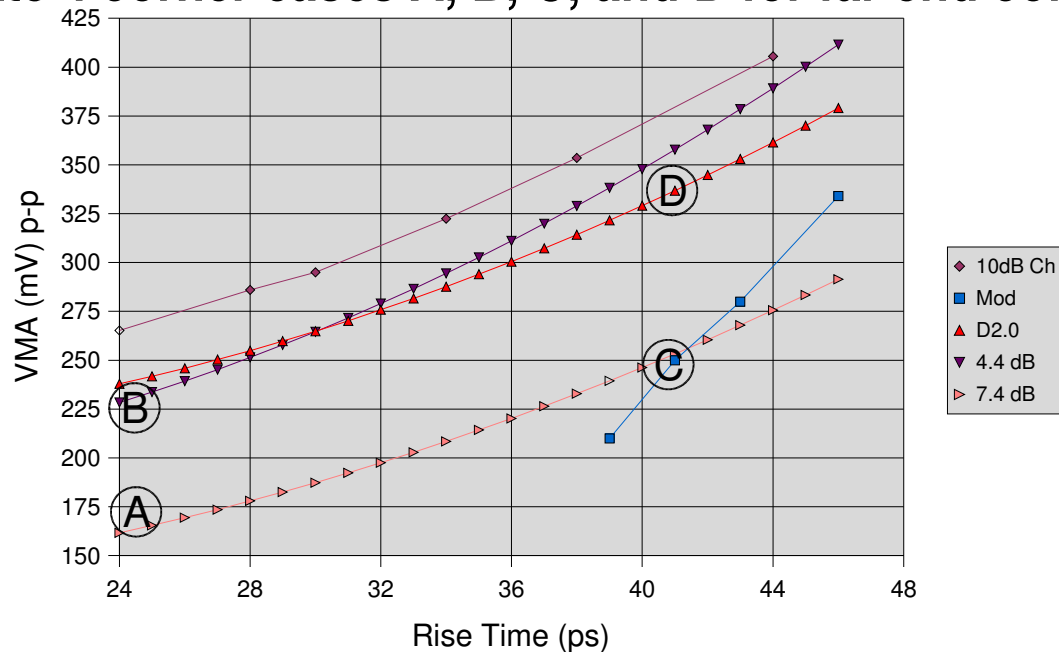
nAUI Compliance Output

- Chip measured with 1 dB DUT board
- Module measured with 1 dB MCB board and assumed module PCB has 2.1 dB loss
- Impact of rise/fall time at nAUI compliance point illustrated below
 - Since the compliance measurement already has some PCB loss the minimum de-emphasis amount will be lower.



Translating Device Setting to nAUI Device DUT Output

- Vtx-demph was adjusted to give same far end eye opening for 10 dB channel then the output measured with 1 dB DUT board
 - $V_{tx-demph} = (234.64 - 2.13 \cdot x + 0.18 \cdot x^2) \cdot 1.32 \cdot (10^{y/20})$
 - The de-emphasis range y is from 4.4 dB to 7.4 dB calibrated at DUT output
 - The device de-emphasis was 7.5 dB
- Next investigate 4 corner cases A, B, C, and D for far end compliance

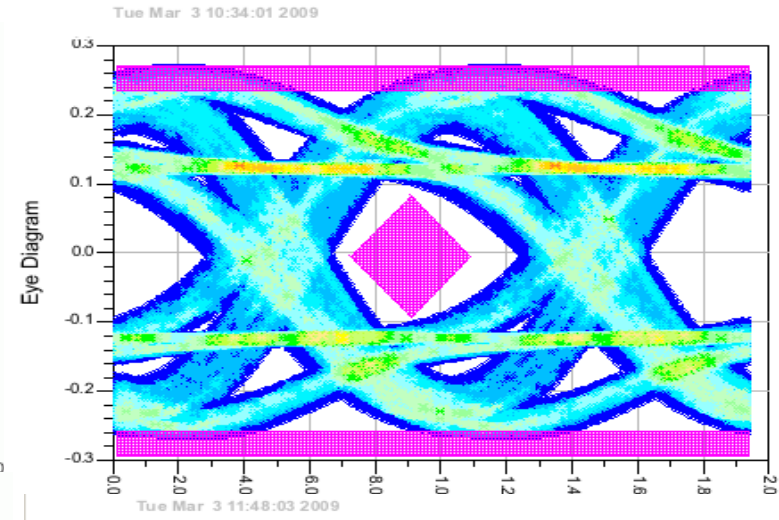
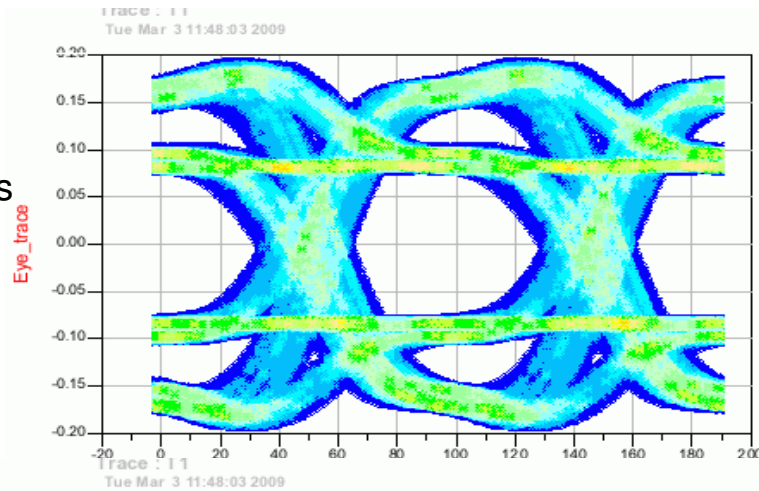


Near End and Far End Eyes

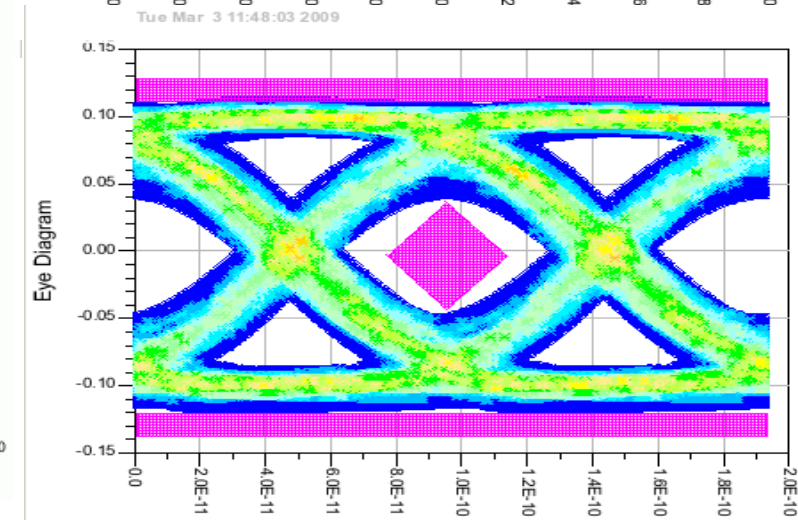
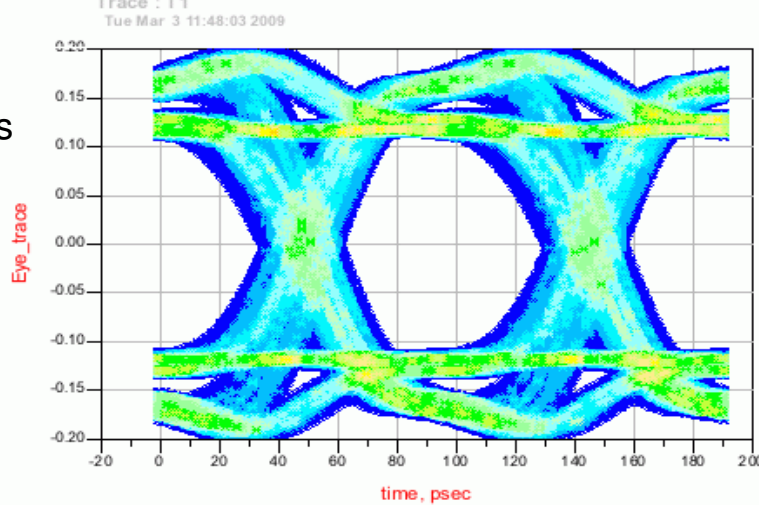
nAUI Near

nAUI Far

Case A
5.2 dB
Tr=24 ps

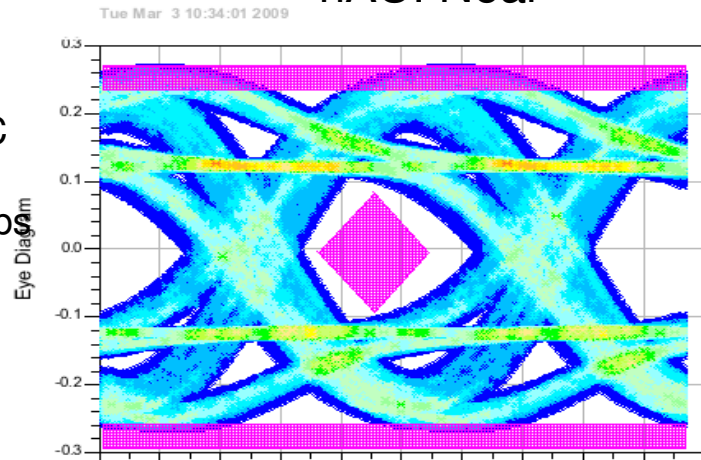


Case B
3.3 dB
Tr=24 ps

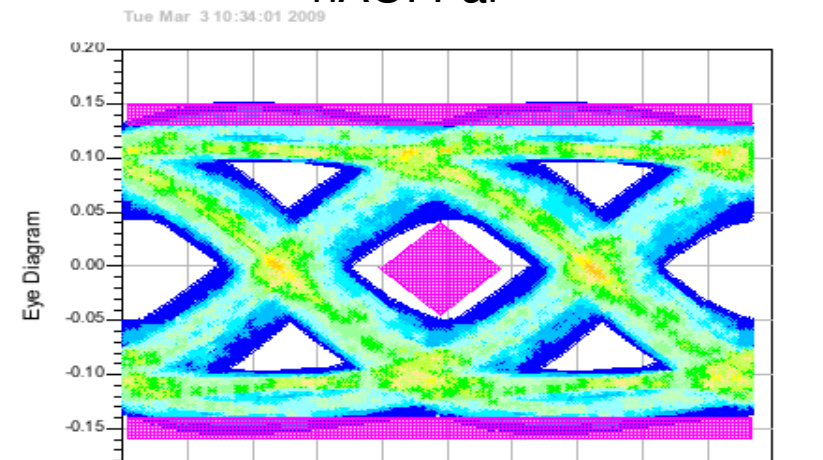


Near End and Far End Eyes

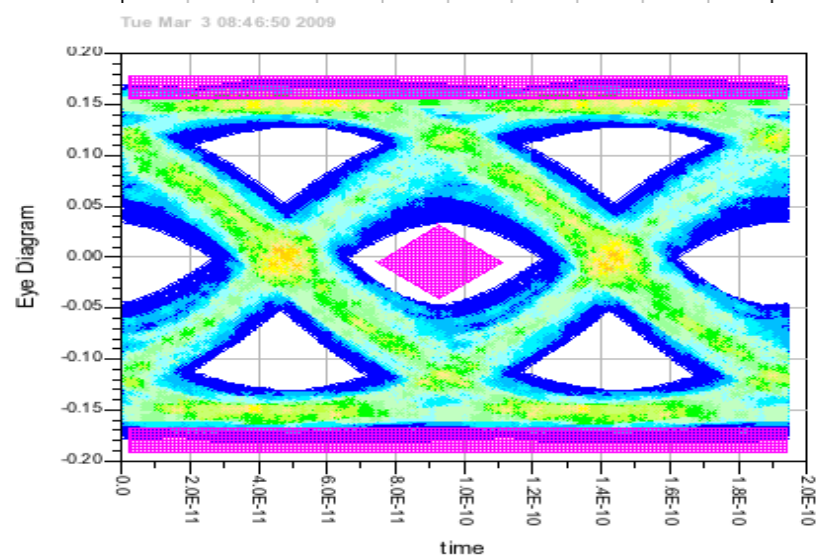
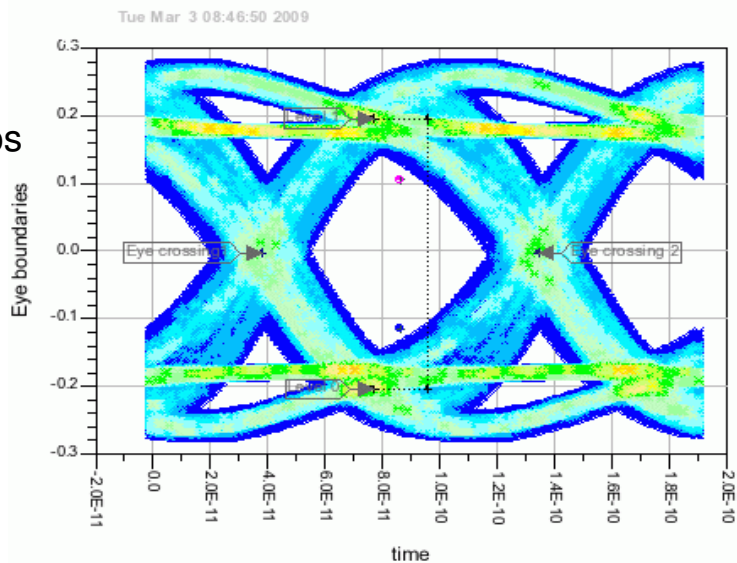
nAUI Near



nAUI Far

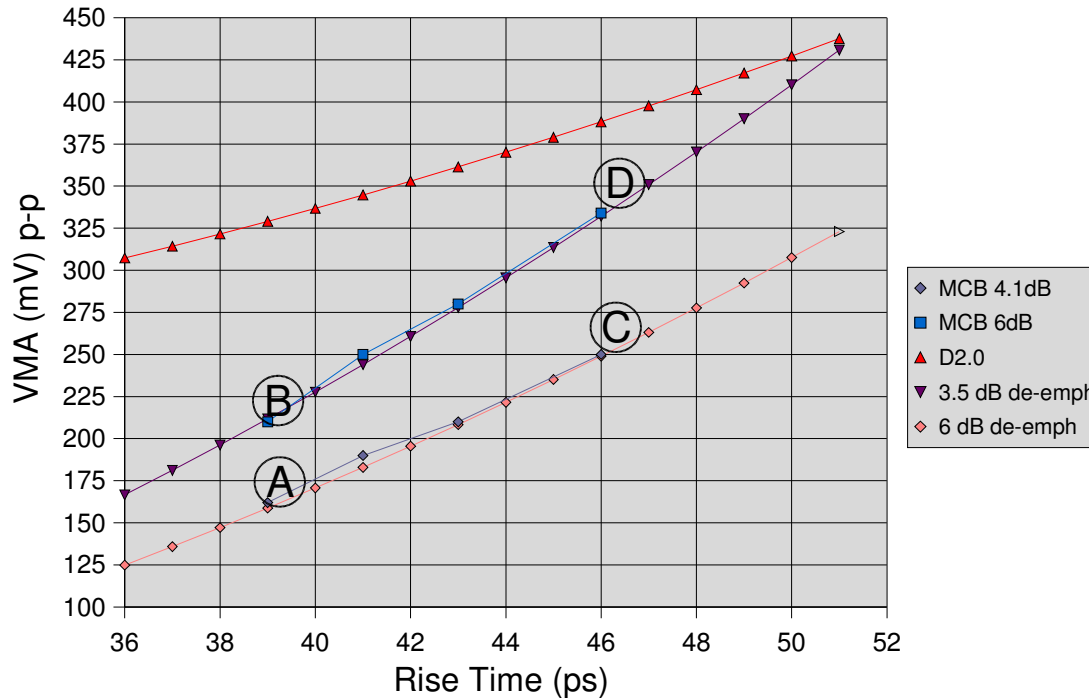


Case D
3.3 dB
Tr=44 ps

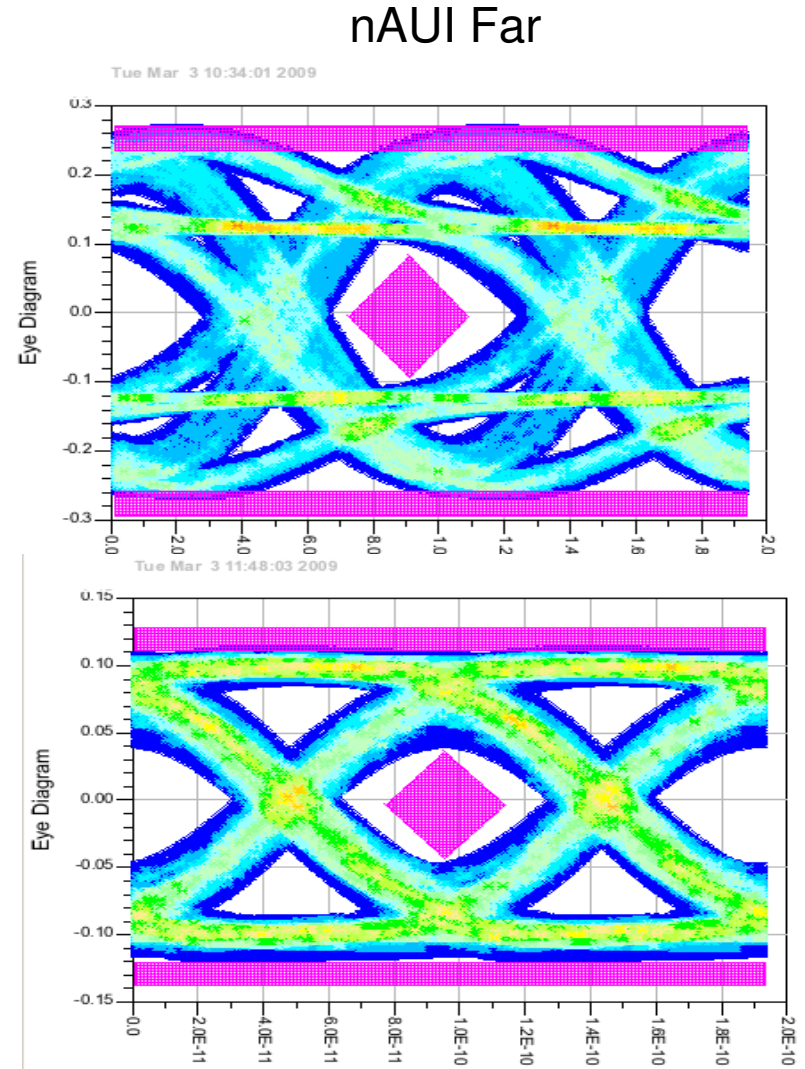
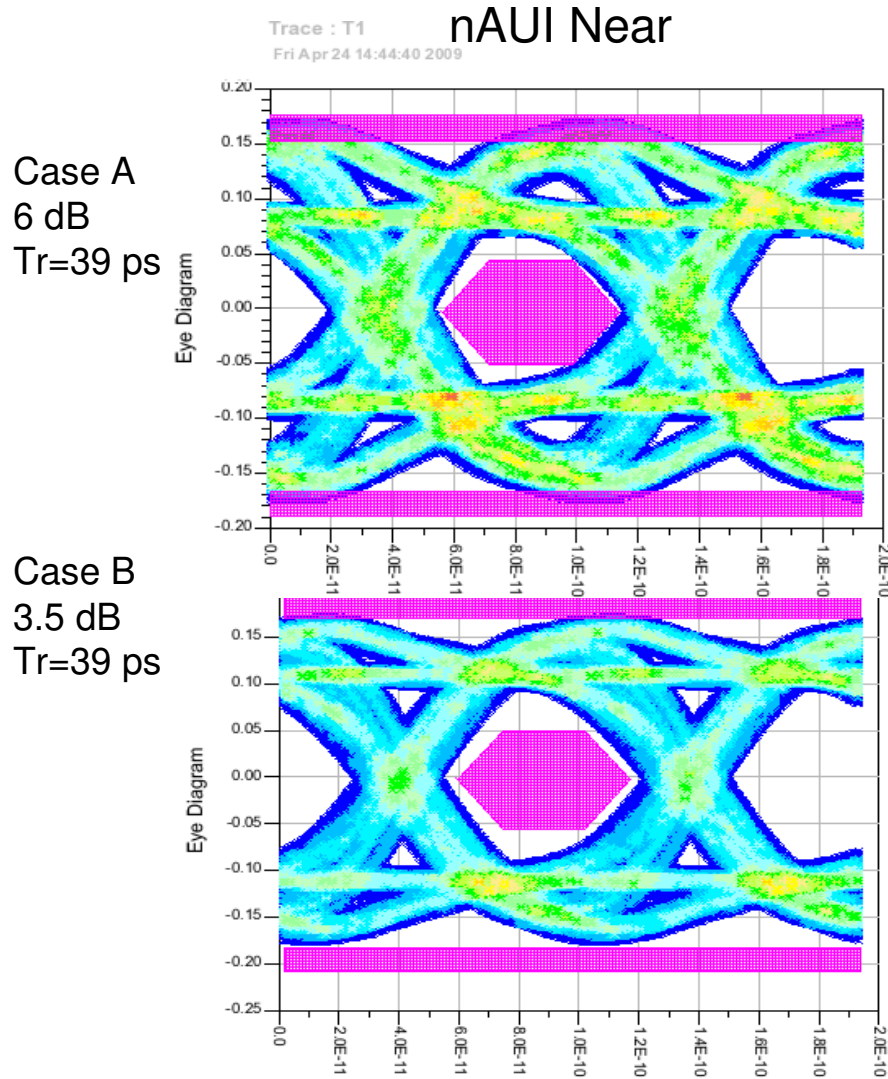


Translating Device Setting to nAUI Module MCB Output

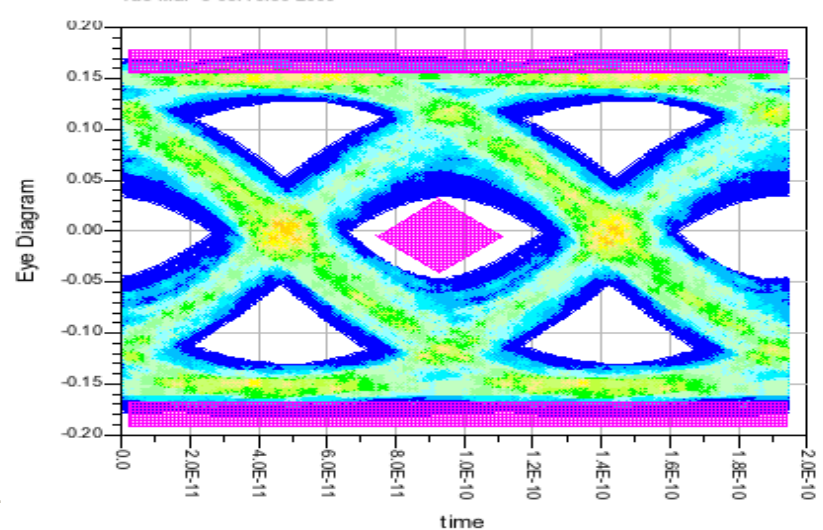
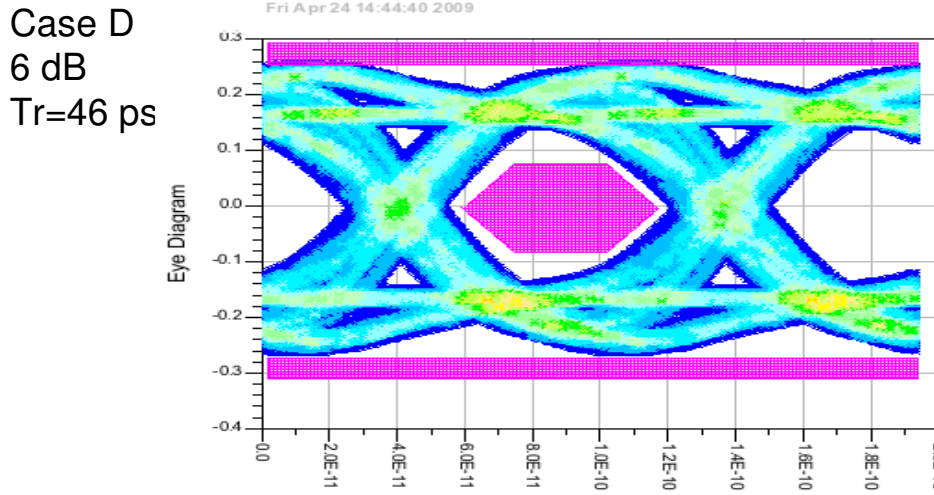
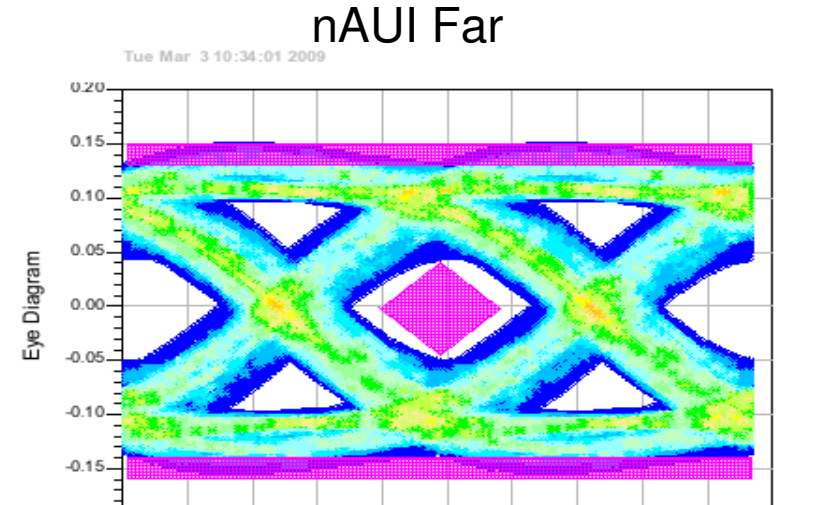
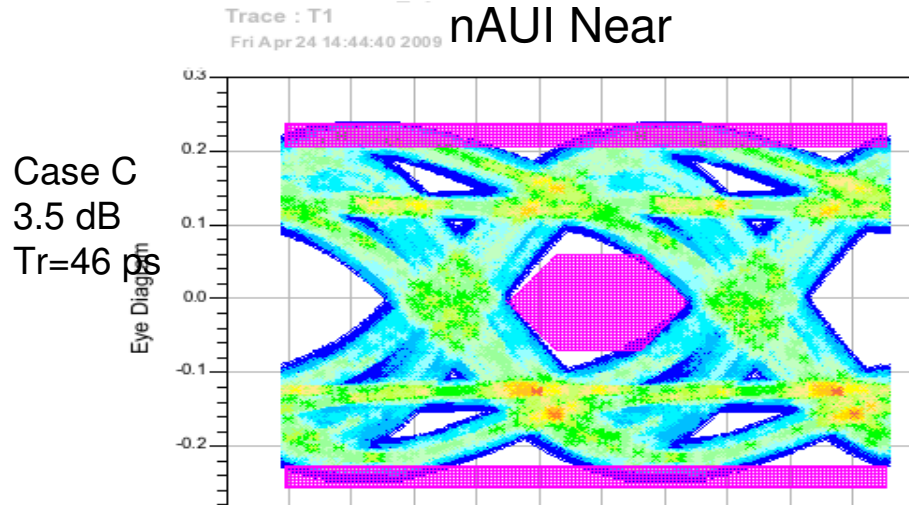
- Vtx-demph was adjusted to give same far end eye opening for 10 dB channel then the output measured with MCB
 - $V_{tx-demph} = (-110 - 2.13 \cdot x + 0.32 \cdot x^2) \cdot (10^{y/20})$
 - The de-emphasis range y varies from 3.5 dB to 6 dB calibrated at MCB output
 - The device de-emphasis was 7.5 dB
- Next investigate 4 corner cases A, B, C, and D for far end compliance



Near End and Far End Eyes



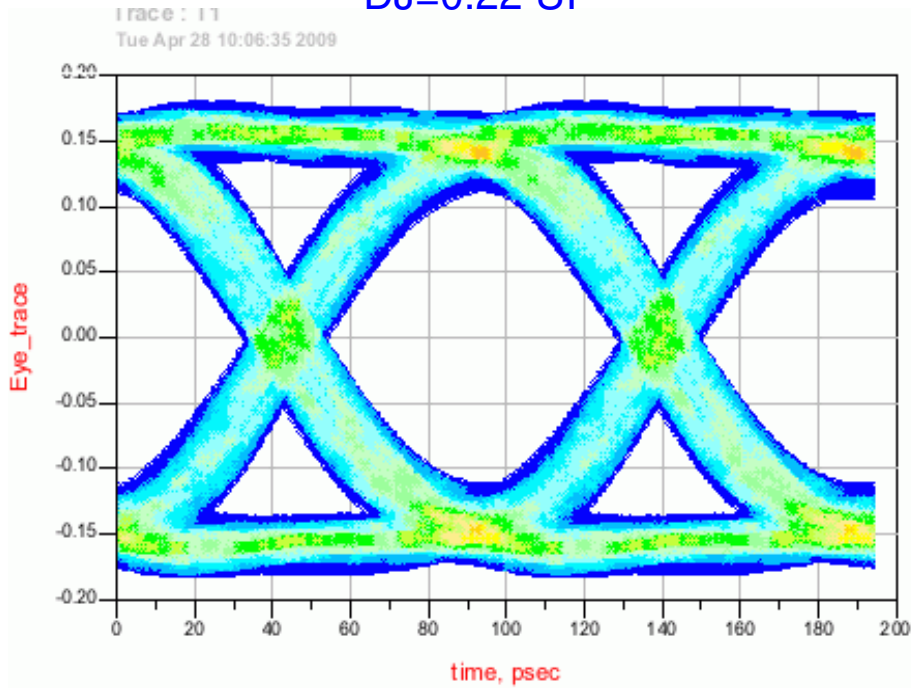
Near End and Far End Eyes



Verifying Module MCB Jitter Output

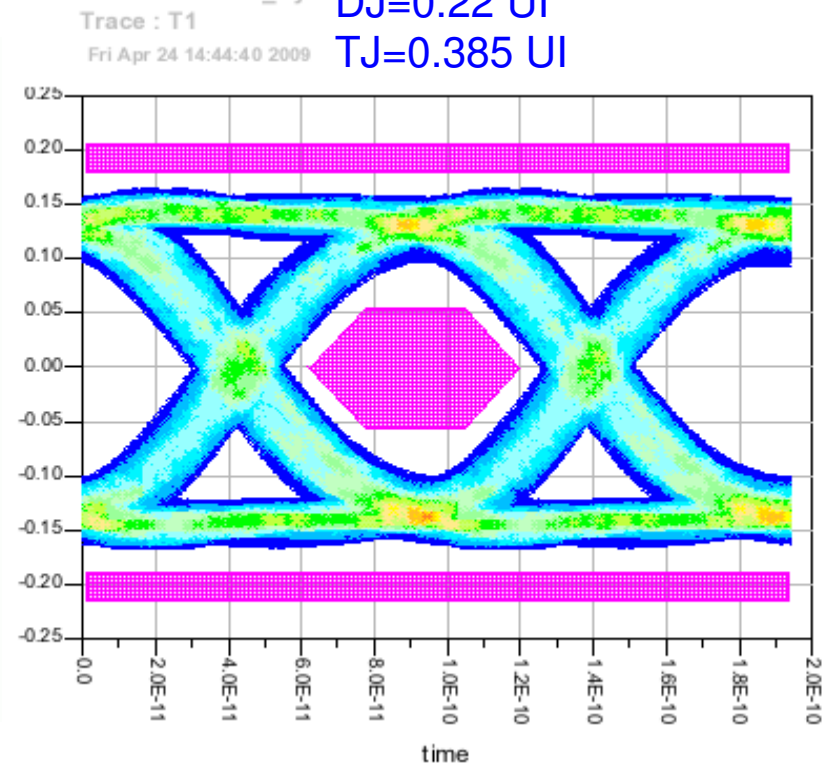
- The current DJ and TJ values are in line with worst case MCB output

DJ=0.22 UI



DJ=0.22 UI

TJ=0.385 UI



Summary

- **Proposed to define nAUI compliance at 1 dB loss at Nyquist to allow practical PCB test board and breakout**
- **The de-emphasis, rise time, and Vtx-demph are shifted to the nAUI TX/RX compliance point.**
 - **Chip-Chip compliance point was move to 1 dB@5.5 Ghz**
 - **Module compliance point was moved to 3.6 dB@5.5 Ghz**
 - **The de-emphasis and rise/fall time were then adjusted based on the chip or module observable compliance point**
- **Module return loss adjusted assuming min channel and MCB loss**
- **Host return loss was adjusted based on HCB loss and with channel**
- **Proposed de-emphasis, Tr/Tf, and Vtx-demph guarantee far end compliance for CL83A and CL83B.**