Common Pluggable Interface

For 100GBASE-CR10 & 100GBASE-SR10

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Outline

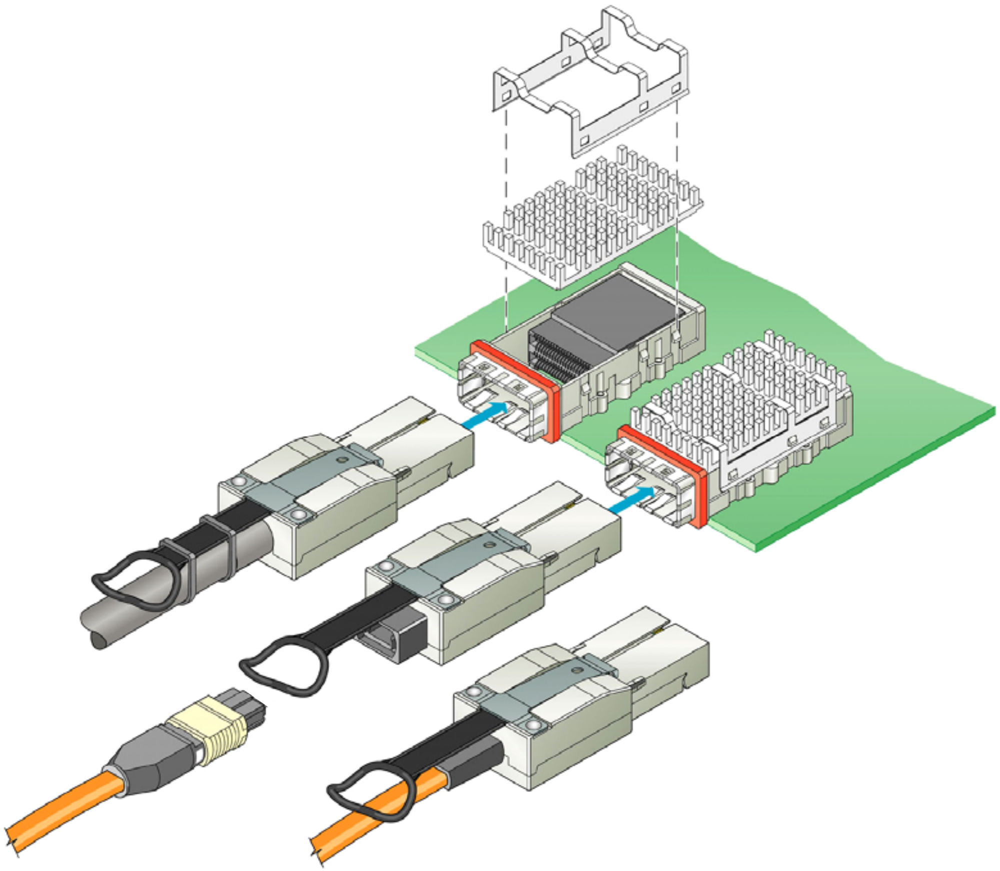
- Objectives
- Opportunity - Reuse twelve-lane form factor
- Issue – Lane selection in twelve-lane form factor for ten-lane applications
- Recommendation

- Addresses D2.0 comment 609

Objectives

- Enable a common pluggable interface for interconnect variants (copper cable assemblies, active cable assemblies and fiber optic transceivers) using a twelve-lane form factor,
- Minimize complexity for ASIC, host board, module and assembly design
- Minimize time-to-market and development cost
- Maximize cable plant performance/reliability

Introduction

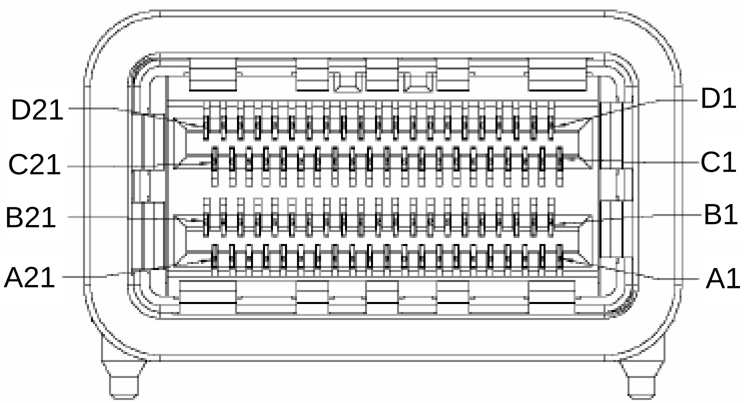


A form factor in development within the InfiniBAnd Trade Association (IBTA) ElectoMechanical Working Group (EWG) supports up to 12 lanes of media including copper, optics and active cable assemblies at 10 GBd signal rates. The electrical interface is based on a two-high, stacked, edge-connector similar to that for PCI Express x16. It offers high port density (27 mm pitch) but has limited power dissipation (< 6 W).

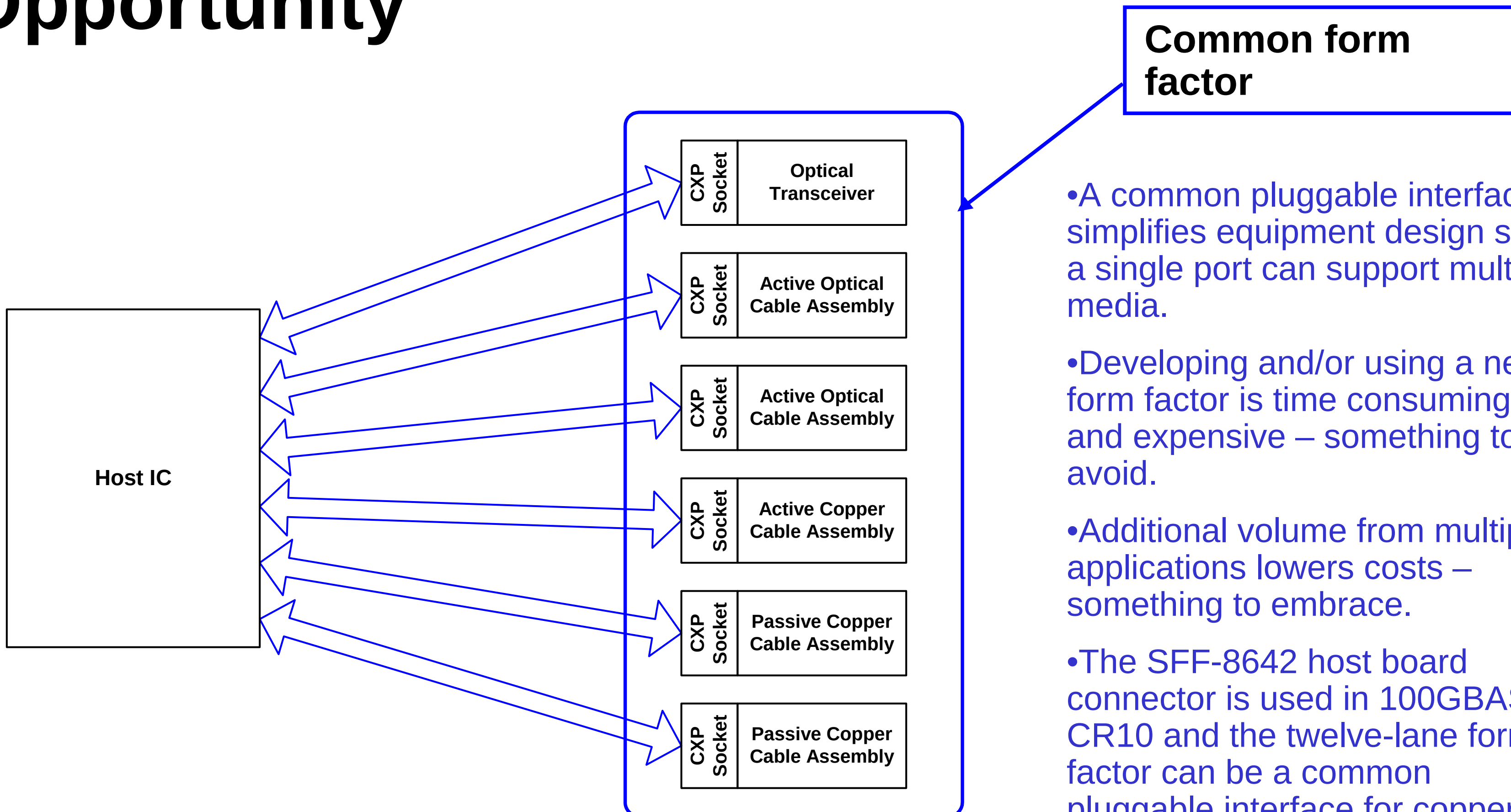
Although not explicitly mentioned, the SFF-8642 connector, the required 100GBASE-CR10 connector, was initially defined for this twelve-lane form factor.

Above, copied with permission, is Figure 1, from ‘120 Gb/s 12x Small Form-factor Pluggable (CXP) Interface Specification for Cables, Active Cables & Transceivers, Version 0.7, March 4’, 2009. The figure on the right is from ‘P802.3ba-D2.0’, Figure 85-15 with contacts labels modified to match SFF-8642.

Host Board Receptacle



Opportunity



- A common pluggable interface simplifies equipment design since a single port can support multiple media.
- Developing and/or using a new form factor is time consuming and expensive – something to avoid.
- Additional volume from multiple applications lowers costs – something to embrace.
- The SFF-8642 host board connector is used in 100GBASE-CR10 and the twelve-lane form factor can be a common pluggable interface for copper and active cable assemblies and transceivers.

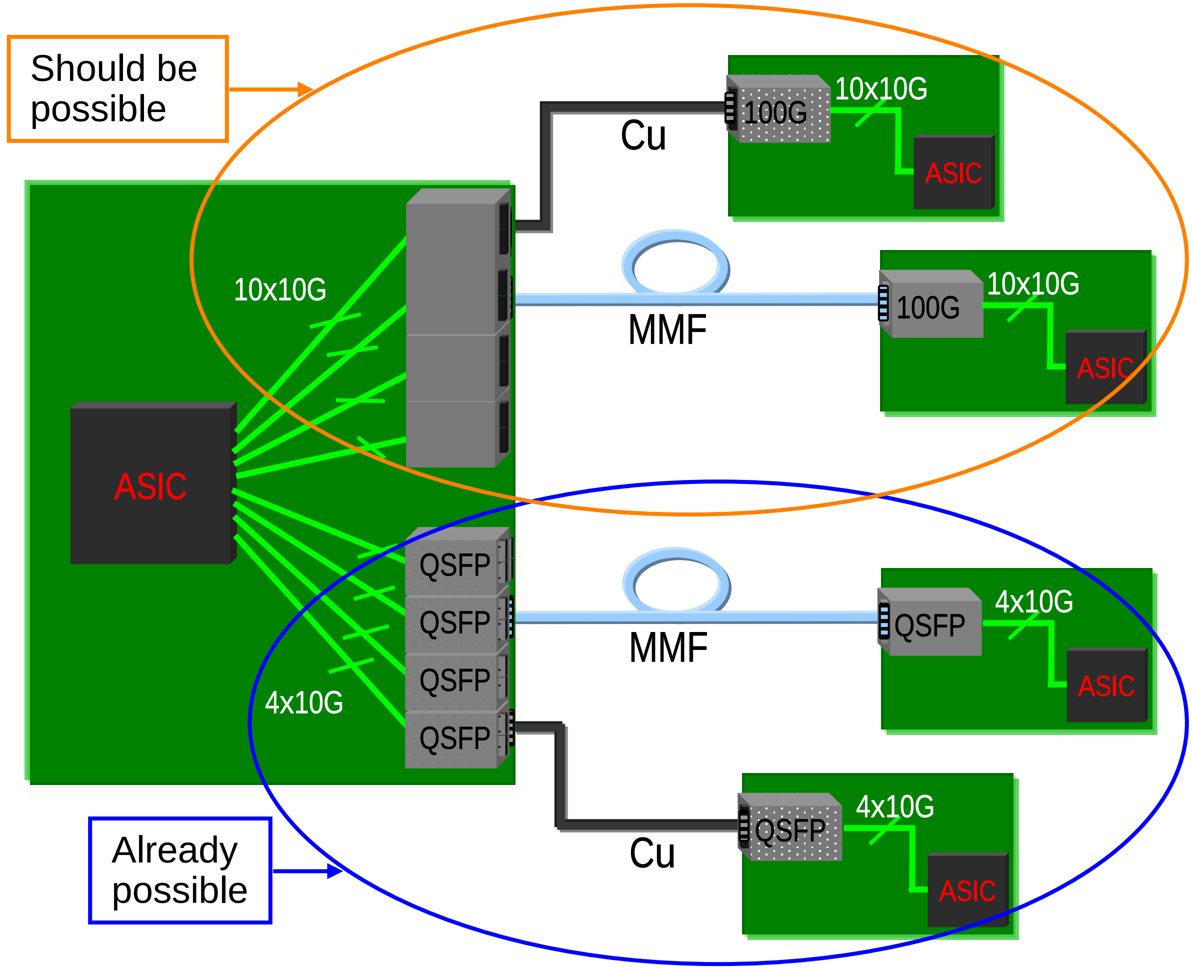
An opportunity exists to reuse a form factor under development for another application. Taking advantage of this opportunity reduces the time to market and eliminates the development costs associated with creating and learning to use a new form factor. The combined volume for both applications also promises economy-of-scale benefits. The popularity of SFP+ and QSFP offer good examples of form factors that support multiple media and applications.

Issue

Since 100GBASE-CR10 and 100GBASE-SR10 only use ten of the twelve lanes available lanes in an emergent form factor, a key item is to identify which ten to use. Choosing a common set of lanes for copper and optical variants will enable its reuse for 100GBASE-CR10 and 100GBASE-SR10 applications with minimum additional effort for ASIC and host board designers. Failure to use a common set would be problematic and frustrating for host ASIC and board designers.

If a common set of ten is not used, the host board designer has onerous choices:
 - dedicate some specific ports to copper variants and others to optical variants
 - route eleven lanes to all ports and require that the ASIC adapt to the variant that is eventually inserted.

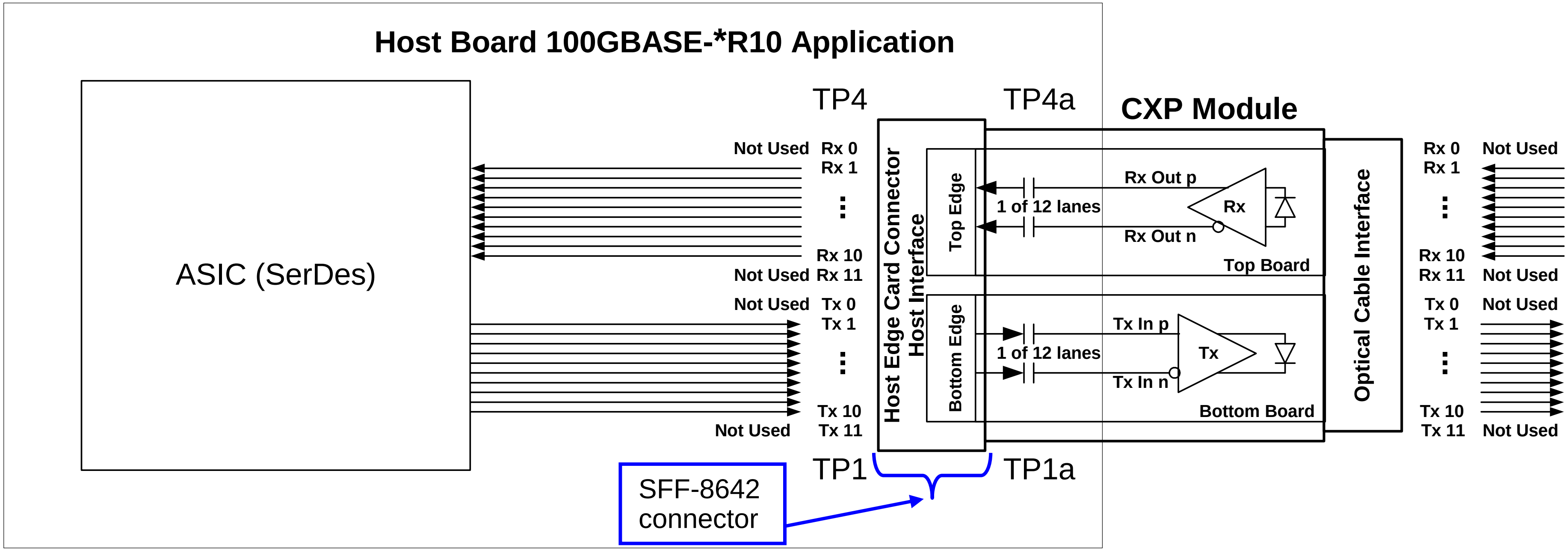
If a common set is used, equipment can be more readily designed to have field-configurable ports providing media flexibility to end users.



•Using the same 10 of the 12 possible lanes for 10GBASE-SR10 and 10GBASE-CR10 provides a significantly more attractive common pluggable interface.

•A common pluggable interface simplifying equipment design and field-configurable ports providing end-user media flexibility will enlarge the market and accelerate market adoption.

Recommendation for 10-Lane CXP Applications (1)



•For ribbon fiber using the middle lanes may reduce variability in insertion loss.

•For copper cable assemblies using the middle lanes centers the conductor bundle, balancing strain relief across the differential pairs.

•Consequently, these outer lanes, lanes 0 and 11 in a twelve lane assembly, are the most logical to have inactive in 10-lane applications.

•For optical modules, de-activating the same lanes in the electrical interfaces (TP1 & TP4) as in the optical interfaces (TP2 & TP3) permits maintaining lane mapping between electrical and optical interfaces and enabling a common design that supports multiple applications.

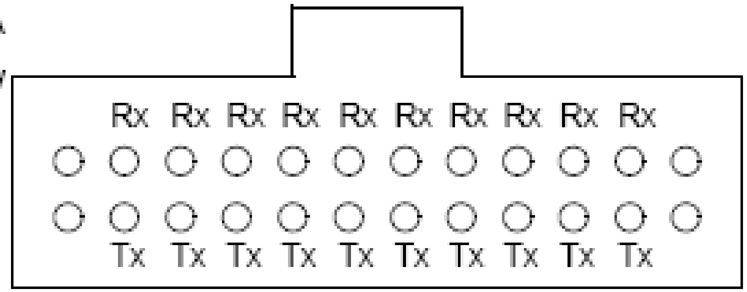
Recommendation for 10-Lane CXP Applications (2)

86.10.3.2 Optical lane assignments for 100GBASE-SR10

The ten transmit and ten receive optical lanes of 100GBASE-SR10 shall occupy the positions depicted in Figure 86–15 when looking into the MDI optical receptacle(s) with the connector keyway feature(s) on top.

Recommended Option A

Transmitter on lower row



The above image is an excerpt from 802.3ba draft 2.0 showing the choice made in Clause 86. Only the recommended option of the three options in Figure 86-15 is shown. The other two options use two single-row connectors.

The advantages if all variants, copper, active cable assemblies and fiber optics, adopt the above lane selection include:

- Less complicated ASIC – same 10 lanes used for all variants, only 10 lanes require support
- Less complicated host board design – same 10 lanes used for all variants, only 10 lanes require support
- Less complicated modules – mapping between inputs and outputs maintained between 10 lane and 12 lane applications, simplifying a common build standard and lowering costs
- Increased cable plant performance/reliability – for ribbon cables the outmost lane members see the most stress and exhibit the most variability in insertion loss and highest attenuation
- Larger market and earlier adoption – reduced ASIC & equipment design complexity and increased network media flexibility for end user

Conclusions & Recommendations

Conclusion:

- A form factor that supports the most popular media for data centers and supercomputers offers advantages to most stake holders and will be very attractive.

Recommendation:

- In Clause 85 replace Table 85-11 with the table shown on the following page.

Summary of changes to Table 85-11:

- For connector row B, left contacts B2 and B3 (corresponding to Tx lane 0 in 12-lane set numbered from 0 to 11) unused and included B17 and B18 instead.
- For connector row D, left contacts D2 and D3 (corresponding to Rx lane 0 in 12-lane set numbered from 0 to 11) unused and included D17 and D18 instead.
- Relabeled Tx and Rx lanes to run from 0 through 9 instead of from 0 through 1 and 3 through 10. Tx lane 0 now maps to contacts A2 and A3 and Rx lane 0 now maps to contacts C2 and C3.
- Changed all entries of “signal gnd” to “Signal shield” to be consistent with Figure 85-2.
- Replaced the term pin with contact since this connector has no pins.

Recommendation: Replace Table 85-11 with the following

Table 85-11 – 100GBASE-CR10 lane to MDI connector contact mapping

Tx lane	MDI connector contact	Tx lane	MDI connector contact	Rx lane	MDI connector contact	Rx lane	MDI connector contact
Signal shield	A1	Signal shield	B1	Signal shield	C1	Signal shield	D1
SL0<p>	A2		B2	DL0<p>	C2		D2
SL0<n>	A3		B3	DL0<n>	C3		D3
Signal shield	A4	Signal shield	B4	Signal shield	C4	Signal shield	D4
SL2<p>	A5	SL1<p>	B5	DL2<p>	C5	DL1<p>	D5
SL2<n>	A6	SL1<n>	B6	DL2<n>	C6	DL1<n>	D6
Signal shield	A7	Signal shield	B7	Signal shield	C7	Signal shield	D7
SL4<p>	A8	SL3<p>	B8	DL4<p>	C8	DL3<p>	D8
SL4<n>	A9	SL3<n>	B9	DL4<n>	C9	DL3<n>	D9
Signal shield	A10	Signal shield	B10	Signal shield	C10	Signal shield	D10
SL6<p>	A11	SL5<p>	B11	DL6<p>	C11	DL5<p>	D11
SL6<n>	A12	SL5<n>	B12	DL6<n>	C12	DL5<n>	D12
Signal shield	A13	Signal shield	B13	Signal shield	C13	Signal shield	D13
SL8<p>	A14	SL7<p>	B14	DL8<p>	C14	DL7p>	D14
SL8<n>	A15	SL7<n>	B15	DL8<n>	C15	DL7<n>	D15
Signal shield	A16	Signal shield	B16	Signal shield	C16	Signal shield	D16
	A17	SL9<p>	B17		C17	DL9<p>	D17
	A18	SL9<n>	B18		C18	DL9<n>	D18
Signal shield	A19	Signal shield	B19	Signal shield	C19	Signal shield	D19