Delays Through MAC and PCS

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Purpose

- Provide data on delay numbers for MAC and PCS
- Make sure delay definitions are correct

Starting Point

Table from 3badelays.pdf by Piers Dawe

Delays, spec worst *Italics: need checking and possible revision*

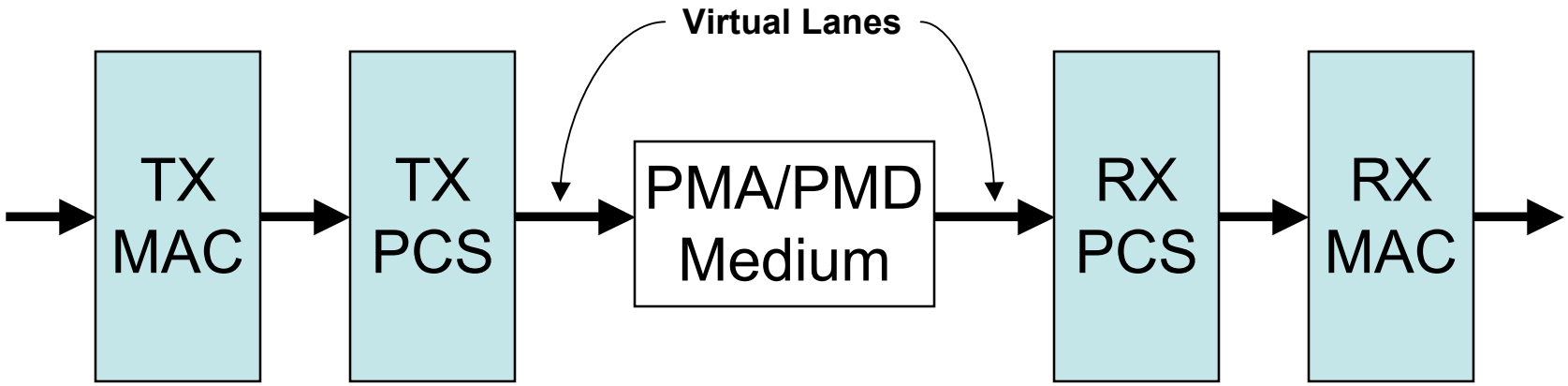
	802.3ae/ap BT at 10G	Pause_ quanta	ns		802.3ba BT at 10G	Pause_ quanta	ns
MAC, RS & MAC control	8192	**16**	819.2	MAC etc	8192	***16***	819.2
XAUI	4096	**8**	409.6				
PCS	3584	**7**	358.4	MLD PCS^	4096	***8***	409.6
FEC	**6144**	12	614.4	FEC *	**8256**	16.1	825.6
				PMA	1536	***3***	153.6
PMA & PMD	512	**1**	51.2	PMD	1024	***2***	102.4
Serial XENPAK total	16384	32	1638.4	w/o FEC	14848	29	1484.8
SFP+ with FEC total	35328	69	3532.8	w/40G FEC	20352	39.8	2035.2
				w/100G FEC	23104	45.1	2310.4
LRM PMA & PMD (EDC)	9216	**18**	921.6				
LRM XENPAK total	25088	49	2508.8	LRM class EDC	9216	18	921.6
10GBASE-T PHY (std)	25600	50	2560				
10GBASE-T total (std)	33792	66	3379.2				

* Per vallippian_01_0708

^ Guessed

- One way delay: one transmit, one medium, one receive

Delay Definitions



- One way delay: one transmit, one medium, one receive
- This means MAC delay includes both TX and RX, PCS delay includes both TX and RX
- The delay through the MAC includes the RS, MAC and MAC Control.

Using FPGA Implementation

- FPGA delays are longer than ASIC delays:
  - Clock frequencies are lower in FPGAs
  - More pipelining
- FPGA delays represent worst case scenario

Delay Numbers

FPGA Implementation

Delays, spec worst *Italics: need checking and possible revision*

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^ Guessed

100G	**40G**
175 ns (17500BT)	120 ns (4800BT)
350 ns (35000BT)	270 ns (10800BT)

NOTES:

- Simulations assume 0 bit skew between the lanes