XLAUI/CAUI Jitter Tolerance Test Requirement Proposal

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Toshihiro SUZUKI - Anritsu Corporation

Introduction

- This presentation proposes a test pattern for the Jitter test requirement in 83A.4.3.2 IEEE802.3ba D1.0.
- Testing should be under the worst conditions to achieve good product reliability.

83A.4.3 Jitter test requirements

[Editor's note: (to be removed prior to publication) - Insert or change, to include jitter test requirement

83A.4.3.1 Transmit jitter

[Editor's note: (to be removed prior to publication) - Insert or change, to include transmit jitter]

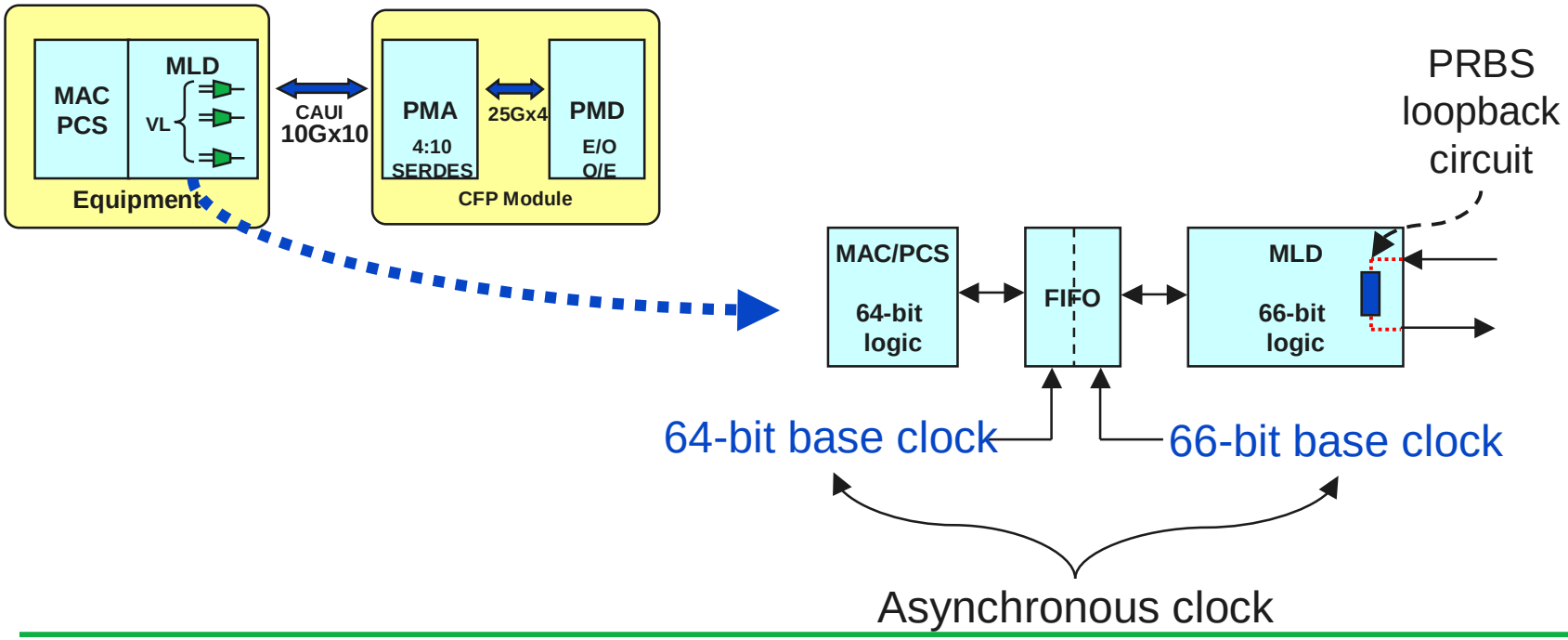
83A.4.3.2 Jitter tolerance

[Editor's note: (to be removed prior to publication) - Insert or change, to include jitter tolerance]

Jitter Tolerance Test Pattern Proposal

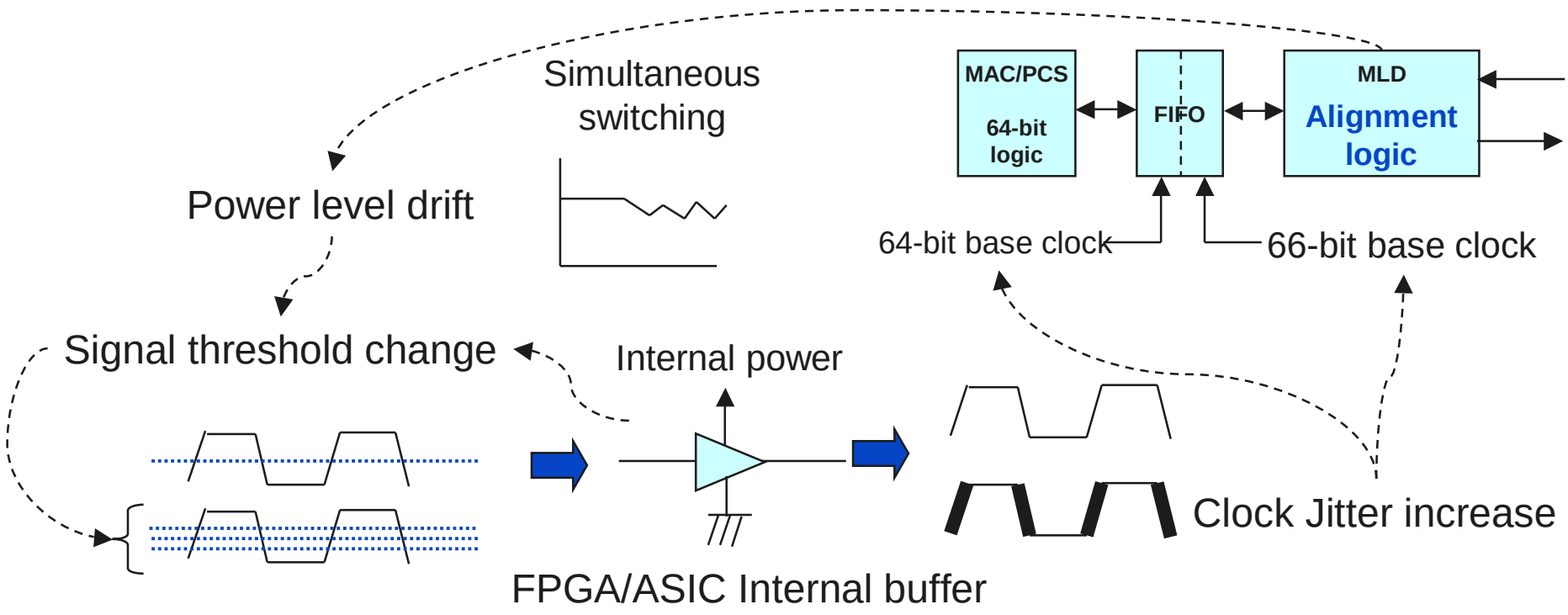
Assumptions about Circuit

- Size of working circuit in MLD block changes according to whether MLD function operating or not
- PRBS Loopback test circuit relatively smaller than MLD alignment circuit
- Logic circuit uses at least two asynchronous clocks (64-bit and 66-bit logic)



Jitter Tolerance Test Pattern Proposal

- Simultaneous switching of large-scale circuit in FPGA/ASIC causes internal power level drift
- Power level drift changes internal buffer threshold level
  - ➔ Jitter in signal output from buffer increases

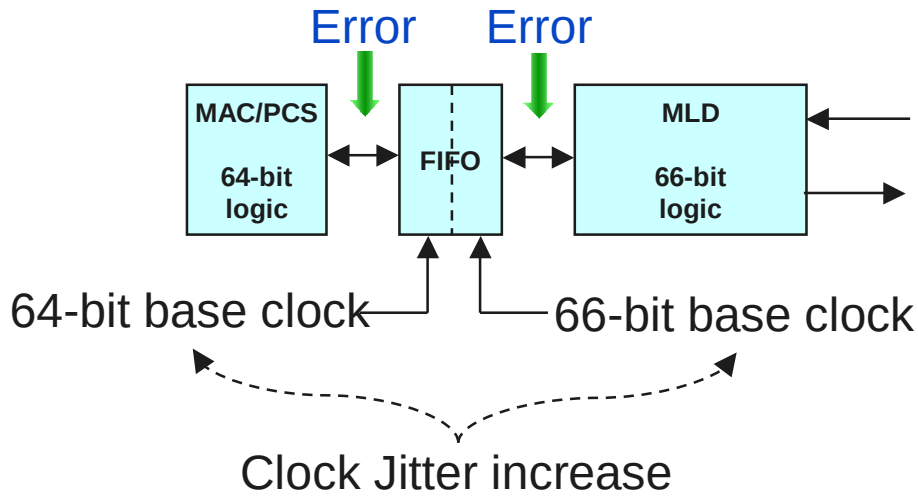


Jitter Tolerance Test Pattern Proposal

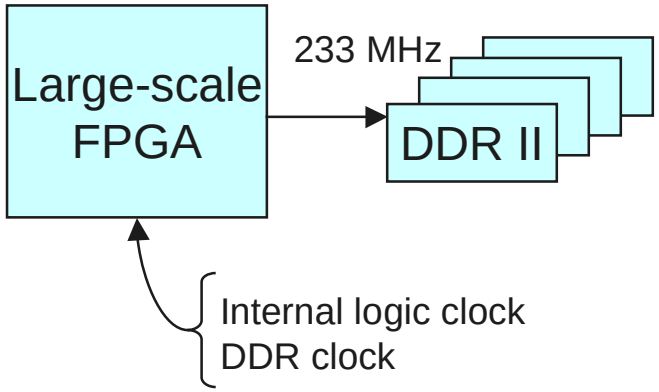
- Different increases in Jitter and timings between two asynchronous clocks (64-bit and 66-bit sides) can cause error at FIFO or decrease in phase margin of internal circuit

■ MLD Input pattern increases working logic circuit (MLD alignment)

➔ Simultaneous switching in FPGA/ASIC increases Jitter causing internal bit errors

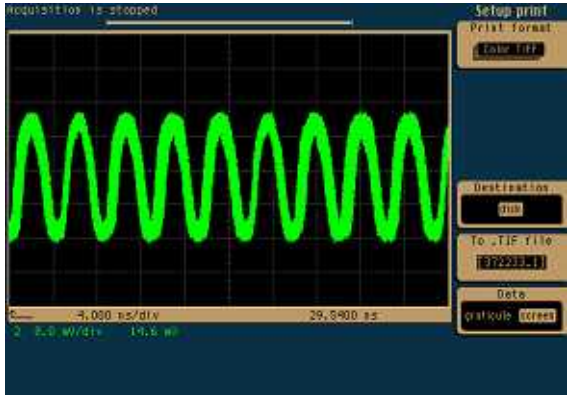


Simultaneous Switching Increases Jitter

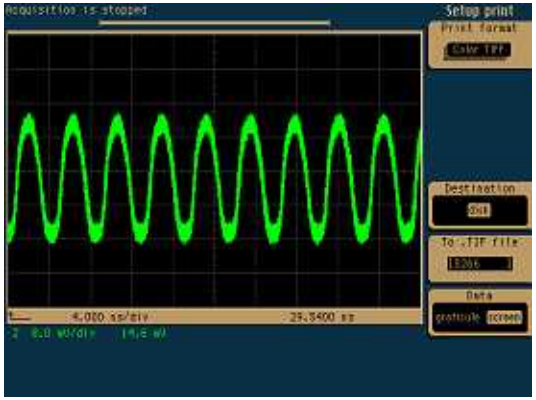


Example
Simultaneous switching causes internal power level drift between between two asynchronous clocks in FPGA causing error at DDR access

Error at DDR II



No error at DDR II



Test Jitter tolerance under worst condition

Jitter Tolerance Test Pattern

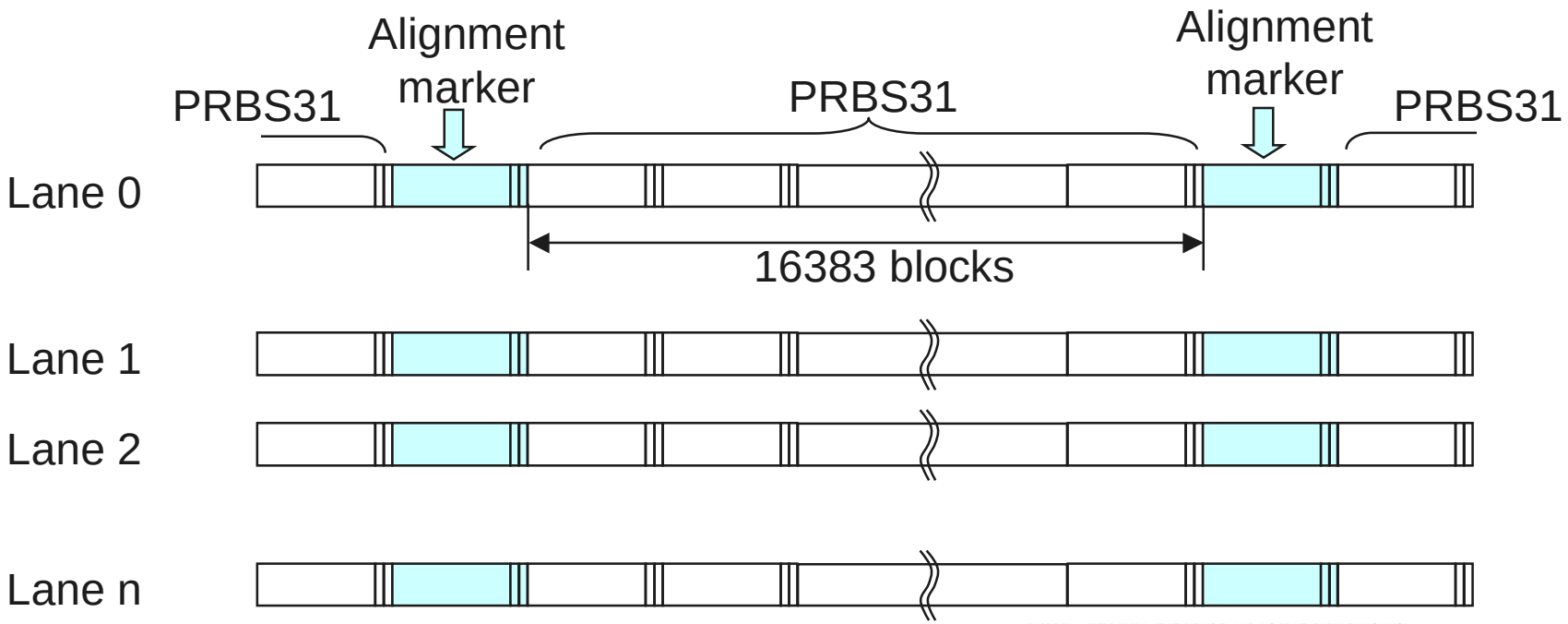


Table 82–2—Alignment marker encodings

Lane Number	Encoding[a] $\{M_0, M_1, M_2, M_3, M_4, M_5, M_6, M_7\}$	Lane Number	Encoding $\{M_0, M_1, M_2, M_3, M_4, M_5, M_6, M_7\}$
0	0xc1, 0x68, 0x21, 0xf4, 0x3e, 0x97, 0xde, 0x0b	10	0xfd, 0x6c, 0x99, 0xde, 0x02, 0x93, 0x66, 0x2d
1	0x9d, 0x71, 0x8e, 0x17, 0x62, 0x8e, 0x71, 0xe8	11	0xb9, 0x91, 0x55, 0xb8, 0x46, 0x6e, 0xaa, 0x47
2	0x59, 0x4b, 0xe8, 0xb0, 0xa6, 0xb4, 0x17, 0x4f	12	0x5c, 0x b9, 0xb2, 0xed, 0xa3, 0x46, 0x4d, 0x32
3	0x4d, 0x95, 0x7b, 0x10, 0xb2, 0x6a, 0x84, 0xef	13	0x1a, 0xf8, 0xbd, 0xab, 0xe5, 0x07, 0x42, 0x54
4	0xf5, 0x 07, 0x09, 0x0b, 0x0a, 0xf8, 0xf6, 0xf4	14	0x83, 0xc7, 0xca, 0xb5, 0x7c, 0x38, 0x35, 0x4a
5	0xdd, 0x14, 0xc2, 0x50, 0x22, 0xeb, 0x3d, 0xaf	15	0x35, 0x36, 0xcd, 0xeb, 0xca, 0xc9, 0x32, 0x14
6	0x9a, 0x4a, 0x26, 0x15, 0x65, 0xb5, 0xd9, 0xea	16	0xe4, 0x31, 0x4e, 0x30, 0x3b, 0xce, 0xb3, 0xcf
7	0x7b, 0x45, 0x66, 0xfa, 0x84, 0xba, 0x99, 0x05	17	0xad, 0xd6, 0xb7, 0x35, 0x52, 0x29, 0x48, 0xca
8	0xa0, 0x24, 0x76, 0xdf, 0x5f, 0xdb, 0x89, 0x20	18	0x5f, 0x66, 0x2a, 0x6f, 0xa0, 0x99, 0xd5, 0x90
9	0x68, 0xc9, 0xfb, 0x38, 0x97, 0x36, 0x04, 0xc7	19	0xc0, 0xf0, 0xe5, 0xa9, 0x3f, 0x0f, 0x1a, 0x16