

Choosing 25G CRU BW and CDR BW Wisely

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Background Statement

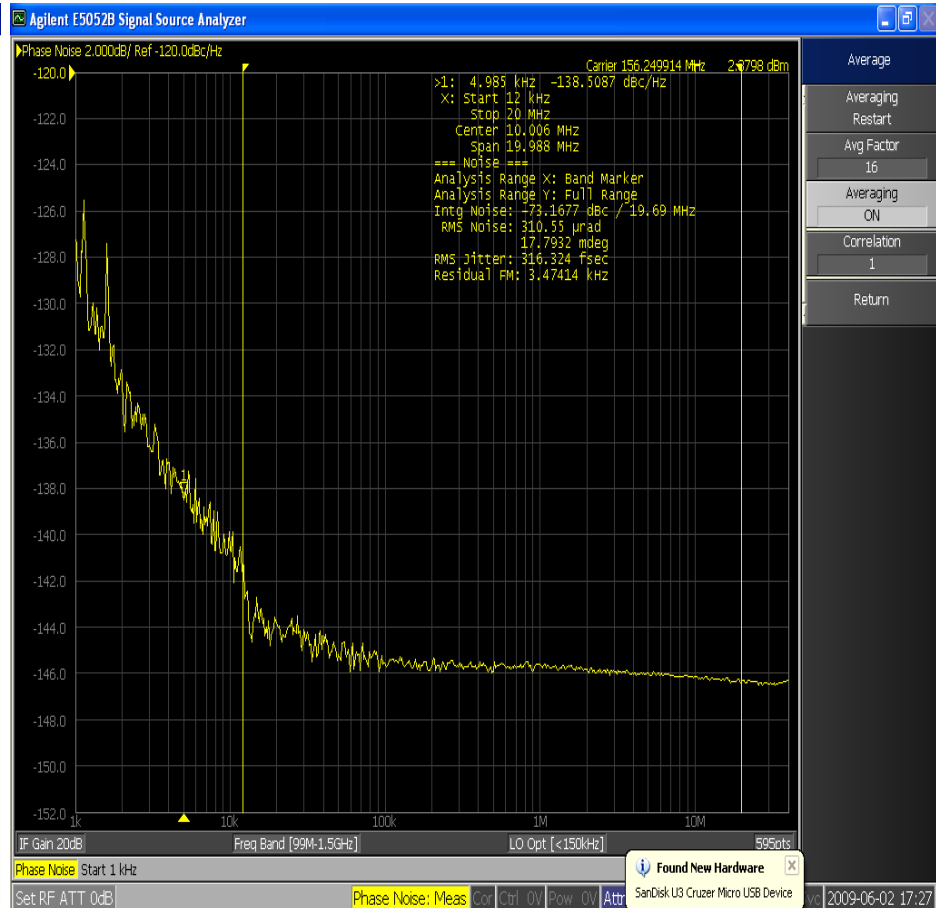
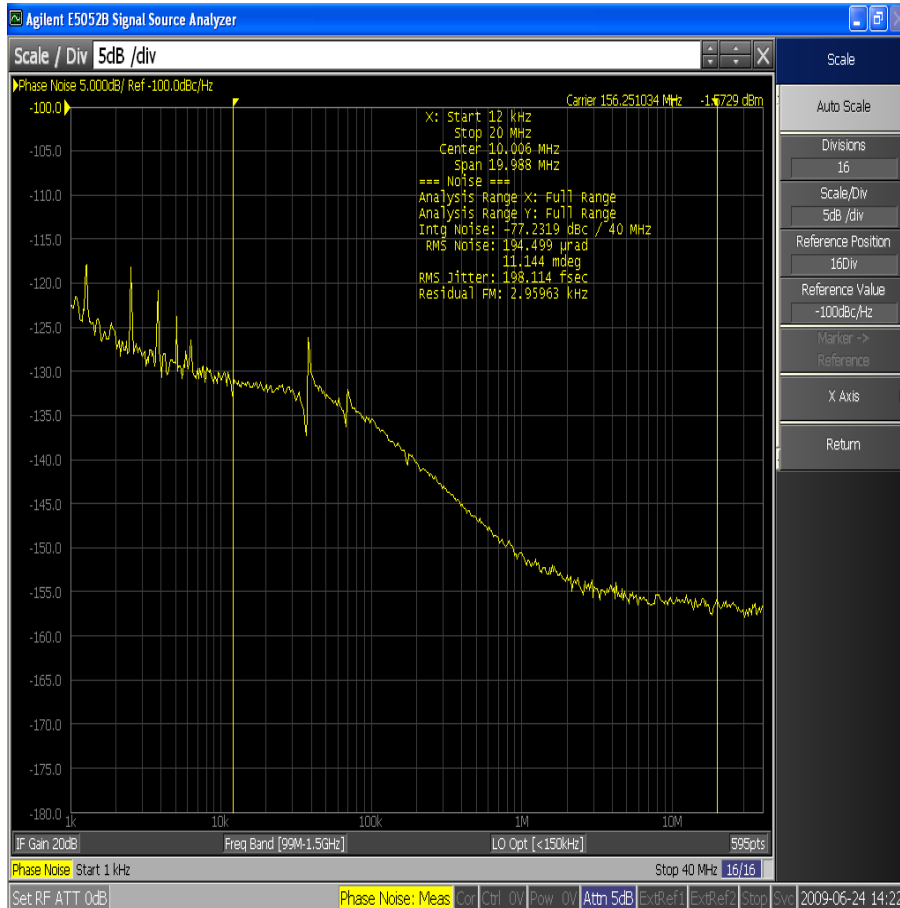
- **88.8.5.3 Reference Receiver, defines CRU used for TDP measurement has 10 MHz BW**
- **88.8.8 Transmitter optical waveform, is defined with CRU with 10 MHz corner frequency**
- **88.8.10 Stress receiver sensitivity, table 88-13 had effective corner frequency of 4 MHz CDR**
- **The recommendation given in ghiasi_02_0909 was to reduce the CRU BW from 10 MHz to 7 MHz and use the same corner frequency for jitter tolerance**
- **The decision in Chicago was to correct the jitter tolerance table 88-13 corner frequency from 4 MHz to 10 MHz, making the specification consistent but there were no consensus on the other part of the recommendation to make the CRU and CDR BW both 7 MHz.**

Consideration for CRU and CDR BW

- **Consideration for the golden PLL CRU BW**
 - **Oscillator phase**
 - Typically no benefit as the phase noise is flat >1 MHz
 - **Crosstalk**
 - High frequency effect >> CRU BW
 - **VCO Phase noise**
 - No benefit for CRU BW > 5 MHz
- **Consideration for CDR BW**
 - **Pattern dependent effects**
 - Does not apply to 64B/66B with its spectrum in the 100KHz
 - **Power**
 - Higher BW loop BW require analog loop filter resulting in higher power
 - **Receiver with DFE**
 - DFE receiver timing recovery introduces latency making jitter tolerance more strenuous, this is the reason LRM and KR jitter tolerance as they are more accommodating.

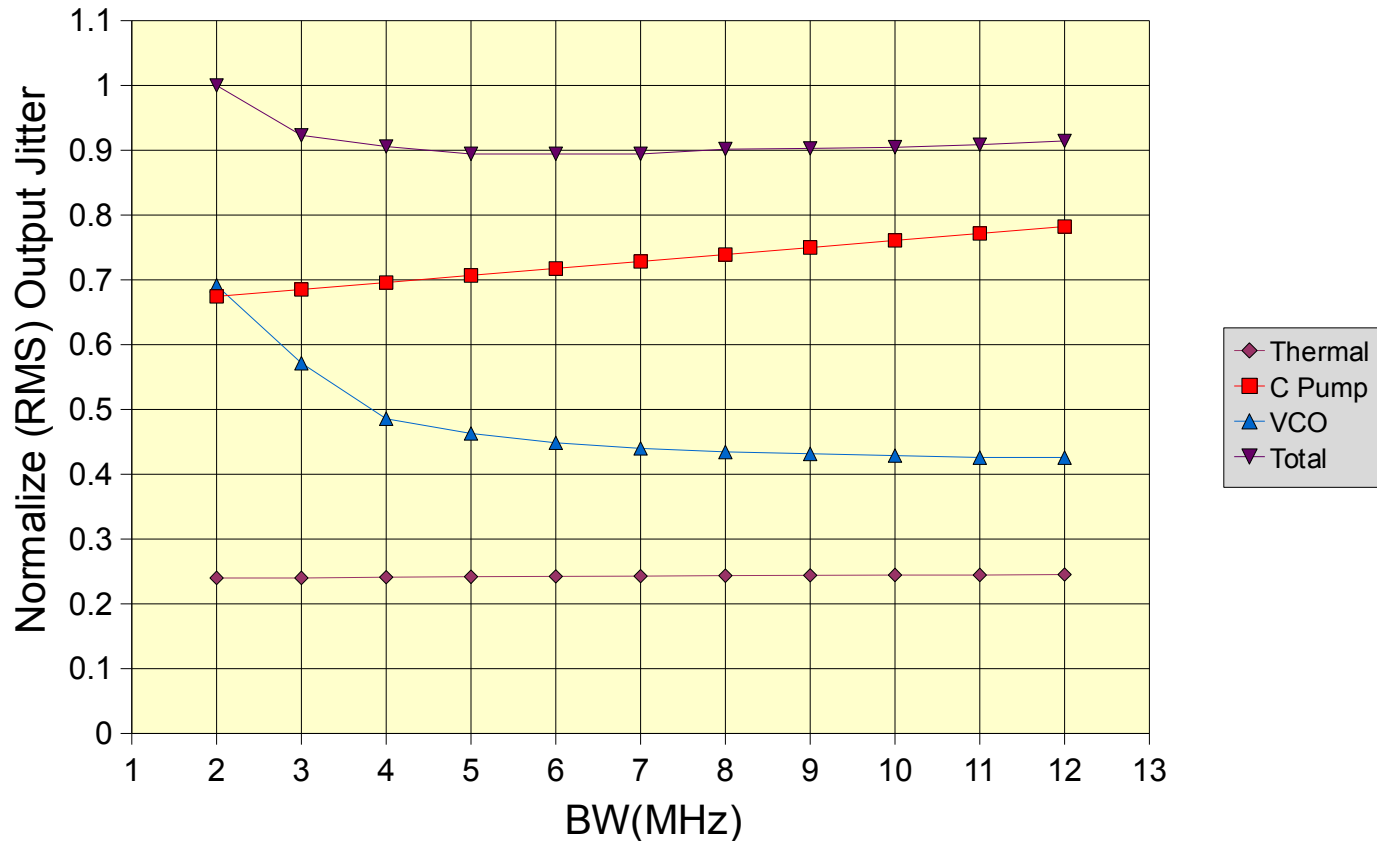
Typical Low Cost Oscillator Phase Noise Plot

- Most oscillator phase noise is flat after 1 MHz
 - There is no benefit to higher CRU BW!



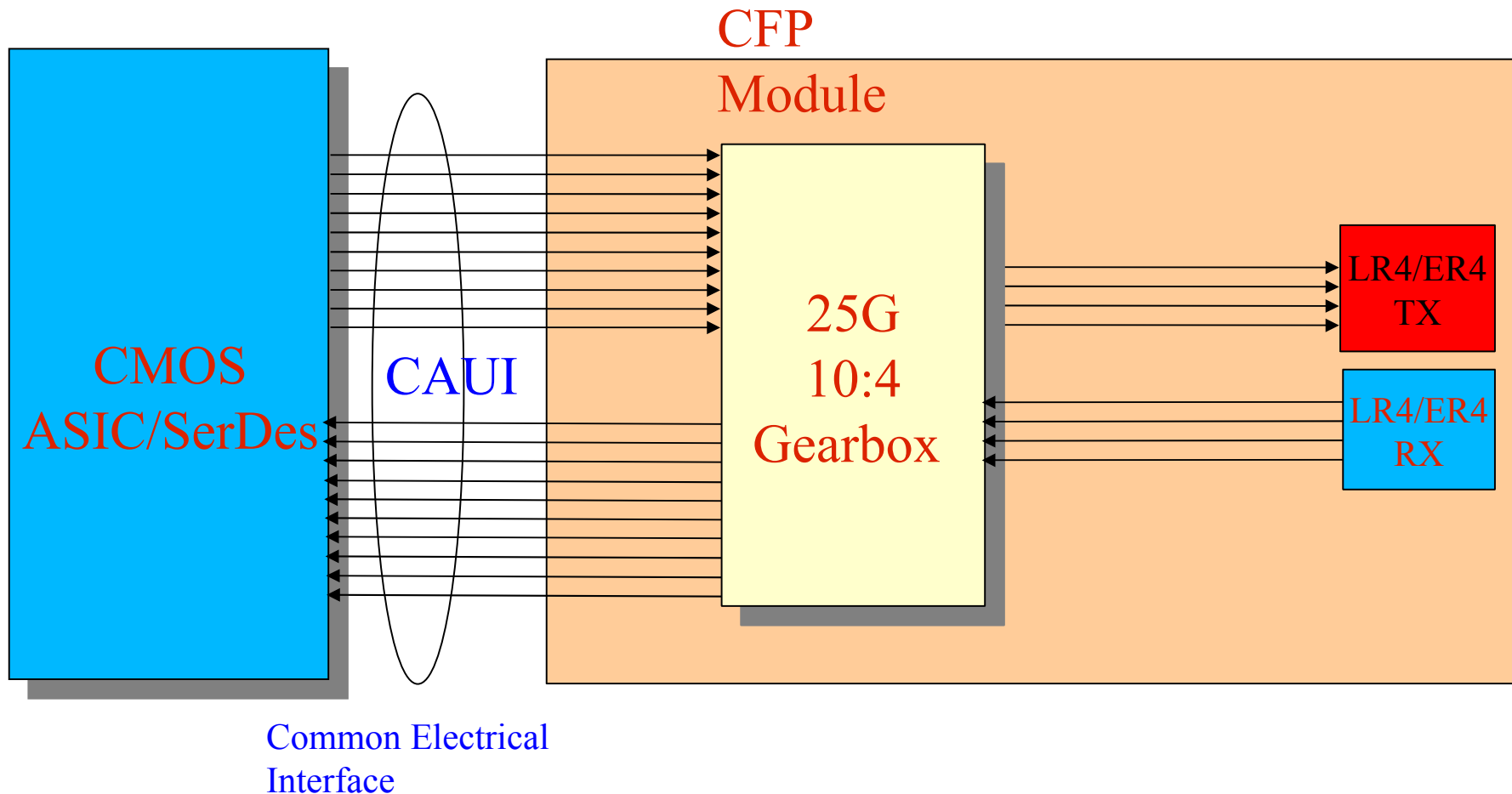
SerDes Transmitter Relative Jitter

- Thermal, charge pump, VCO, and total relative output jitter as function of BW
 - BW of 5-7 MHz gives best total output jitter and there is no benefit having CRU BW > 7 MHz



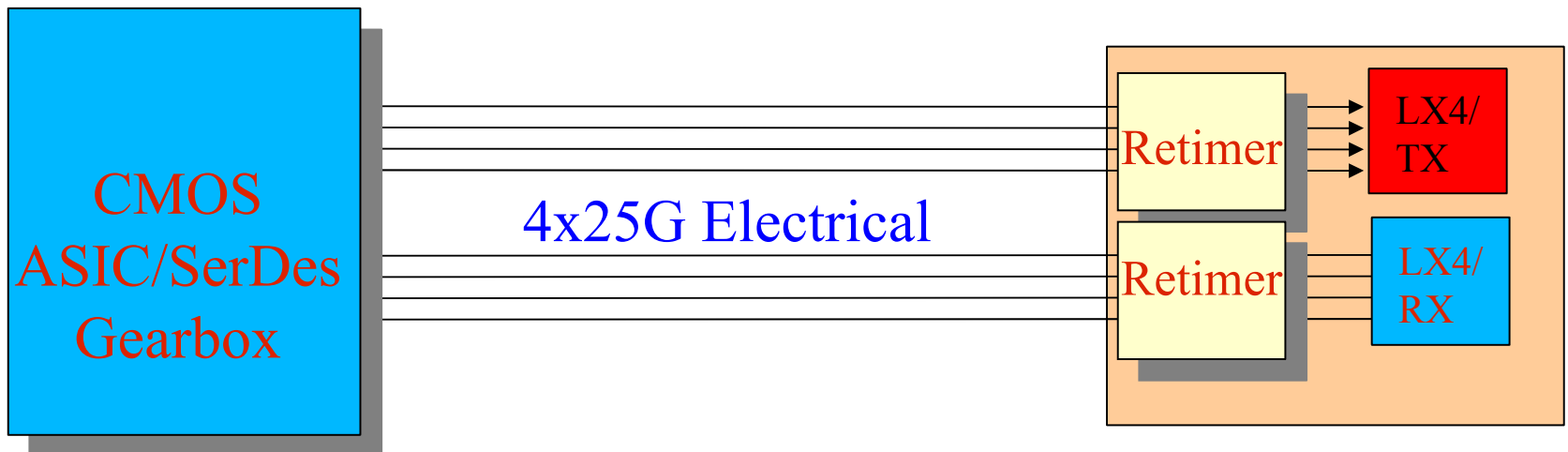
100GBase-LR4/ER4 Current Implementation

- Module interface based on CAUI
- The jitter tolerance defined for LR4/ER4 will remain for ever!



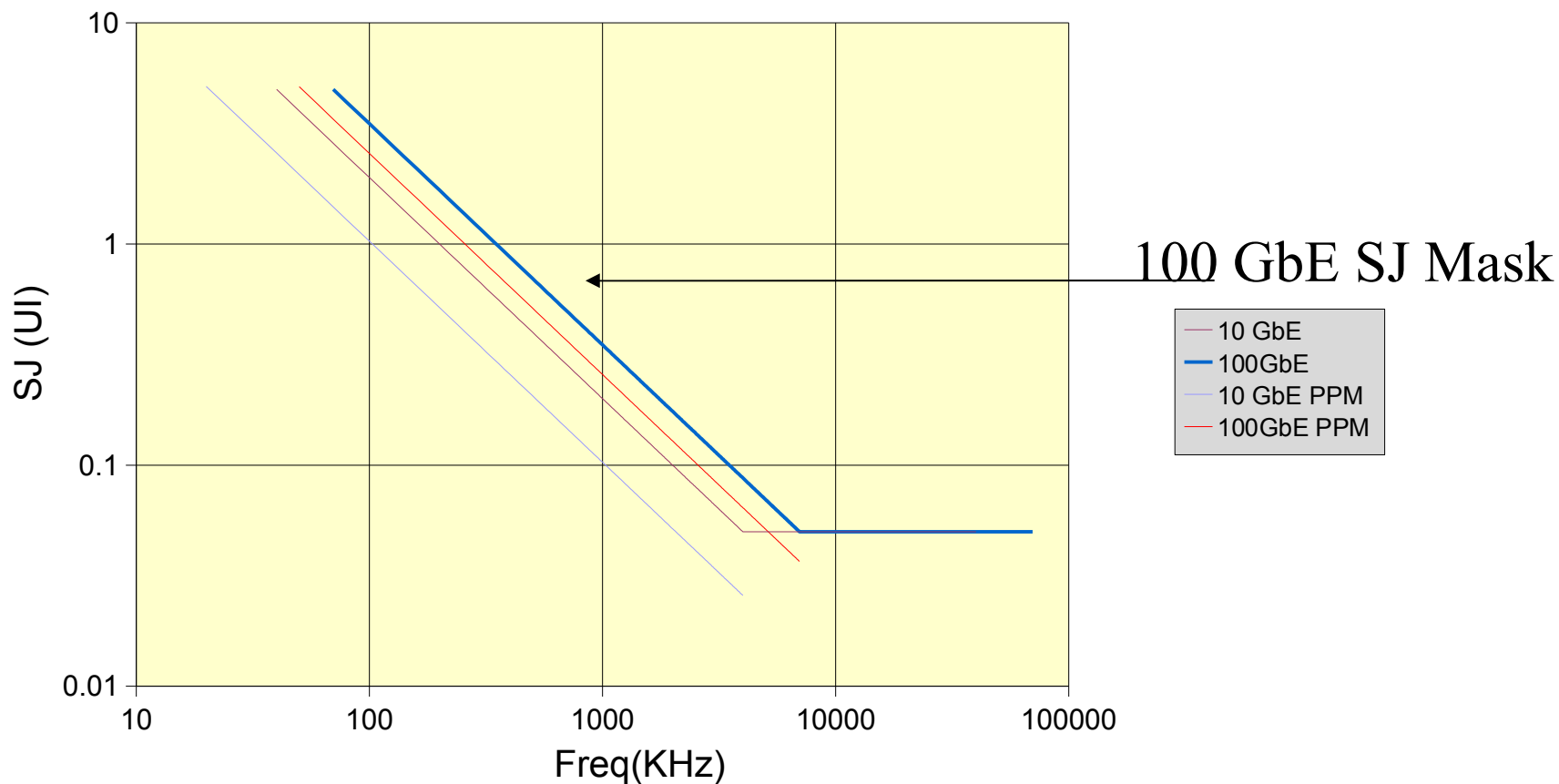
Next Generation 100GBASE-LR4/ER4

- Next ASIC/Serdes will integrate the 4x25G gearbox
- Interface operating at 25.7 Gbd will require some DFE
- The retimer in the module will pass through SJ stress
- The 4x25G host receiver must absorb the SJ!



10 GbE SJ Mask and Proposed 100 GbE Mask

- 100 GbE mask with proposed compromised 7 GHz BW



Overview of 10GbE Jitter Tolerance Specifications

- **SR/LR/ER**
 - 4 MHz transmit CRU
 - Comprehensive stress sensitivity with 4 MHz SJ corner frequency
- **LRM**
 - 4 MHz transmit CRU
 - Tested unstress 5UI @ 75 Khz and 1 UI @ 375 Khz
- **KR**
 - 4 MHz transmit CRU
 - Comprehensive stress sensitivity with SJ of 0.115UI >15 MHz

Summary

- **Current 10 MHz CRU BW has no benefit for the transmitter but burdens the receiver in term of power, implementation and is not future looking to host operating with 4x25G electrical**
- **The 7 MHz CRU and SJ corner frequency is a compromise between the current 10 MHz CRU BW and 4 MHz SJ corner frequency**
 - **5-7 MHz BW results in the lowest output jitter**
 - **SJ corner frequency of ≤ 7 MHz allow lower cost and power DFE receiver**
- **Proposed resolution assuming 7 MHz for CRU and SJ corner frequency**
 - **Change 88.8.5.3 and 88.8.8 CRU BW from 10 MHz to 7 MHz**
 - **Change 88.8.10 SJ corner frequency from 4 MHz to 7 MHz**
 - **$f < 70$ KHz not specified**
 - **$70 \text{ KHz} \leq f \leq 7 \text{ MHz}$ $3.5 \times 10^5 / f + s - 0.05$**
 - **$7 \text{ MHz} \leq f \leq 10 \text{ LB}$ $0.05 \leq S \leq 0.15$**