

Cl 85 SC 85.11.1.1 P272 L # 1
McGrath, Jim Cinch Connectors

Comment Type T Comment Status A

Clause 85.11.1.1. Style 1 Hardware Contact Definitions Table 85-12

This table requires that the current low speed electrical specification for the QSFP+ cable as defined by SFF8436 be violated. It should be a goal of IEEE802.3ba to facilitate the use industry standard cables that are defined in other documents. SFF8436 includes an EEPROM cable management interface with a detailed memory map. The functional requirements of Table 85-12 have been addressed in the SFF8436 memory map.

SuggestedRemedy

Table 85-12 should be deleted.

Response Response Status C

ACCEPT IN PRINCIPLE.
See response comment#2.

Cl 85 SC 85.11 P274 L1 # 2
Oganessyan, Gourgen Quellan (part of Intersil)

Comment Type TR Comment Status A

Hardware contact definitions in Table 85-12 violate the QSFP connector specification of SFF-8436: the table requires that contact 27 be open in the case of a copper module, while the QSFP spec defines this contact as module presence pin and requires it to be grounded in the module. As a result of this discrepancy, passive QSFP copper cables created for all other standards using SFF-8436 will not be interoperable with 40GE. Conversely, if the connector is pinned out per table 85.11, the cable will not as a general rule be able to be used in Infiniband and other equipment already deployed in the field. While not strictly a problem from IEEE point of view, I believe this incompatibility will have negative impact on the broad market potential and future adoption of this standard. In addition, electronic keying is also required for CR10 and is currently missing, and defining it along the lines of table 85-12 causes even more severe discrepancy with the CXP specification (see my next comment).

SuggestedRemedy

The entire section 85.11.1.1.1 as currently written needs to be deleted. There does not appear to be a way to define electronic keying without violating the QSFP spec. The reasonable solution is to use the SFF-8436 management interface, which has provisions for identifying the module as a copper or an optical module. Also, it is obvious that everyone will end up using the management interface anyway, because it is de facto industry standard and it does the job. If management interface definition is beyond the scope of the project, then we could either make an informative statement referencing the SFF-8436 management interface; or we could make a statement along the lines of "Electronic keying shall be used in order to enable detection of Style-1 plug connector versus fiber module or no module present. The details of implementation of such keying are beyond the scope of this standard". This would prompt people to use the management interface without calling it out, or it would enable proprietary/custom designs along the lines of table 85-12.

Response Response Status C

ACCEPT IN PRINCIPLE.
The basis for Table 85-12 requires a distinction between a module and a direct attach plug. If this distinction is clear in SFF-8436, as I had assumed when creating the table, Table 85-12 is not in conflict with SFF-8436. Given the number of similar comments the distinction is not clear or not made.

Delete: sub-clause 85.11.1.1.1
Add: 85.11.4 Electronic keying

Electronic keying can be used to enable the detection of Style-1 40GBASE-CR4 MDI connectors or 100GBASE-CR10 MDI cable assembly plugs versus fiber modules or no modules present. Specifications of electronic keying are beyond the scope of this standard.

CI 85 SC 85.11 P275 L44 # 3
Oganessyan, Gourgen Quellan (part of Intersil)

Comment Type TR Comment Status A

Electronic keying needs to be defined for CR10 as well, in order to enable distinction of copper from fiber modules by the host. However, there does not appear to be a way to do this via hardware keys without violating the CXP spec, particularly as it is defined in the InfiniBand Architecture Specification. The only way to do this along the lines of Table 85-12 would be to have contact C20 open, and contact C21 pulled low. But C20 is the module presence pin that is required to be grounded in all cases by the CXP spec, and C21 is a shared interrupt/reset pin, so pulling it low will disrupt the operation of InfiniBand equipment. As a result, passive cables designed for Infiniband will not interoperate with CR10.

SuggestedRemedy

Add an Electronic Keying section, stating: "Electronic keying shall be used in order to enable detection of CR10 plug connector versus fiber module or no module present. The details of implementation of such keying are beyond the scope of this standard"

Response Response Status C

ACCEPT IN PRINCIPLE.
See response comment#2.

CI 83B SC 83B.2 P403 L24 # 4
Rabinovich, Rick Alcatel-Lucent

Comment Type T Comment Status A

The equation (83B-3) has an inequality sign for the |SDD21| Host Compliance Board insertion loss.

Parameters for HCB and MCB Equations should use an equal sign, for example, equations (86A-4) and (86A-5) for the SDD21 HCB and MCB in CL86A Subclause 86A.5.1.1.1 use equal sign "=" correctly.

SuggestedRemedy

Replace the inequality sign with an equal sign "=".

Response Response Status C

ACCEPT IN PRINCIPLE.

See comment#186

CI 83B SC 83B.2 P404 L24 # 5
Rabinovich, Rick Alcatel-Lucent

Comment Type T Comment Status A

The equation (83B-4) has an inequality sign for the |SDD21| Module Compliance Board insertion loss.

Parameters for HCB and MCB Equations should use an equal sign, for example, equations (86A-4) and (86A-5) for the SDD21 HCB and MCB in CL86A Subclause 86A.5.1.1.1 use equal sign "=" correctly.

SuggestedRemedy

Replace the inequality sign with an equal sign "=".

Response Response Status C

ACCEPT IN PRINCIPLE.

Delete "The differential insertion loss, CPIL, expressed in decibels, for the MCB shall be less than CPILmax, as defined by Equation (83B-4)"
Replace with:"

The reference MCB test fixture PCB insertion loss is given in Equation (83B-4-[note change <= to =]). The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss should be accounted for in the measurements.

CI 85 SC 85.2 P240 L40 # 6
Marris, Arthur Cadence

Comment Type E Comment Status A

unnecessary hyphen

SuggestedRemedy

Change 'The-' to 'The '

Response Response Status C

ACCEPT.
See suggested remedy

Cl 45 **SC 45.2.1** **P40** **L5** # **7**
 Marris, Arthur Cadence
Comment Type E **Comment Status A**
 Change 'that packaged' to 'that is packaged'
SuggestedRemedy
 as above
Response **Response Status C**
 ACCEPT.

Cl 45 **SC 45.2.1.88** **P60** **L41** # **8**
 Marris, Arthur Cadence
Comment Type E **Comment Status A**
 Change 'Register_1.174' to 'Register 1.174'
SuggestedRemedy
 As above
Response **Response Status C**
 ACCEPT.

Cl 74 **SC 74.8.4.1** **P124** **L40** # **9**
 Marris, Arthur Cadence
Comment Type T **Comment Status A**
 74.8.4.1 and 74.8.4.2 need to be updated for multi-lane operation
SuggestedRemedy
 Change to:

FEC_corrected_blocks_counter and FEC_corrected_blocks_counter_i count once for each corrected FEC block processed when FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication is OK. This is a 32-bit counter. These variables may be mapped to the registers defined in 45.2.1.87 (1.172, 1.173) and 45.2.1.89 (1.176 to 1.215).

FEC_uncorrected_blocks_counter and FEC_uncorrected_blocks_counter_i count once for each uncorrected FEC block processed when FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication is OK. This is a 32-bit counter. These variables may be mapped to the registers defined in 45.2.1.88 (1.174, 1.175) and 45.2.1.90 (1.216 to 1.255).

Response **Response Status C**
 ACCEPT IN PRINCIPLE.

Change:

FEC_corrected_blocks_counter counts once for each corrected FEC blocks processed when FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication is OK.

to:

FEC_corrected_blocks_counter (for single lane PHYs) or FEC_corrected_blocks_counter_i (for multi-lane PHYs) count once for each corrected FEC block processed when FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication is OK. These are 32-bit counters. These variables are accessed through a management interface that may be mapped to the registers defined in 45.2.1.87 (1.172, 1.173) and 45.2.1.89 (1.176 to 1.215).

Change:

FEC_uncorrected_blocks_counter counts once for each uncorrected FEC blocks processed when FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication is OK.

to:

FEC_uncorrected_blocks_counter (for single lane PHYs) or FEC_uncorrected_blocks_counter_i (for multi-lane PHYs) count once for each uncorrected FEC block processed when FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication is OK. These are 32-bit counters. These variables are accessed through a management interface that may be mapped to the registers defined in 45.2.1.88 (1.174, 1.175) and 45.2.1.90 (1.216 to 1.255).

Cl 73 SC 73.10.1 P106 L8 # 10
Marris, Arthur Cadence

Comment Type T Comment Status A

Implement 802.3 maintenance request 1209:

http://grouper.ieee.org/groups/802/3/maint/requests/maint_1209.pdf

SuggestedRemedy

Change DME_receive_idle to an_receive_idle

also do the same for mr_parallel_detection_fault variable

Response Response Status C

ACCEPT.

Cl 87 SC 87.1 P313 L35 # 11
Marris, Arthur Cadence

Comment Type T Comment Status A

IEEE is not the same as ISO/IEC

SuggestedRemedy

Delete '(IEEE)'

Response Response Status C

ACCEPT IN PRINCIPLE.

Some clauses in the base standard (e.g. 46, 53, 57) use "to the ISO/IEC (IEEE) OSI" while others (e.g. 22, 54, 65) use just "to the ISO/IEC OSI".

Delete "(IEEE)" here, in subclause 88.1 and also in subclause 81.1
See also comment #12

Cl 88 SC 88.1 P343 L34 # 12
Marris, Arthur Cadence

Comment Type T Comment Status A

IEEE is not the same as ISO/IEC

SuggestedRemedy

Delete '(IEEE)'

Response Response Status C

ACCEPT IN PRINCIPLE.

See Response to comment #11

Cl 00 SC 0 P L # 13
Anslow, Peter Nortel Networks

Comment Type E Comment Status A

In the equations within the draft, the use of "x" to signify multiplication is inconsistent. According to the style manual, A multiplication sign "x" should only be used to indicate multiplication of two numbers (e.g., "1 x 10" or "3 cm x 4 cm").

Some equations do not use "x" e.g. "10log" or "2f" and others use "10 x log" or "2 x f"

SuggestedRemedy

Remove all of the "x"s from equations:

85-1, 85-14, 85-15, 85-17, 85-25, 85-26, 85-27, 85-28, 85-34, 85-36, 85-37, 85-38, 85-39, 85-40, 85-41, 85-42, 83A-1, 83A-2, 83B-4, 85A-3, 85A-4

Note there is another comment against equation 85A-4

Remove all but the first "x" from equation 85-16

Change equation 85-23 from " $= -0.7 - 0.2x10^{-9}(fx106)$ " to " $= -0.7 - 0.2x10^{-3}f$ "

Change equation 85-24 from " $= -0.7 + 0.2x10^{-9}(fx106)$ " to " $= -0.7 + 0.2x10^{-3}f$ "

Remove the first two "x"s from equations 85-31 and 85-32

Remove the "x" between "20" and "log" in equations 85-35, 85A-1 and 85A-2

Response Response Status C

ACCEPT.

Also see comment #54 regarding style

Some of the suggested equations may be modified by other comments.

Cl 00 SC 0 P L # 14
Anslow, Peter Nortel Networks

Comment Type T Comment Status A

The draft is inconsistent on how it defines the frequency break points in equations. For some multi-segment limit lines, there is a small discontinuity at the break point, so it should be clear which limit applies to the exact break frequency.

SuggestedRemedy

In equations 85-39, 85-40, 85-41, 85-42 change " <10 " to " ≤ 10 "

In equation 86A-1, 86A-2, 86A-3, 86A-7, 86A-8, 86A-9, 86A-10, 86A-11, 86A-12, 86A-13, 86A-14, 86A-19, 86A-20 for all the frequency segments except the highest segment, change the second inequality from \leq to $<$. e.g. for equation 86A-8 change " $0.01 \leq f < 2.5$ " to " $0.01 <= f < 2.5$ " and change " $2.5 \leq f <= 5$ " to " $2.5 <= f < 5$ "

Response Response Status C

ACCEPT IN PRINCIPLE.

Change where appropriate to make the equations consistent across the draft as per suggested response

CI 00 SC 0 P L # 15
 Anslow, Peter Nortel Networks

Comment Type T Comment Status A

The draft is not consistent in its use of parameter names and figures illustrating limit lines. For example "Return loss" and "Reflection response, SDD22" are used for the same parameter.

See comment #327 against D 2.1

For a detailed discussion of this issue see dambrosia_01_0909.pdf

SuggestedRemedy

Apply changes as described in dambrosia_01_0909.pdf

Response Response Status C

ACCEPT IN PRINCIPLE.

Apply changes as described in dambrosia_01_0909.pdf "Detailed changes" and "Proposal for consistency for graphs" slides with the exception of the "Indicate compliant region" bullet.

A vote of the task force on the above response was:

Yes 30

No 0

See also comment 85

CI 80 SC 80.5 P138 L5 # 16
 Anslow, Peter Nortel Networks

Comment Type T Comment Status A

The definition of Skew Variation is not correct.
 Consider a link with relative delays on 4 lanes of 0, 20, 20, 20 UI.

The definition of Skew is:

Skew is defined as the difference between the times of the earliest PCS lane and latest PCS lane for the one to zero transition of the alignment marker sync bits.

So the skew of the above example is 20 UI.

Now change the delay in the second lane so that the relative delays become:
 0, 0, 20, 20 UI. The Skew is still 20 UI

Skew Variation is defined as:

Skew Variation is defined as the difference between the lowest value of Skew and the highest value of Skew over the entire time that the link is in operation.

So the Skew Variation after the change is 0 UI. However, the delay on the second lane has changed by 20 UI so you need 20 bits in the gearbox buffer.

SuggestedRemedy

Change:

"Skew Variation is defined as the difference between the lowest value of Skew and the highest value of Skew over the entire time that the link is in operation."

to:

"Skew Variation is defined as the change in skew between any PCS lane and any other PCS lane over the entire time that the link is in operation."

Response Response Status C

ACCEPT.

CI 83 SC 83.5.4 P213 L13 # 17
 Anslow, Peter Nortel Networks

Comment Type E Comment Status A

Double full stop ".."

SuggestedRemedy

Change ".." to "."

Response Response Status C

ACCEPT.

Cl **83A** SC **83A.3.3** P**385** L**19** # **18**
 Anslow, Peter Nortel Networks

Comment Type **E** Comment Status **A**

In Table 83A-1, the "Maximum De-emphasis" is given as 7.0 dB
 In Table 83B-3, the "Maximum De-emphasis" is given as 6.0 dB
 In accordance with the response to comment #501 against Draft 1.1, these should be 7 dB and 6 dB respectively.

Also on page 398 line 33 7.0 dB should be 7 dB

SuggestedRemedy

In Table 83A-1, change "7.0" to "7"
 In Table 83B-3, change "6.0" to "6"
 On page 398 line 33, change "7.0" to "7"

Response Response Status **C**
 ACCEPT.

Cl **83A** SC **83A.3.3.3** P**387** L**12** # **19**
 Anslow, Peter Nortel Networks

Comment Type **E** Comment Status **A**

The differential output return loss is required to be met from 10 MHz, but Figure 83A-6 stops at 50 MHz.
 Also applies to Figures 83A-7, 83A-10, 83A-11

SuggestedRemedy

Extend Figures 83A-6, 83A-7, 83A-10, 83A-11 to 10 MHz

Response Response Status **C**
 ACCEPT.

Cl **83A** SC **83A.3.3.5** P**382** L**32** # **20**
 Anslow, Peter Nortel Networks

Comment Type **E** Comment Status **A**

Several references in Clauses 83A and 83B that should be cross-references are not.

SuggestedRemedy

Make the following references to other places in the draft cross-references.

Page 380, line 32, "Clause 83"
 Page 386, line 43, "83.5.10"
 Page 388, lines 33 to 38 contain 5 instances (also "83A-1" should be "Table 83A-1")
 Page 395, line 11, "Annex 48B.3" should be blue
 Page 401, line 19, "Table 83B-1"

Response Response Status **C**
 ACCEPT.

See suggested remedy

Cl **83B** SC **83B.2.1** P**405** L**40** # **21**
 Anslow, Peter Nortel Networks

Comment Type **E** Comment Status **A**

In Table 83B-2 two references to equations should say "Equation 83B-x"

SuggestedRemedy

Change "See 83B-5" to "See Equation (83B-5)"
 Change "See 83B-6" to "See Equation (83B-6)"

Response Response Status **C**
 ACCEPT.

See suggested remedy

CI 85 SC 85.10.3 P263 L4 # 22
 Anslow, Peter Nortel Networks

Comment Type E Comment Status A

The Cable assembly insertion loss deviation is required to be met from 50 MHz to 7.5 GHz. However, in Figure 85-7 the limits are illustrated from 50 MHz to 6 GHz only. Also applies to Figure 85-14 where the lines cannot be seen from 8 to 10 GHz. Also Figure 85A-1 is plotted to 6 GHz but only applies to 5.15625 GHz

SuggestedRemedy

Extend the lines in Figure 85-7 to 7.5 GHz
 Make the lines visible in Figure 85-14 up to 10 GHz
 Stop the line in Figure 85A-1 at 5.15625 GHz

Response Response Status C

ACCEPT.
 See suggested remedy

CI 85 SC 85.10.4 P263 L28 # 23
 Anslow, Peter Nortel Networks

Comment Type E Comment Status A

Double full stop ".."

SuggestedRemedy

Change ".." to "."

Response Response Status C

ACCEPT.
 See suggested remedy

CI 85 SC 85.10.8 P266 L41 # 24
 Anslow, Peter Nortel Networks

Comment Type E Comment Status A

This says:
 "where
 IL) IL denotes the value..."

SuggestedRemedy

change "IL) IL denotes the value..." to " IL is the value..."

Response Response Status C

ACCEPT.
 See suggested remedy

CI 85 SC 85.8.3.6 P256 L48 # 25
 Anslow, Peter Nortel Networks

Comment Type E Comment Status A

Some of the equations in Clause 85 introduce an extra variable name that is not used elsewhere.

For example Equation 85-16 starts:

$IL_{tf}(f) \leq IL_{tfmax}(f) = (0.054)...$

The $IL_{tfmax}(f)$ variable is not referred to anywhere in the draft and only serves to complicate the equation.

Where there are limit lines for both max and min for the same parameter (e.g., Equations 85-23 and 85-24) and the extra variables e.g. $ILD_{min}(f)$ and $ILD_{max}(f)$ are used elsewhere, they should be retained.

Also applies to Equations 85-35, 85A-3 and 85A-4

SuggestedRemedy

In 85-16 change " $IL_{tf}(f) \leq IL_{tfmax}(f) = (0.054)...$ " to " $IL_{tf}(f) \leq (0.054)...$ "

In 85-35 change " $IL_{CATF}(f) \leq IL_{catfmax}(f) = (0.029)...$ " to " $IL_{CATF}(f) \leq (0.029)...$ "

In 85A-3 change " $IL_{Ch}(f) \leq IL_{Chmax}(f) = IL...$ " to " $IL_{Ch}(f) \leq IL...$ "

In 85A-4 change " $IL_{Ch}(f) \leq IL_{Chmax}(f) = (0.05)...$ " to " $IL_{Ch}(f) \leq (0.05)...$ "

Response Response Status C

ACCEPT.
 See suggested remedy

CI 85 SC 85.2 P240 L44 # 26
 Anslow, Peter Nortel Networks

Comment Type E Comment Status A

Several references in Clause 85 that should be cross-references are not.

SuggestedRemedy

Make the following references to other places in the draft cross-references.

Page 240, line 44, "80.3"
 Page 244, line 20, "85.10"
 Page 246, line 39, "85.7.4"
 Page 247, line 45, "45.2.1.7.4" (not blue)
 Page 247, line 53, "45.2.1.7.5" (not blue)
 Page 251, line 27, "85.7.12"
 Page 252, line 3, "83.5.10" (not blue)
 Page 252, line 34, "83.5.10"
 Page 253, line 42, "85.7.3.2.3"
 Page 267, line 28, "85.10"

Response Response Status C

ACCEPT.
 See suggested remedy

CI 85 SC 85.9 P259 L33 # 27
 Anslow, Peter Nortel Networks

Comment Type E Comment Status A
 spurious "."

SuggestedRemedy

Change "through.85A.7" to "through 85A.7"

Response Response Status C
 ACCEPT.
 See suggested remedy

CI 85 SC 85.12 P277 L46 # 28
 Anslow, Peter Nortel Networks

Comment Type E Comment Status A
 References to clauses not in the draft should be blue

SuggestedRemedy

Page 277, line 46, "14.7" should be blue
 Page 278, line 11, "Clause 21" should be blue
 Page 278, line 44, "Clause 21" should be blue

Response Response Status C
 ACCEPT.
 See suggested remedy

CI 85A SC 85A.5 P423 L15 # 29
 Anslow, Peter Nortel Networks

Comment Type E Comment Status A
 For equations 85A-3, 85A-4 and 85A-5 the phrase "is the frequency in MHz" is shown in italic font. This should be normal font.

SuggestedRemedy

For equations 85A-3, 85A-4 and 85A-5 change the phrase "is the frequency in MHz" to normal font.

Response Response Status C
 ACCEPT.
 See comment#58

CI 85A SC 85A.5 P423 L24 # 30
 Anslow, Peter Nortel Networks

Comment Type T Comment Status A
 Equation 85A-4 starts with a spurious "(" and the second "x" should be "+"

SuggestedRemedy

Change "(ILCh(f)" to "ILCh(f)"
 Change "(0.05 x ILCamax(f)) x (2 x ILHost(f))" to "0.05ILCamax(f) + 2ILHost(f)"

Response Response Status C
 ACCEPT IN PRINCIPLE.
 See response to comment#171

CI 85A SC 85A.4 P422 L51 # 31
 Anslow, Peter Nortel Networks

Comment Type T Comment Status A
 Equation 85A-2 starts:
 "ILPCB(f) <= ILPCBmin(f) = (0.103)..." but ILPCB(f) should be greater than ILPCBmin(f) not less than.

SuggestedRemedy

change "ILPCB(f) <= ILPCBmin(f) = (0.103)..." to "ILPCB(f) >= ILPCBmin(f) = (0.103)..."

Response Response Status C
 ACCEPT.
 See suggested remedy.

CI 85A SC 85A-4 P422 L46 # 32
 Anslow, Peter Nortel Networks

Comment Type E Comment Status A
 "(i.e., the maximum insertion loss between TP0-TP1 and TP4-TP5)" is unclear and does not conform with the style manual.

SuggestedRemedy

Change "(i.e., the maximum insertion loss between TP0-TP1 and TP4-TP5)"
 to
 "(i.e., the maximum insertion loss between TP0 and TP1 and between TP4 and TP5)"

Response Response Status C
 ACCEPT IN PRINCIPLE.
 See response comment#168.

Cl 86 SC 86.5.4 P290 L42 # 33
 Anslow, Peter Nortel Networks

Comment Type T Comment Status A

Table 86-5 requires SIGNAL_DETECT to be OK when:
 "Optical power at TP3 >= stressed receiver sensitivity (max) in OMA in Table 86.8" This is -5.4 dBm (OMA).
 However, in Table 86-7 "Characteristics of signal within, and at the receiving end of, a compliant optical channel" we see that the OMA, each lane can be -7.9 dBm.
 Consequently, a fully compliant link can have SIGNAL_DETECT = FAIL

SuggestedRemedy

In Table 86-5 change:
 "Optical power at TP3 >= stressed receiver sensitivity (max) in OMA in Table 86.8"
 to
 "Optical power at TP3 >= Optical Modulation Amplitude (OMA), each lane in Table 86.7"

Response Response Status C

ACCEPT IN PRINCIPLE.
 In Table 86-5 change:
 "Optical power at TP3 >= stressed receiver sensitivity (max) in OMA in Table 86.8"
 to
 "Optical power at TP3 >= Minimum OMA, each lane, in Table 86.7"

Cl 86 SC 86.8.4.6.1 P300 L49 # 34
 Anslow, Peter Nortel Networks

Comment Type E Comment Status A

This says "an ideal 4th order Bessel Thompson response". However all other occurrences use "fourth" rather than "4th" and the style manual also states that "In general text, isolated numbers less than 10 should be spelled out."

SuggestedRemedy

Change "an ideal 4th order" to "an ideal fourth order"

Response Response Status C

ACCEPT IN PRINCIPLE.
 Change "an ideal 4th order Bessel Thompson" to "an ideal fourth-order Bessel-Thomson"

 Also in 88.8.8 change "Thompson" to "Thomson"

Cl 86A SC 86A.4.1.1 P428 L52 # 35
 Anslow, Peter Nortel Networks

Comment Type E Comment Status A

In the equations of clause 86A, the phrase "f is the frequency in gigahertz" is used. In the rest of the draft (27 instances) this is "f is the frequency in GHz".
 In the base document the words "gigahertz", "megahertz" or "kilohertz" do not occur at all.

SuggestedRemedy

Change "gigahertz" to "GHz" throughout clause 86A (14 instances)

Response Response Status C

ACCEPT.

Cl 85 SC 85.11.1.1.1 P274 L3 # 36
 Moeller, Merrick Cinch Connectors Inc.

Comment Type T Comment Status A

Referencing Table 85-12.
 Style-1 contact 27 is designated to state 1 for copper module presence. This contact is defined in SFF-8436 as ModPrsL, and fixed to state 0 for passive copper assemblies.
 Contact 28 is defined as IntL, which is a don't care state for passive interconnects, but may be used in other instances.

SuggestedRemedy

Remove Table and text. Use management protocol based on SFF-8436.

Response Response Status C

ACCEPT IN PRINCIPLE. [Editor's Note: Commenter submitted a TR comment. Changed to comment type: T since the commenter is not in P802.3ba ballot group]See response comment#2.

Cl 82 SC 82.1.1 P165 L11 # 37
 Mark, Gustlin Cisco

Comment Type T Comment Status A

Avoid listing of PMDs in the PCS clause that will create a maintenance issue in future. So rephrase sentence as suggested.

SuggestedRemedy

The 40GBASE-R PMA(s) can support any of the 40 Gb/s PMD as specified in Table 80-1. Change:

"The 40GBASE-R PCS is a sublayer of the following Physical Layers: 40GBASE-SR4, 40GBASE-LR4, 40GBASE-CR4 and 40GBASE-KR4. The 100GBASE-R PCS is a sublayer of the following Physical Layers: 100GBASE-SR10, 100GBASE-LR4, 100GBASE-ER4 and 100GBASE-CR10."

To:

"The 40GBASE-R PCS is a sublayer of the 40 Gb/s PHYs listed in Table 80-1. The 100GBASE-R PCS is a sublayer of the 100 Gb/s PHYs listed in Table 80-1."

Response Response Status C

ACCEPT.

Cl 00 SC 0 P13 L0 # 38
 Mark, Gustlin Cisco

Comment Type E Comment Status A

The header is not consistent with respect to having a space between the number and unit. Starting on this page there is not space, but there should be a space.

SuggestedRemedy

Change:

IEEE 802.3ba 40Gb/s and 100Gb/s Ethernet Task Force

To:

IEEE 802.3ba 40 Gb/s and 100 Gb/s Ethernet Task Force

Response Response Status C

ACCEPT IN PRINCIPLE.

Change:"IEEE 802.3ba 40 Gb/s and 100 Gb/s Ethernet Task Force"

To: "IEEE 802.3ba 40Gb/s and 100Gb/s Ethernet Task Force"

where not consistent.

Cl 00 SC 0 P L # 39
 Mark, Gustlin Cisco

Comment Type TR Comment Status A

The CR4/10 Host IL (85-14) and the nPPI recommended electrical channel (86A-19) both defined with connector and test fixtures) should be IDENTICAL also for low frequencies (see page 4 of mazzini_01_0909).

SuggestedRemedy

Harmonize the curves as above.

Response Response Status W

ACCEPT IN PRINCIPLE.

Change equation (85-14)

From:

$$0.114+0.8914 \times \sqrt{f}+0.846 \times f \quad 0.05 = f < 7$$

$$- 35.91 + 6.3291 \times f \quad 7 = f < 8$$

$$14.72 \quad 8 = f = 10$$

To:

$$0.682 \quad 0.05 = f < 0.2$$

$$0.114+0.8914 \times \sqrt{f}+0.846 \times f \quad 0.2 = f < 7$$

$$- 35.91 + 6.3291 \times f \quad 7 = f < 8$$

$$14.72 \quad 8 = f = 10$$

Cl 00 SC 0 P L # 40
 Mark, Gustlin Cisco

Comment Type TR Comment Status D

The recommended maximum loss for the PCB only (without connector) (Draft 2.2, page 446, row 51), should be aligned with formula 85A-2 (Transmitter and receiver differential printed circuit board trace loss) that gives maximum PCB loss @5.156GHz = 3.5dB (see page 4 of mazzini_01_0909).

SuggestedRemedy

Harmonize the loss.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Harmonize the PCB only (without connector) loss between Annex 85A and Annex 86A.

Introduce additional text in to 85A saying that alternative loss allocations are allowed

CI 00 SC 0 P L # 41
 Mark, Gustlin Cisco

Comment Type TR Comment Status A

The cable assembly test fixture (85-35) and the MCB (86A-5) loss formulas must be IDENTICAL. In D2.2 losses just cross at same value @ 5.165GHz (see page 5 of mazzini_01_0909).

SuggestedRemedy

Harmonize the loss.

Response Response Status C

ACCEPT IN PRINCIPLE.

See response to comment #43

CI 00 SC 0 P L # 42
 Mark, Gustlin Cisco

Comment Type TR Comment Status A

The test fixture (85-16) and the HCB (86A-4) loss formulas must be IDENTICAL. In D2.2 losses just cross at same value @ 5.165GHz. (see page 5 of mazzini_01_0909).

SuggestedRemedy

Harmonize the loss.

Response Response Status C

ACCEPT IN PRINCIPLE.

See response to comment #43

CI 85 SC 85.10.10.1 P266 L48 # 43
 Mark, Gustlin Cisco

Comment Type TR Comment Status A

The connector loss (calculated as 85-37 values minus 85-35 and 85-16) of the test fixture improves when frequency increase (see slide 5). Above formulas should be corrected to avoid this.

SuggestedRemedy

As above.

Response Response Status W

ACCEPT IN PRINCIPLE.

Replace: Test fixture insertion loss equation (85-16).
 With: equation (86A-4) using frequency range of 0.05 GHz to 10 GHz.

Also Replace: Cable assembly test fixture equation (85-35).
 With: equation (86A-5) using frequency range of 0.05 GHz to 10 GHz.

CI 86A SC 86A.6 P444 L37 # 44
 Mark, Gustlin Cisco

Comment Type TR Comment Status A

Formula 86A-19 seems incorrect from in the range from 0.2 to 7GHz, should be = -0.114-0.8914*f-0.846*f

SuggestedRemedy

Change the + to a -.

Response Response Status C

ACCEPT.

Note: Comment 15 has changed the sign of this equation.
 see also comments 68, and 232

Cl 83 SC 5.10 P211 L27 # 45
 Szczepanek, Andre HSZ Consulting Ltd

Comment Type TR Comment Status A

There is no limit to the potential increment rate of the PRBS31 checker referenced in 49.2.12.

The checker implementation is difficult to match at high increment rates or in the presence of burst errors (the source synchronous descrambler implementation error multiplication factor depends on burst pattern).

There will be less scope for a complex implementation in a PMA device versus a PCS.

For most practical purposes stringent matching of the 49.2.12 implementation is not necessary. It would be sufficient to match the result of a 49.2.12 implementation only for isolated single bit errors and at errors rates less than 1 in a thousand.

SuggestedRemedy

Replace:
 (see 49.2.12)

With:

The PRBS31 checker shall match the results of the checker implementation in 49.1.12 for isolated single bit errors and at errors rates less than 1 in a thousand.

There will be a contribution at the September interim to support this comment

Response Response Status C

ACCEPT IN PRINCIPLE. [Editor's Note: Commenter did not indicate comment type. Assigned comment Type TR]

Replace:
 (see 49.2.12)

With:

The checker shall increment the test pattern error counter by one for each incoming bit error in the PRBS31 pattern (see 49.2.8) for isolated single bit errors. Implementations should be capable of counting at least one error whenever one or more errors occur in a sliding 1000 bit window.

Cl 87 SC 87.8.11.2 P329 L1 # 46
 Szczepanek, Andre HSZ Consulting Ltd

Comment Type TR Comment Status R

" With the sinusoidal interference and sinusoidal jitter turned off, greater than two thirds of the dB value of the VECP should be created by the selection of the appropriate bandwidth for the fourth-order Bessel-Thomson filter."

Provide a range rather than a limit for the Bessel-Thomson Filter contribution

SuggestedRemedy

Change to :

" With the sinusoidal interference and sinusoidal jitter turned off, between 0.6 and 0.7 of the dB value of the VECP should be created by the selection of the appropriate bandwidth for the fourth-order Bessel-Thomson filter."

There will be a contribution at the September interim to support this comment

Response Response Status C

REJECT.

[Editor's note: Subclause changed from 8.11.1 to 87.8.11.2. Commenter did not indicate comment type. Assigned comment Type TR]

This text is drawn from clause 52 and includes a range of 0.667 to 1.0 of the VECP. The proposed changes restrict the range and is an unnecessary constraint on test equipment manufacturers.

Cl 87 SC 87.8.11.2 P329 L16 # 47
 Szczepanek, Andre HSZ Consulting Ltd

Comment Type ER Comment Status A

" The sinusoidal jitter added should result in at least 0.05 UI peak to peak DCD."

This is the only indication of a minimum DCD requirement in the draft and is not normative anyway. This sentence is redundant and should be removed.

SuggestedRemedy

Remove the sentence.

Response Response Status C

ACCEPT IN PRINCIPLE.

[Editor's note Subclause changed from 8.11.1 to 87.8.11.2]

Many requirements are contained at only one place in the draft.

To be discussed by the Task Force.

Change "The sinusoidal jitter added should result in at least 0.05 UI peak to peak DCD." to "The sinusoidal jitter added should result in at least 0.05 UI of duty cycle distortion (DCD)."

Cl 87 SC 87.8.11.1 P326 L41 # 48
 Szczepanek, Andre HSZ Consulting Ltd

Comment Type TR Comment Status R

"The sinusoidal amplitude interferer may be set at any frequency between 100 MHz and 2 GHz"

Providing such a wide range of frequency (in addition to amplitude) makes compliance testing difficult.

SuggestedRemedy

Select a single sinusoidal amplitude interferer frequency of 1GHz.

There will be a contribution at the September interim to support this comment

Response Response Status C

REJECT.

[Editor's note Subclause changed from 8.11.1 to 87.8.11.1]

The added sinusoidal jitter frequency is constrained to be at least a factor of ten higher than the loop bandwidth of the receiver CDR used, making it a specific frequency is an unnecessary constraint on test equipment manufacturers. This variation is the same as was used in subclause 52.9.9.1.

Cl 87 SC 87.8.11 P326 L15 # 49
 Szczepanek, Andre HSZ Consulting Ltd

Comment Type TR Comment Status R

" Stressed receiver sensitivity shall be within the limits given in Table 87-8 for 40GBASE-LR4 if measured using the method described in 87.8.11.1 and 87.8.11.5 with the conformance test signal at TP3 as described in 87.8.11.2.."

Stressed receiver sensitivity compliance is a normative requirement, but the test setup has a number of variable parameters : BT filter parameters, sinusoidal jitter frequency, sinusoidal amplitude interferer frequency and amplitude, etc.

Given the wide range of alternative configurations that could meet the stressed eye VECF and SEJ values, is it the intention of the committee that all such test setups be tested against the Stressed receiver sensitivity requirement ?

i.e. In order to be compliant is it sufficient to demonstrate compliance at just one such configuration, or does failure at any such configuration mean an implementation is non-compliant.

I see hazards in either position.

A single pass might allow an implementation to select a set of parameters particularly favorable in order to pass.

Conversely demonstrating that there is no single combination of parameters that does not cause a failure would cause testing to take an impracticable amount of time.

SuggestedRemedy

Add some text indicating the committees intention.

There will be a contribution at the September interim to support this comment

Response Response Status C

REJECT.

[Editor's note Subclause changed from 8.11.1 to 87.8.11]

If all such test setups needed to be tested against the Stressed receiver sensitivity requirement, then the test definition would say so.

With any of the tests defined in the draft there is the possibility that one arrangement for measurement may pass a device while another fails it.

The stressed signal for SRS testing is tightly constrained: the calibration reference receiver filter parameters are exact, and the results of sinusoidal amplitude and jitter interferers is precisely defined.

Cl 85 SC 85.8.3.2 P250 L 29 # 50
Healey, Adam LSI Corporation

Comment Type T Comment Status A

It is more appropriate to define RMSIdev as the square-root of the sum of the square values σ_{l^2} and 2^2 . Similarly for the RMSHdev.

SuggestedRemedy

Update Equations (85-2) and (85-3) accordingly. The far-end transmit output noise requirements may need to be updated accordingly.

Response Response Status C

ACCEPT IN PRINCIPLE. Define RMSIdev as the square-root of the sum of the square values σ_{l^2} and 2^2 in equation (85-2). Define RMSHdev as the square-root of the sum of the square values σ_{h^2} and 1^2 in equation (85-3).

Cl 85 SC 85.8.3.3 P251 L 36 # 51
Healey, Adam LSI Corporation

Comment Type TR Comment Status A

The transmitter output waveform requirements do not address the case where the transmitter is requested to INITIALIZE per 72.6.10.4.2.

SuggestedRemedy

Insert a new subclause under 85.8.3.3 with the heading "85.8.3.3.X Coefficient initialization" and containing the following text:

"When the PMD enters the INITIALIZE state of the Training state diagram (Figure 72-5) or receives a valid request to "initialize" from the link partner, the coefficients of the transmit equalizer shall be configured such that the ratio $(c(0)+c(1)-c(-1))/(c(0)+c(1)+c(-1))$ is 1.29 +/- 10% and the ratio $(c(0)+c(1)-c(-1))/(c(0)+c(1)+c(-1))$ is 2.57 +/- 10%. These requirements apply upon the assertion a coefficient status report of "updated" for all coefficients."

Response Response Status W

ACCEPT.
See suggested remedy.

Cl 85 SC 85.8.3.3 P251 L 47 # 52
Healey, Adam LSI Corporation

Comment Type TR Comment Status A

Correct the mapping from q_i to the normalized coefficients $c(n)$ by replace all instances of "Dw" with "Dp".

SuggestedRemedy

"... $c(-1)$ is the value of q_i at time $t_0+(Dp-1)$ UI."
"... $c(0)$ is the value of q_i at time t_0+Dp UI."
"... $c(1)$ is the value of q_i at time $t_0+(Dp+1)$ UI."

Response Response Status W

ACCEPT.
See suggested remedy.

Cl 85 SC 85.8.3.3.5 P254 L 46 # 53
Healey, Adam LSI Corporation

Comment Type TR Comment Status A

Definitions of P2 and P3 are not correct.

SuggestedRemedy

Transpose P2 in Equation (85-11) and, in the following paragraph, define P3 to be the first Nw columns of P2.

Response Response Status W

ACCEPT.
See suggested remedy.

Cl 00 SC 0 P1 L 1 # 54
Healey, Adam LSI Corporation

Comment Type E Comment Status A

In relation to the presentation of equations in the draft, consult the IEEE style guide 17.3 for instructions on the use of italic and upright text in mathematical expressions.

SuggestedRemedy

Update equations to be consistent with the format prescribed by the style guide.

Response Response Status C

ACCEPT.
Editors will review this issue for their clauses in coordination with each other.
See related comment #13

Cl 85 SC 85.10.8 P265 L40 # 55
Healey, Adam LSI Corporation

Comment Type TR Comment Status A

Equations (85-29) and (85-30) are in error. The expression "sinc² x (f/fn)" should be "(sinc(f/fn))²" in both cases.

SuggestedRemedy

Remove the superfluous "x" in both equations.

Response Response Status W

ACCEPT.
See suggested remedy.

Cl 85A SC 85A.5 P421 L4 # 56
Healey, Adam LSI Corporation

Comment Type T Comment Status A

The specified frequency range for channel insertion loss is inconsistent with the frequency range for cable assembly insertion loss in 85.10.2. It seems that they should be consistent.

This should also apply to the transmitter and receiver differential printed circuit board trace loss in 85A.4 and the channel insertion loss deviation in 85A.7.

SuggestedRemedy

Recommend using a consistent frequency range throughout.

Response Response Status C

ACCEPT IN PRINCIPLE.
Specify the transmitter and receiver differential printed circuit board trace loss equations (85A-1) and (85A-2) from 50 MHz to 7500 MHz.

Specify the maximum channel insertion loss equation (85A-3) from 50 MHz to 7500 MHz.

Cl 85A SC 85A.8 P422 L9 # 57
Healey, Adam LSI Corporation

Comment Type T Comment Status A

For the cable assembly, specifications for insertion loss to crosstalk ratio were replaced with integrated crosstalk noise requirements. It seems that the channel requirements should follow suit.

SuggestedRemedy

Refer to healey_01_0909.pdf for proposed text for channel integrated crosstalk noise recommendations.

Response Response Status C

ACCEPT.

See healey_01_0909.pdf for comment response.

Cl 85A SC 85A.5 P421 L14 # 58
Healey, Adam LSI Corporation

Comment Type E Comment Status A

"is the frequency in MHz" should not be italicized.

SuggestedRemedy

Correct two occurrences in this subclause, as well as an occurrence in 85A.7.

Response Response Status C

ACCEPT.
See suggested remedy

Cl 85 SC 85.10.5 P262 L38 # 59
Healey, Adam LSI Corporation

Comment Type TR Comment Status A

MDNEXTloss is defined to be computed over that range of 50 to 6000 MHz, but the calculation that uses this quantity, integrated crosstalk noise (85.10.8), requires values from 50 to 10000 MHz.

SuggestedRemedy

Correct the frequency range to be consistent with 85.10.8. Also correct the frequency range in 85.10.6 (MDFEXTloss).

Response Response Status W

ACCEPT.
See suggested remedy.

CI 85 SC 85.10.7 P263 L14 # 60
Healey, Adam LSI Corporation

Comment Type T Comment Status A

There are no requirements on PSXT(f) and it is not used as a parameter in any of the cable assembly specifications.

SuggestedRemedy
Remove 85.10.7.

Response Response Status C
ACCEPT.

CI 83 SC 83.1.4 P205 L49 # 61
Dawe, Piers Independent

Comment Type E Comment Status A
Gbaud

SuggestedRemedy
GBd (twice)

Response Response Status C
ACCEPT.

CI 87 SC 87.8.11.3 P329 L31 # 62
Dawe, Piers Independent

Comment Type E Comment Status A

Elsewhere in 802.3 where a Bessel-Thomson response for measurement (scope or reference receiver) is specified, it isn't called "3 dB upper electrical cutoff frequency" but "bandwidth" or "reference frequency fr" or simply "7.5 GHz Bessel-Thomson".

SuggestedRemedy

Please change "3 dB upper electrical cutoff frequency" to "reference frequency fr", or change "ideal fourth-order Bessel-Thomson response with a 3 dB upper electrical cutoff frequency of * GHz." to "ideal * GHz fourth-order Bessel-Thomson response", or "ideal fourth-order Bessel-Thomson response with a bandwidth of * GHz."
But please don't try to change "response" to "loss"!

Response Response Status C

ACCEPT IN PRINCIPLE.
Change "fourth-order Bessel-Thomson response with a 3 dB upper electrical cutoff frequency of" to "fourth-order Bessel-Thomson response with a reference frequency fr of"

CI 86A SC 86A.1 P427 L6 # 63
Dawe, Piers Independent

Comment Type ER Comment Status R

In D2.2, "Parallel Physical Interface" is abbreviated to nPPI. As we have decided not to use nAUI in the document, this would be the only such nSomething abbreviation in 802.3. The word "Parallel" implies multiple lanes so "n" has no purpose any more. Other multi-lane things e.g. PMD types put the multiple number at the end not the beginning.

SuggestedRemedy
Change "nPPI" to "PPI" throughout.

Response Response Status W
REJECT.

This term was inserted in response to comment 537 against draft 2.0. The n represents "C" or "XL" which describes the rate of operation supported by the interface and not the number of lanes.

CI 85 SC 85.10.10.3 P270 L32 # 64
Dawe, Piers Independent

Comment Type ER Comment Status A

Apparently, variable names in equations are not allowed to contain spaces. I suppose this is because to a mathematician "NEXT loss" means "NEXT" multiplied by "loss".

SuggestedRemedy
My preferred solution is change "NEXT loss" to "NEXT" and flip the sign.

Response Response Status W
ACCEPT IN PRINCIPLE.
Follow style guide; if space is to be removed then>

Change: NEXT loss
To: NEXT with subscripted loss

Cl 85 SC 85.10.10.3 P270 L48 # 65
Dawe, Piers Independent

Comment Type ER Comment Status R

Draft says "MDNEXT loss is specified as the power sum of the individual NEXT losses." This is not correct. MDNEXT is the power sum of the individual NEXTs, but "MDNEXT loss" is the inverse of the power sum of the individual inverses of "NEXT losses".

SuggestedRemedy

My preferred solution is change "NEXT loss" to "NEXT" and "MDNEXT loss" to "MDNEXT", and flip the signs.

Response Response Status W

REJECT.

Multiple disturber power sum near-end crosstalk calculation and associated description in (85-26) is used in base document e.g., 802.3an..10GBASE-T..

Cl 86A SC 86A.5.1.1.2 P434 L33 # 66
Dawe, Piers Independent

Comment Type T Comment Status A

While adjusting the cosmetics of equation 86A-7, a sign error has crept in.

SuggestedRemedy

Change +0.861 back to -0.861.

Response Response Status C

ACCEPT IN PRINCIPLE.

In equation 86A-7 change "+ 0.861" to "- 0.861"

In equation 86A-8 change "- 28.85" to "+ 28.85"

Note: comment 15 has changed the sign of these equations.

See also comments 44, 68 and 232

Cl 85 SC 85.8.3.7 P256 L48 # 67
Dawe, Piers Independent

Comment Type T Comment Status A

85.8.3.4's "Insertion loss TP0 to TP2 or TP3 to TP5" is (above 200 MHz) consistent with the minimum SDD21 of host PCB, connector and HCB in 86A.6. The mated test fixtures insertion loss limits of 85.10.10.1 are consistent with the through response (SDD21) limits of mated HCB-MCB in 86A.5.1.1.2. Yet the test fixture insertion loss of 85.8.3.7 and the cable assembly test fixture insertion loss of 85.10.9 do not agree with the reference through responses (SDD21) of HCB and MCB in 86A.5.1.1.1. 85.8.3.7 and 85.10.9 use scaled backplane Amax while 86A.5.1.1.1 is based on experience with actual compliance boards. Because compliance boards are not backplanes (e.g. may use PTFE dielectric rather than FR4), the equations in 86A.5.1.1.1 are preferable.

SuggestedRemedy

Change equations 85-16 and 85-35 so they are consistent with 86A-4 and 86A-5 respectively.

Response Response Status C

ACCEPT IN PRINCIPLE.

See response to comment #43.

Cl 86A SC 86A.6 P446 L37 # 68
Dawe, Piers Independent

Comment Type T Comment Status A

Sign error in equation 86A-19. It should be a scaled version of D2.1 86A-20.

SuggestedRemedy

Change + 0.846f to - 0.846f.

Response Response Status C

ACCEPT IN PRINCIPLE.

see comment 44 and 232

Cl 82 SC 82.2.1 P171 L 22 # 69
Dawe, Piers Independent

Comment Type T Comment Status R

Clarifying D2.1 comment 32:

There are two error counting mechanisms that can be used on 64B/66B signals: errored blocks and BIP errors. For isolated errors at error rates of interest, they will give near-identical results. But if burst errors are involved, the errored block counter will typically count 1 per burst while the BIP error counters will typically count the number of errors in the burst.

We should be unambiguous which is meant by BER for the purposes of compliance. As the errored block counter is not very good in service at good BERs, we expect in-service monitoring to use BIP (that's why it was introduced). It is HIGHLY desirable that the same definition of BER apply in compliance testing with the scrambled idle signal as in service. Also, as MTTFPA is so important and burst errors are a threat to it, BIP counting is preferable for another reason.

The response to D2.1 comment 32 points out that BIP counting saturates too low for the current hi_ber threshold. So continue with block counting (as is) for the BER monitor state diagram, but...

SuggestedRemedy

Say that BER for 64B/66B signals (including the scrambled idle signal) is defined by BIP error counting (rather than by the BER monitor state diagram). Although the count from the BER monitor state diagram may be useful for diagnostics at very bad BER.

Response Response Status C

REJECT.

The proposal is not a complete solution and is proposing a significant change to the PCS test pattern operation.

Cl 83 SC 83.5.10 P215 L 40 # 70
Dawe, Piers Independent

Comment Type T Comment Status A

Piling on to D2.1 comment 253. What is in the draft seems so impractical and unnecessarily power-hungry that it won't be obeyed fully. Draft refers to 49.2.12 which says "The test-pattern error counter shall increment once for each bit time that the PRBS31 pattern error signal is high." which could approach the lane line rate. Unlike the assertion in the response to comment 34, choosing an implementation dependent limitation would seem not to be allowed. For comparison, even a lab BERT saturates or drops sync at some point e.g. 10^{-3} or 10^{-2} .

SuggestedRemedy

If you want to stay with the checker of 49.2.12 then write down that a .3ba version need not count error ratios above $1e-3$ accurately. This will ease both the high-speed analog silicon and also the management counters.

Also, it might be desirable to define a maximum reported error rate so that the management software doesn't have to be designed to cope with ridiculous BERs. (Per response to D2.1 comment 32, the high BER state machine kicks in at a 10^{-4} BER, so anything much above that is hopelessly bad and we don't need an exact measurement of it.)

Also, it may ease the implementation to write down that a .3ba version need not count burst errors precisely as 49.2.12 (which isn't accurate for all bursts, anyway).

Response Response Status C

ACCEPT IN PRINCIPLE.

See response to comment 45.

Cl 83 SC 83.5.10 P215 L 24 # 71
Dawe, Piers Independent

Comment Type T Comment Status A

Draft says "There shall be at least 31 bits delay between the PRBS31 patterns generated on one lane and any other lane.". Elsewhere, Skew and delay specs are in BT (and PQ and ns). This "31 bits" is misleading.

SuggestedRemedy

Change "bits" to "UI".

Response Response Status C

ACCEPT IN PRINCIPLE.

Overtaken by events. See comment #75.

CI 86A SC 86A.4.1 P428 L21 # 72
Dawe, Piers Independent

Comment Type T Comment Status A

If Table 86A-3, nPPI module electrical output specifications at TP4, has a termination mismatch spec, why doesn't Table 86A-1, nPPI host electrical output specifications at TP1a? I don't believe that a 1 MHz measurement will be affected by the few inches of PCB trace in the host, as was alleged.

SuggestedRemedy

Add row, Termination mismatch at 1 MHz, max 5%.

Response Response Status C

ACCEPT.

CI 86A SC 86A.4.2 P431 L21 # 73
Dawe, Piers Independent

Comment Type T Comment Status A

Transition time is given as 34 ps TBC.

SuggestedRemedy

Confirm it or change it to a better number. Delete "TBC".

Response Response Status C

ACCEPT IN PRINCIPLE.
Delete "TBC"

CI 86A SC 86A.5.1.1.2 P434 L44 # 74
Dawe, Piers Independent

Comment Type T Comment Status A

Do we have measurements on QSFP and CXP mated HCB-MCB reflection response?

SuggestedRemedy

If appropriate, update equations 86A-8 and Figure 86A-4 in line with measurements.

Response Response Status C

ACCEPT IN PRINCIPLE.

Replace crosstalk limits of equations 86A-11 through 86A-14 and associated text and Figure 86A-6 with a requirement that the ICN limits of 85.10.10.3 must be met.

See also comment 114.

CI 83 SC 83.5.10 P215 L24 # 75
Dawe, Piers Independent

Comment Type T Comment Status A

Draft says "There shall be at least 31 bits delay between the PRBS31 patterns generated on one lane and any other lane.". This was to stop the lanes being highly correlated and hence the lane-to-lane crosstalk being unrealistic. However, Skew Variation, not necessarily in the generating PMA, could reduce these relative delays.

SuggestedRemedy

Increase 31 by the appropriate Skew Variation or say "a delay of 31 UI plus the allowance for Skew Variation for the downstream sublayers as given in Table 80-5." But see another comment.

Response Response Status C

ACCEPT IN PRINCIPLE.

Replace:

"There shall be at least 31 bits delay between the PRBS31 patterns generated on one lane and any other lane."

with:

"To avoid correlated crosstalk, it is highly recommended that the PRBS31 patterns generated on each lane be generated from independent, random seeds or at a minimum offset of 1000 UI between the PRBS31 sequence on any lane and any other lane."

CI 87 SC 87.8.11.3 P329 L31 # 76
Dawe, Piers Independent

Comment Type TR Comment Status A

All but two 10G Ethernet Bessel-Thomson responses for measurement (even the one in 87.8.9) have a bandwidth / reference frequency $f_r / 3$ dB upper electrical cutoff frequency of 7.5 GHz. 86.8.4.4 has 6.2 GHz for a reason. Here we have 7.73 GHz. Implementers are going to use the same 10G instruments for 40GBASE-LR4 as for 10GBASE-L and 10GEPON, so this difference, between 7.5 and 7.73, is not practical.

SuggestedRemedy

Change 7.73 to 7.5.

Response Response Status W

ACCEPT.

Cl 87 SC 87.8.11.2 P328 L8 # 77
 Dawe, Piers Independent

Comment Type TR Comment Status A

87.8.11.2 has a definition of VECP that contradicts the rest of 802.3. Detail follows:
 In 52.9.9.2, VECP is defined as $10 \log(\text{OMA}/\text{AO})$. Applies to 10G, scrambled, including 10GEPON. Also applies in 86.8.4.7.
 In 58.7.11.2, VECP is defined as $10 \log_{10}(\text{AN}/\text{AO})$, where AN is to be measured with a square wave pattern consisting of four to eleven consecutive ones followed by an equal run of zeros. Applies to 100M and 1G, block coded.
 In 53.9.14, VECP is defined as $10 \log(\text{AO}/\text{AN})$ (sign error), where "AN is the normal amplitude without ISI, as measured in Figure 53-12." Applies to 10GBASE-LX4 (3.125 GBd, block coded).
 10GBASE-LRM doesn't use VECP.
 In D2.2 87.8.11.2, VECP is defined as $10 \log(\text{AN}/\text{AO})$, where "AN is the normal amplitude without ISI, as shown in Figure 87-4." but unlike Figure 53-12, Figure 87-4 shows AN as difference of means of histograms at crossing time, which is not exactly OMA nor the "normal amplitude without ISI". (52.9.9.2 says "OMA is the normal amplitude without ISI, as shown in Figure 52-11" but 52.9.5 gives a precise definition.)
 D2.2 88.8.5.1 uses the 52.9.9.2 definition of VECP while 88.8.10 uses 87.8.11.

SuggestedRemedy

Definitions and stressed eye generators will be shared across 40GBASE-LR4, 10GBASE-LR, 10GBASE-ER and 10GEPON, so 87.8.11.2 should conform.
 Change the definition of VECP to $10 \log_{10}(\text{OMA}/\text{AO})$.
 To avoid confusion, modify Figure 87-4 to remove "AN" (which is the "Approximate OMA" of Fig 52-11 and "Approximate AN" of Fig 58-9, and it's not relevant) and remove the histograms at the crossing time.
 If wished, add pointers to illustrate where OMA would be, at the settled one and zero levels (this would be better done with the waveform of Figure 53-12 or 58-9).

Response Response Status W

ACCEPT IN PRINCIPLE.
 In equation 87-1 change " $10 \log(\text{AN}/\text{AO})$ " to " $10 \log(\text{OMA}/\text{AO})$ " and "AN is the normal amplitude without ISI, as shown in Figure 87-4." to "OMA is the optical modulation amplitude as defined in 87.8.5".
 In Figure 87-4 remove AN and related histograms etc.
 In 88.8.5.1 change "as defined in 52.9.9.2 is less than" to "as defined in 87.8.11.2 is less than".

Cl 85 SC 85.8.3.7 P256 L46 # 78
 Dawe, Piers Independent

Comment Type TR Comment Status A

The test fixture insertion losses aren't maxima, they are reference losses. See text at 86A.5.1.1.

SuggestedRemedy

Change "maximum" to "reference" here and in 85.10.9.

Response Response Status W

ACCEPT IN PRINCIPLE.
 See response to comment#167, comment#177.

Cl 83 SC 83.5.10 P215 L 22 # 79
Dawe, Piers Independent

Comment Type TR Comment Status R

Following up on D2.1 comment 33. anslow_05_0709 showed that for two scenarios with an almost-minimum 32 UI delay between lanes, the peak baseline wander was about 50% more than for a single PRBS31. I believe that if the delay is substantially increased, that 50% will substantially reduce. Maybe I'll get the simulation done by the meeting. The larger delay could be generated by choosing appropriate seeds for each lane's PRBS generator and starting the generators together, but that's implementation.

SuggestedRemedy

The first part of the remedy is similar to last time:
Change "on each of the lanes" to "on each of the PCS lanes" here and at line 30.
Change "one lane and any other lane" to "one PCS lane and any other PCS lane"
In the paragraphs beginning line 38 and line 50, change "lane" or "lanes" to "PCS lane" or "PCS lanes".
Delete "Note that bit multiplexing of per-lane PRBS31 may produce a signal which is not meaningful for downstream sublayers."
Provide 20 PRBS31 error counters in each direction, one per PCS lane.
Another solution which would take a few more words would be to generate by 10G lanes and check by 20G PCS lanes, for 100G. Do we have a name for a 10G lane? For 40G, because we have a binary series of lane speeds, generating per lane (whatever that is) and checking per (10G) PCS lane is ideal, but generating by 10G lanes with offset would still work.
Increase the 31 bits (UI) minimum delay between generator lanes to a number TBD, around 2000 UI.

Response Response Status W

REJECT.

D2.1 comment 33 was rejected based on the analysis in anslow_05_0709. The decision should not be reconsidered unless:

- 1) simulation results can be provided to show that larger offsets do not significantly increase the baseline wander over PRBS31;
 - 2) it can be shown that it is not unduly onerous to be required to generate 20 PRBS31 sequences that are offset by 2000 UI; and
 - 3) a specific offset value can be provided which meets the necessary requirements.
- Note that there is no other aspect of the PMA which is aware of PCS lanes and other mechanisms (e.g., scrambled idle test pattern, BIP) are available for multi-sublayer testing.

Cl 83A SC 83A.3.3.4 P387 L 49 # 80
Dawe, Piers Independent

Comment Type TR Comment Status R

As I pointed out in D2.1 comment 35, S-parameters define power gain, not loss. [SCC22] as a ratio must be <1, [SCC22] in dB must be negative. I'm sure our readers can cope with S-parameters and negative numbers.

SuggestedRemedy

Change the signs on the right hand side, change the direction of the inequality back to <= as in D2.1.

Response Response Status W

REJECT.

See comment 151

Cl 85 SC 85.3 P241 L 18 # 81
Dawe, Piers Independent

Comment Type TR Comment Status R

The response to D2.1 comment 37 (Exchange of DME frames is unnecessary) shows a misunderstanding by the BRC. Response says "include backward compatability with CX4". CX4 doesn't use and can't understand DME frames, so compatability with CX4 is achieved by Parallel Detection. Response says "Suggested remedy inconsistent with ... 802.3ap electricals": this isn't about electricals but about a protocol. DME frames are used in Backplane Ethernet where there is a choice of DME-aware PMD types. On a front-side port, there isn't. There is 10GBASE-CX4 and 40GBASE-CR4. You don't need DME frames to tell them apart. You have Parallel Detection to detect CX4. So you can use it to detect CR4 also.

The unnecessary burden, apart from the obvious extra complexity of an unnecessary protocol, is that DME frames run at 312.5 MBd, 1/33 of the normal 10G rate, so a normal 10G CDR won't lock to this.

SuggestedRemedy

Add text in Clause 85 saying that 40GBASE-CR4 and 100GBASE-CR10 can use Parallel Detection. This is in line with the backward compatibility with CX4 and baseline "Parallel detection function to detect legacy 10GBASE-CX4 PHYs".
If you wish, advertise FEC ability in the Training frame.

Response Response Status W

REJECT.

AN uses DME signaling to exchange link partner abilities and to negotiate FEC capability.

The commenter has not provided a sufficiently complete proposal for replacement of DME with parallel detection.

Cl 83A SC 83A.2 P383 L6 # 82
Dawe, Piers Independent

Comment Type TR Comment Status R

Following up D2.1 comment 159, According to 83.3, a PMA has TX and RX directions, each of which has an input and an output. nAUI is intended to connect PMAs, e.g. one in the host and one in a module. Therefore nAUI must connect a (host) TX (transmitter) output to a (module) transmitter input, and a (module) RX (receiver) output to a (host) receiver input. 83B and 86A use the terms host output, module input, module output, host input, which is compatible with 83. But Figure 83A-2 shows two "Transmitter"s and two "Receiver"s, one for each direction. This isn't compatible terminology.

SuggestedRemedy

Change "Transmitter" to "output" or "driver" or "driver output" as appropriate, "Transmit Compliance Point" to "output compliance point", "Receiver" to "input", and "Receiver Compliance Points" and "Receive Compliance Point" to "output compliance point", throughout 83A.

Response Response Status W

REJECT.

See comment 200 for consistency between 83A & 83B

Cl 83A SC 83A.2.1 P383 L25 # 83
Dawe, Piers Independent

Comment Type TR Comment Status A

SDD21 does not represent loss, it represents forward gain ("through response" or just "response"; 47.4.1 calls it "transmission magnitude response"). For modules, we should stay with S-parameters, as is common industry practice in SFP+, CXP, XAUI (Clause 47) and so on, but the names need cleaning up.

SuggestedRemedy

Change "differential insertion loss" to "differential response". Change "less than" to "more than or equal to". Reverse the signs and the inequality in equation 83A-1 and Figure 83A-3.

Response Response Status W

ACCEPT IN PRINCIPLE.

See comment 151.

Cl 83A SC 83A.3.3.1 P386 L8 # 84
Dawe, Piers Independent

Comment Type TR Comment Status R

De-emphasis means a relative attenuation of the higher frequencies, as in "Dolby noise reduction is a form of dynamic preemphasis employed during recording, plus a form of dynamic deemphasis used during playback". So de-emphasis is the opposite of what you want.

SuggestedRemedy

We don't need to argue about de- versus pre-: just change "De-emphasis" to "Emphasis", and "Vtx-demph" (or "Vth-demph") to "VMA", throughout.

Response Response Status W

REJECT.

De-emphasis is an industry standard term.

Cl 85 SC 85.10.10.3 P270 L32 # 85
Dawe, Piers Independent

Comment Type TR Comment Status R

"NEXT loss" sounds wrong. We never expected all the power incident on the pair of test fixtures to appear as crosstalk, so how is it "lost"? It seems to be "lost" several times over, to NEXT, to FEXT, to regular transmission loss, and to reflection. This doesn't make sense. A better term than loss, which is used frequently in 802.3, is attenuation, because it focuses on the signal that's there rather than the signal that's "lost". Of course, it would be much better to specify NEXT (-ve dB) rather than "NEXT loss" or "NEXT attenuation" (you need to the right-way-up NEXT to calculate MDNEXT anyway).

SuggestedRemedy

This is a defensive comment. Whatever you do, don't mess up 86A. It will take a lot of comments in probably more than one meeting cycle to repair the collateral damage.

Response Response Status W

REJECT.

NEXT loss consistent with the use of "loss" for naming other signal impairments e.g., return loss, insertion loss, channel loss..etc..used in clause 85 and other IEEE 802.3 clauses.

See response to comment 15

Cl 85 SC 85.10 P260 L14 # 86
Moore, Charles Avago Technologies

Comment Type T Comment Status A

In table 85-8 Minima for MDNEXT loss, MDFEXT loss and power sum crosstalk loss are listed but the references do not specify either values or equations for minima. This is because these specs have been replaced by Minimum integrated crosstalk noise. These minima are no longer needed.

SuggestedRemedy

Delete unused specs from table 85-8

Response Response Status C

ACCEPT IN PRINCIPLE. [Editor's Note: Commenter did not indicate comment type, assigned Comment Type: T, since the commenter is not part of the P802.3ba ballot group]
Response:
85.10.8 Cable assembly integrated crosstalk noise (ICN) uses MDNEXT and MDFEXT.
Delete minimum Table 85-8 from "minimum MDNEXT" and "minimum FEXT".

Cl 85 SC 85.8.3 P249 L22 # 87
Moore, Charles Avago Technologies

Comment Type E Comment Status A

"Amplitude peak-to-peak" should be "Amplitude peak-to-peak (max)"

SuggestedRemedy

make indicated change

Response Response Status C

ACCEPT IN PRINCIPLE.

See response comment#222.

Cl 85 SC 85.10.2 P262 L10 # 88
Moore, Charles Avago Technologies

Comment Type E Comment Status A

Figure 85-6, 85-7 and others, plot vs log frequency quantities which can be seen more clearly if plotted versus linear frequency

SuggestedRemedy

convert all frequency plots to linear frequency.

Response Response Status C

ACCEPT IN PRINCIPLE.

Use linear scale for: 85-4,85-7,85-12,85-6,85-13,85-14,85-8

Cl 85 SC 85.8.3.4 P255 L9 # 89
Moore, Charles Avago Technologies

Comment Type T Comment Status D

Normative insertion loss spec between TP0 and TP2 and TP3 and TP5 is no longer needed

SuggestedRemedy

Delete 85.8.3.4 including Equation 85-14 and Figure 85-Rely on 85A.4.

In 85A.5, repalce "Equation(85-14)" on line 18 and line 33 to "Equation (85A-1)"

In equation 85A-3 and equation 85A-4, delete term "-(2 x ILMatedTF(f))

or

Move 85.8.3.4 including Equation 85-14 and Figure 85-into annex 85A, most likely 85A.4

If Figure 85-4, use a linear frequency scale.

Proposed Response Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

The 85.8.3.4 Insertion loss basis is tied to supported trace lengths identified in D2.1 comment#96 resolution using gustlin_04_0709.

Cl 85 SC 85.8.3.3 P252 L14 # 90
Moore, Charles Avago Technologies

Comment Type T Comment Status A

pulse amplitude out Tx at TP2 is defined but DC gain is not. This could allow slow, high amplitude Tx, which is hard to equalize, to pass.

SuggestedRemedy

Specify Tx DC amplitude of Tx as "sum of linear fit pulse from step 3 divided by M from step 3" specify that DC amplitude is greater than 0.375 and less than 0.6 and that the peak of the linear fit pulse from step 3 shall be greater than 0.60*DC amplitude

Response Response Status C

ACCEPT IN PRINCIPLE.

Specify Tx DC amplitude of Tx as "sum of linear fit pulse from step 3 divided by M from step 3" specify that DC amplitude is greater than [0.34 v] and less than 0.6 v and that the peak of the linear fit pulse from step 3 shall be greater than [0.63]*DC amplitude.

Editor given license to implement in procedure.

Cl 85 SC 85.8.4.2 P258 L1 # 91
Moore, Charles Avago Technologies

Comment Type T Comment Status A

Receiver interference tolerance test is incomplete.

SuggestedRemedy

Proposed wording will be presented a meeting

Response Response Status C

ACCEPT IN PRINCIPLE.

Replace "85.8.4.2 Receiver interference tolerance test at TP3" with moore_01a_0909.pdf revision to moore_01_0909.pdf.

Cl 85 SC 85.8.3.1 P249 L42 # 92
Ghiasi, Ali Broadcom

Comment Type ER Comment Status A

Special character

SuggestedRemedy

Please remove the special character at end of line

Response Response Status W

ACCEPT.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed U/unsatisfied Z/withdrawn
SORT ORDER: Comment ID

Cl 85 SC 85.8.3.2 P250 L3 # 93
Ghiasi, Ali Broadcom

Comment Type ER Comment Status A

The sentence does not read well "The far-end transmitter output noise is noise in .."

SuggestedRemedy

Suggested "The far-end transmitter output noise is the summ of this noise in .."

Response Response Status W

ACCEPT IN PRINCIPLE.

Replace:"The far-end transmitter output noise is noise in addition to the cable assembly integrated crosstalk noise (ICN)."

With:The far-end transmitter output noise is an additional source of noise to the cable assembly's integrated crosstalk noise (ICN).

Cl 80 SC 80.5 P138 L5 # 94
Ghiasi, Ali Broadcom

Comment Type T Comment Status A

Column heading state maximum skew but the values have approximate symbol-

SuggestedRemedy

Please replace~with max value of skew

Response Response Status C

ACCEPT IN PRINCIPLE. [Editor's note: Please do not use special character "tilde" or approximate symbol in comments since this is used as delimiter by the comment tool] Also see related comment #95

Replace all tilde characters with [approx =] in tables 80-4 and 80-5

In footnotes change "Note that for 40GBASE-R, 1 UI is equal to 96.969697 ps at PCS lane signaling rate of 10.3125 GBd." to "[approx =] indicates approximate equivalent of maximum skew in UI for 40GBASE-R, based on 1 UI equals 96.969697 ps at a PCS lane signaling rate of 10.3125 GBd." and change "Note that for 100GBASE-R, 1 UI is equal to 193.939394 ps at PCS lane signaling rate of 5.15625 GBd." to "[approx =] indicates approximate equivalent of maximum skew in UI for 100GBASE-R, based on 1 UI equals 193.939394 ps at a PCS lane signaling rate of 5.15625 GBd."

Cl **80** SC **80.5** P**140** L**32** # **95**
 Ghiasi, Ali Broadcom

Comment Type **T** Comment Status **A**

Column heading state maximum skew variation but the values have approximate symbol-

SuggestedRemedy

Please replace~with max value of skew variations

Response Response Status **C**

ACCEPT IN PRINCIPLE. [Editor's note: Please do not use special character "tilde" or approximate symbol in comments since this is used as delimiter by the comment tool]

See response to comment #94

Cl **86A** SC **86A.4.2** P**430** L**14** # **96**
 Ghiasi, Ali Broadcom

Comment Type **TR** Comment Status **R**

With current set of specifications the SerDes transmitter may have very large amount of de-emphasis 3-5 dB resulting in signifincat distortion at TP1a and also see comment 216/218 on D2.1

SuggestedRemedy

The options here are either limit max DDJ to about 0.125 or max 3 dB de-emphasis, see ghiasi_03_0909

Response Response Status **U**

REJECT.
 see also response to comment 131

Cl **85A** SC **85A.5** P**423** L**9** # **97**
 Ghiasi, Ali Broadcom

Comment Type **TR** Comment Status **A**

ILmated could have as low as 2 dB loss and as high as 2.8 dB which could result cabling having higher loss

SuggestedRemedy

Add note the cable loss of 24.44 dB is when ILmated loss is 2.4 dB, if ILmated loss is less than 2.4 dB then ILch shall be reduced by the same amount

Response Response Status **W**

ACCEPT IN PRINCIPLE.
 See response comment#170

Cl **85** SC **85.8.3** P**249** L**31** # **98**
 Ghiasi, Ali Broadcom

Comment Type **TR** Comment Status **A**

No test method is defined how to measure "Total Jitter Excluding Data Dependent Jitter"

SuggestedRemedy

A suggested method is given below:
 Total jitter is measured with PRBS31 (pattern 3) at BER of 10-12. Data Dependent jitter is measured with PRBS9 based on method given in 85.8.3 with following definition
 $DDJ = \max(dt1, dt2, \dots, dt256) - \min(dt1, dt2, \dots, dt256)$.
 Section 85.8.3 would need to be updated or the other option is to create a standalone section.

Total Jitter Excluding DDJ = TJ - DDJ

Response Response Status **W**

ACCEPT IN PRINCIPLE. [Editor's note removed mistyped special character from subclause field. Changed to 85.8.3]

Response: Measure Total jitter at BER 1E-12 per 83A.5.1.=TJ

Measure DDJ with PN9=DDJ
 Total Jitter excluding Data Dependent Jitter = TJ - DDJ

Editor given license to implement response incorporating comment#218 in response.

Cl **85** SC **85.8.3.1** P**249** L**40** # **99**
 Ghiasi, Ali Broadcom

Comment Type **TR** Comment Status **D**

Transmitter common mode output return loss is missing

SuggestedRemedy

The reference impedance for common mode return loss measurement shall be 25 ohms

Return loss $\geq -7 + 1.6 * f$ from -.05 to 2.5 GHz
 -3 from 2.5 to 10 GHz

Proposed Response Response Status **Z**

PROPOSED REJECT.

This comment was WITHDRAWN by the commenter.

Common-mode return loss specified;
 see Table 85-4- Common-mode output return loss (min.).

Cl 85 SC 85.8.3.4 P255 L35 # 100
Ghiasi, Ali Broadcom

Comment Type TR Comment Status A

It would more readable if Fig 85-4 is plotted with linear scale and similar to Fig 86A-12

SuggestedRemedy

Please follow or copy Fig 86A-12

Response Response Status C

ACCEPT IN PRINCIPLE.

Change figure 85-4 to linear scale

Cl 85 SC 85.8.3.4 P255 L35 # 101
Ghiasi, Ali Broadcom

Comment Type TR Comment Status R

Figure is missing min loss

SuggestedRemedy

Please add min loss and follow or copy Fig 86A-12

Response Response Status W

REJECT.

The 86A specification for a minimum provides no real benefit as it produces a minimum specification of 0.15 dB extracted connector insertion loss.

Y:7

N:0

A:2

Room attendance:9

Cl 85 SC 85.8.3.7 P256 L48 # 102
Ghiasi, Ali Broadcom

Comment Type TR Comment Status D

It is very difficult to read the graph with log scale

SuggestedRemedy

Please use linear freq scale

Proposed Response Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

No graph on page 256 line 48.

Cl 85A SC 85A.4 P422 L51 # 103
Ghiasi, Ali Broadcom

Comment Type TR Comment Status A

Min loss Eq 85A-2 is not consistent with mated channel loss

SuggestedRemedy

The mated min channel loss =2.08

less min HCB loss= 1.04 dB

Min connector loss= 0.3 dB

Result in 0.74 dB loss per end

Response Response Status C

ACCEPT IN PRINCIPLE.

Change (0.103) to scale equation (85A-2) to $2*(0.67)$ db @ 5.515626 GHz.

Cl 80 SC 80.5 P140 L5 # 104
Ghiasi, Ali Broadcom

Comment Type TR Comment Status A

No test method is defined for measuring skew

SuggestedRemedy

Transmitter lane under test transmits suitably long PRBS pattern with length at least twice as long as the maximum skew and based on the scope capability while other lanes transmit PRBS31.

Transmitter lane under test output is split in to two. One set of output goes to the golden PLL as defined by the specific PMDS to provide triggering to oscilloscope. The second output goes to the to the oscilloscope inputs which can lock to the PRBS pattern. A visible edge is identified for the first lane, the measurement is then repeated for the remaining lanes to determine maximum skew.

Response Response Status W

ACCEPT IN PRINCIPLE.

See response to comment #40

Cl 80 SC 80.5 P140 L31 # 105
Ghiasi, Ali Broadcom

Comment Type TR Comment Status A

No test method is defined for measuring dynamic skew

SuggestedRemedy

Transmitter lane under test transmits suitably long PRBS pattern with length at least twice as long as the maximum skew variation and based on the scope capability while other lanes transmit PRBS31.

Transmitter lane under test output is split in to two. One set of output goes to the golden PLL as defined by the specific PMDS to provide triggering to oscilloscope. The second output goes to the to the oscilloscope inputs which can lock to the PRBS pattern. Skew variation on the first lane is recorded, the measurement is then repeated for the remaining lanes to determine maximum skew variation.

Response Response Status W

ACCEPT IN PRINCIPLE.

At the end of 85.5 add

The measurements of Skew and Skew Variation are defined in 85.5.1 >>>Title 85.5.1 Measurements of Skew and Skew Variation

Skew and Skew Variation are defined in 80.5 and are required to remain within the limits given in 85.5 over the time that the link is in operation. The measurement of Skew and Skew variation is made by acquiring the data on each lane using a clock and data recovery unit with a high frequency corner bandwidth and slope as specified in 86.8.3.2. The arrival times of the one to zero transition of the alignment marker sync bits on each lane are then compared. This arrangement ensures that any high frequency jitter that is present on the signals is not included in the skew measurement.

Cl 85 SC 85.10.10.1 P269 L15 # 106
Ghiasi, Ali Broadcom

Comment Type TR Comment Status A

graph with log scale is not readable

SuggestedRemedy

Please use linear freq scale similar to fig 86A-3

Response Response Status C

ACCEPT IN PRINCIPLE. For Figure 85-12 use linear scale for consistency with linear freq scale of Figure 86A-3.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed U/unsatisfied Z/withdrawn
SORT ORDER: Comment ID

Cl 85 SC 85.10.10.1 P268 L46 # 107
Ghiasi, Ali Broadcom

Comment Type TR Comment Status A

The mated test fixture loss are included but the target loss for host and module test board are not included in CL85. Mated fixture loss can be met by shifting the loss from host to module or from module to host PCB by different users, in effect meeting Figure 85-12 but not interoperable

SuggestedRemedy

Please copy section 86A.5.1.1 in to CL85

Response Response Status C

ACCEPT IN PRINCIPLE.

The 85.10.10 Mated test fixtures insertion loss as well as the test fixtures (85.8.3.7-[TP-TF]) and (85.10.9-[CA-TF]) insertion losses are specified.

See response to comment #43.

Cl 85 SC 85.10.9 P267 L34 # 108
Ghiasi, Ali Broadcom

Comment Type TR Comment Status A

The cable assembly test fixture is not consistent with Eq 86A-5. Max freq range is 6 GHz which is also not consistent with Eq 85-36/37 with max range of 10 GHz. Test fixture should have at least 10 GHz freq range.

SuggestedRemedy

Please use Eq 86A-5

Response Response Status C

ACCEPT IN PRINCIPLE.

See response comment #43.

Cl **85A** SC **85A.4** P**422** L**36** # **109**
 Ghiasi, Ali Broadcom

Comment Type **TR** Comment Status **D**

The channel loss budget has been changed during D2.1 but this equation was not adjusted accordingly

SuggestedRemedy

Mated response loss 6.5 dB at 5.16 GHz, less 1.25 dB for HCB, less 0.5 dB for connector, leaves 4.75 dB loss per end.

The 4.75 dB host PCB loss is based on assumption the connector has loss of 0.5 dB, higher loss connector require reducing channel PCB loss.

Proposed Response Response Status **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

The maximum channel insertion loss of 24.44 dB is consistent with D2.1 comment#96 resolution.

where
 $IL_{Cmax}(f)$ (17.04 dB), $IL_{Host}(f)$ (6.5 dB) and $IL_{MatedTF}(f)$ (2.8 dB).

$IL_{Ch}(f) = IL_{Chmax}(f) = 17.04 + (2 \times 6.5) - (2 \times 2.8) = 24.44$ dB

Cl **85** SC **85.8.3.7** P**256** L**3448** # **110**
 Ghiasi, Ali Broadcom

Comment Type **TR** Comment Status **A**

The cable assembly test fixture is not consistent with Eq 86A-4. Max freq range is 6 GHz which is also not consistent with Eq 85-36/37 with max range of 10 GHz. Test fixture should have at least 10 GHz freq range.

SuggestedRemedy

Please use Eq 86A-4

Response Response Status **C**

ACCEPT IN PRINCIPLE.
 85.8.3.7 is Test fixture insertion loss.
 See comment #43.

Cl **85** SC **85.8.3.5** P**256** L**18** # **111**
 Ghiasi, Ali Broadcom

Comment Type **TR** Comment Status **A**

Figure 85-5 is not helpful and conflicts with definition in 85.8.3.7 and implies the loss include 100 nF and scope front end

SuggestedRemedy

Change Figure 85-5 title to "Example TP2 or TP3 Measurement Setup"

Replace TP2 or TP3 with MDI

Add a box between MDI and bias connection with RF ports, name this box Transmit/Receive Test Fixture

Added label to the RF ports "TP2/TP3"

Response Response Status **C**

ACCEPT IN PRINCIPLE.
 See response comment#158

Cl **85** SC **85.10.10.2** P**269** L**27** # **112**
 Ghiasi, Ali Broadcom

Comment Type **TR** Comment Status **D**

Nominal mated test fixture loss not defined

SuggestedRemedy

Add nominal test fixture loss at Nyquist is 2.4 dB. Test fixtures with loss lower than nominal shall account for test fixture loss difference from nominal in the equation 85-19.

Proposed Response Response Status **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

This comment was WITHDRAWN by the commenter.

CI 85 SC 85.10.10.3 P270 L32 # 113
Ghiasi, Ali Broadcom

Comment Type TR Comment Status A

Mated test fixture crosstalk loss in current draft are place holder and some of the limit specially PSFXT will impact the measurements accuracy

SuggestedRemedy

For the new limits please see ghiasi_01_0909

Response Response Status C

ACCEPT IN PRINCIPLE.

Delete content in 85.10.10.3 -
Under new 85.10.10.3:

Provide reference to ICN RMS noise calculation
for crosstalk distrubers and specify RMS noise values in a table for
NEXT = 0.7 mV
FEXT = 2.5 mV
MDNEXT= 1 mV
MDFEXT= 3.5 mV

Update PICs:

CI 86A SC 86A.5.1.1.2 P436 L32 # 114
Ghiasi, Ali Broadcom

Comment Type TR Comment Status A

Mated test fixture crosstalk loss in current draft are place holder and some of the limit specially PSFXT will impact the measurements accuracy

SuggestedRemedy

For the new limits please see ghiasi_01_0909

Response Response Status C

ACCEPT IN PRINCIPLE.
see response to comment 113

CI 85 SC 85.11.1.1 P272 L34 # 115
Ghiasi, Ali Broadcom

Comment Type TR Comment Status A

Connector IEC number is missing

SuggestedRemedy

Please add connector IEC number, if not avilable then use the SFF number

Response Response Status W

ACCEPT IN PRINCIPLE.
SFF-8436

CI 85 SC 85.11.1.1 P274 L10 # 116
Ghiasi, Ali Broadcom

Comment Type TR Comment Status R

Contact 27 is not listed in table 85-11

SuggestedRemedy

Please add all 38 contacts to table 85-11

Response Response Status W

REJECT. See response comment#2.
Table 85-12-Style-1 hardware contact definitions has been deleted; contact 27 not specified. See NOTE-Although the 40GBASE-CR4 Style-1 MDI supports 38 connections only the transmitter and receiver contact assignments are specified.

CI 85 SC 85.11.3 P277 L10 # 117
Ghiasi, Ali Broadcom

Comment Type TR Comment Status R

Some of the contcts shown in the MDI diagram are not listed in table 85-11

SuggestedRemedy

Please include all contacts

Response Response Status W

REJECT. The 100GBASE-CR10 MDI supports 84 connections only the transmitter and receiver contact assignments are specified.The other pins are not used in the scope of this specification.

Cl 86 SC 86.1 P285 L34 # 118
Ghiasi, Ali Broadcom

Comment Type **TR** Comment Status **D**

The PMD electrical definition XLPPi and CPPI has no MDI definition

SuggestedRemedy

Please MDI definition from CL 85.11

Proposed Response Response Status **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

The medium dependent interface (MDI) for Clause 86 PMDs is the optical interface between the transmission medium (fiber) and the PMD (see 1.4.220 for definition of MDI). XLPPi and CPPI are physical instantiation of PMD service interface for 40GBASE-SR4 and 100GBASE-SR10.

Cl 85 SC 85.11.1.1.1 P274 L9 # 119
Ghiasi, Ali Broadcom

Comment Type **TR** Comment Status **A**

Due to overvoltage concern see comment 208 D2.1, there is no hardware definition for CR10 similar to table 85-12

SuggestedRemedy

Please create hardware pin definition to identify CR10

Response Response Status **W**

ACCEPT IN PRINCIPLE.
See response comment#2.

Cl 85 SC 85.11.1.1.1 P274 L9 # 120
Ghiasi, Ali Broadcom

Comment Type **TR** Comment Status **A**

Due to overvoltage concern see comment 208 D2.1, the default peak to peak must not exceed 700 mV

SuggestedRemedy

Add note to 1200 mV that default output must not be greater than 700 mV to prevent over voltage damage to XLPPi or CPPI PMD

Response Response Status **W**

ACCEPT IN PRINCIPLE.

Table-85-4 footnote 1200 mV row.

Because Style-1 and 100GBASE-CR10 connectors support 40GBASE-CR4/100GBASE-CR10 and nPPI interfaces the transmitter should not exceed the nPPI voltage maximum until a 40GBASE-CR4 or 100GBASE-CR10 cable assembly has been identified.

Cl 88 SC 88.5.1 P346 L12 # 121
Ghiasi, Ali Broadcom

Comment Type **TR** Comment Status **D**

Fig 88-2 as drawn indicate and optical retimer!

SuggestedRemedy

Please move L0-L3 before and after optical mux.

Proposed Response Response Status **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

L0 through L3 are the four lanes. This designation is not specifically optical or electrical. The same arrangement is shown in Figure 53-2 and also in Figure 86-2. See also comment #125

Cl 88 SC 88.5.1 P346 L12 # 122
Ghiasi, Ali Broadcom

Comment Type TR Comment Status D

The L0-L3 is not connected to any instantiation logical or Physical

SuggestedRemedy

Please update figure to show gearbox and CAUI

Proposed Response Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

CAUI is an optional interface and therefore may not be present.
The gearbox function is within the PMA function and a possible future 25G electrical interface would not need it.
See also comment #124

Cl 83A SC 88.5.2 P395 L37 # 123
Ghiasi, Ali Broadcom

Comment Type TR Comment Status A

FR4 trace stress not clear what it is

SuggestedRemedy

Suggest either use Frequency Dependnet Attenuator or PCB Trace

Response Response Status C

ACCEPT IN PRINCIPLE.

Change:
FR4 trace stress is then added
until 0.42 UI peak-to-peak deterministic jitter is achieved

to:
Stress is then added using PCB trace or Frequency Dependent Attenuation which emulates PCB loss. PCB trace stress is added until 0.42 UI peak-to-peak deterministic jitter is achieved.

Modify diagram (change FR4 to PCB)

Make same changes in 83B.2.3

Cl 87 SC 87.5.3 P317 L12 # 124
Ghiasi, Ali Broadcom

Comment Type TR Comment Status D

The L0-L3 is not connected to any instantiation logical or Physical

SuggestedRemedy

Please update figure to show XLAUI retimer

Proposed Response Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

[Editor's note: Subclause changed from 88.5.3 to 87.5.3, Page changed from 316 to 317]

XLAUI is an optional interface and therefore may not be present.
See also comment #122

Cl 87 SC 87.5.3 P317 L12 # 125
Ghiasi, Ali Broadcom

Comment Type TR Comment Status D

Fig 87-2 as drwan indicate and optical retimer!

SuggestedRemedy

Please move L0-L3 before and after optical mux.

Proposed Response Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

[Editor's note: Subclause changed from 88.5.3 to 87.5.3]
L0 through L3 are the four lanes. This designation is not specifically optical or electrical. The same arrangement is shown in Figure 53-2 and also in Figure 86-2.
See also comment #121

Cl 88 SC 88.8.5.3 P356 L12 # 126
Ghiasi, Ali Broadcom

Comment Type TR Comment Status R

The CRU BW for the TDP measurement is defiend to be 10 MHz also see comment 224 and 225 D2.1 can limit the receiver to analog type instead of more efficent lower power digital implementation. The 10 MHz burden will remin even in the case of future generations where ASIC/SerDes operate at 25 G!

SuggestedRemedy

Propose to consider CRU BW 7.5 MHz instead of current 10 MHz, see ghiasi_02_0909

Response Response Status C

REJECT.
See Response to Comment # 127

Cl 88 SC 88.8.5.3 P356 L12 # 127
Ghiasi, Ali Broadcom

Comment Type TR Comment Status A

The CRU BW for the TDP measurement is defiend to be 10 MHz also see comment 224 and 225 D2.1 can limit the receiver to analog type instead of more efficent lower power digital implementation. The clock and power supply noise do not scale with higher baudrate so there is very little benefit of higher CRU BW. The CRU increased BW has very little benefit on the VCO noise. The 10 MHz burden will remin even in the case of future generations where ASIC/SerDes operate at 25 G!

SuggestedRemedy

Propose to consider CRU BW 7 MHz instead of current 10 MHz. Higher CRU BW has very little benefit on the VCO noise and power supply nosie but significant penalty on the receiver, see ghiasi_02_0909

Response Response Status U

ACCEPT IN PRINCIPLE.

In Table 88-13 correct the formula:
change "2 x 10⁵/ f" to "5 x 10⁵/ f"

The Task Force voted on whether to:

- A - Leave the CRU corner frequency at 10 MHz and correct the formula in Table 88-13
- B - Change the CRU corner frequency to 7 MHz in a consistent manner in clause 88

A 9
B 1

Cl 88 SC 88.8.5.3 P356 L12 # 128
Ghiasi, Ali Broadcom

Comment Type TR Comment Status R

Transmitter eye diagrm is measured CRU BW of 10 MHz also see comment 224 and 225 D2.1 can limit the receiver to analog type instead of more efficent lower power digital implementation. The clock and power supply noise do not scale with higher baudrate so there is very little benefit of higher CRU BW. The CRU increased BW has very little benefit on the VCO noise. The 10 MHz burden will remin even in the case of future generations where ASIC/SerDes operate at 25 G!

SuggestedRemedy

Propose to consider CRU BW 7 MHz instead of current 10 MHz. Higher CRU BW has very little benefit on the VCO noise and power supply nosie but significant penalty on the receiver, see ghiasi_02_0909

Response Response Status C

REJECT.
See Response to Comment # 127

Cl 88 SC 88.8.10 P357 L21 # 129
Ghiasi, Ali Broadcom

Comment Type TR Comment Status R

Stress receiver sensitivity has corner frequency of 10 MHz also see comment 224 and 225 D2.1 can limit the receiver to analog type instead of more efficent lower power digital implementation. The clock and power supply noise do not scale with higher baudrate so there is very little benefit of higher CRU BW. The CRU increased BW has very little benefit on the VCO noise. The 10 MHz burden will remin even in the case of future generations where ASIC/SerDes operate at 25 G!

SuggestedRemedy

Propose to consider corner frequency of 7 MHz instead of current 10 MHz and change 100 KHz to 70 KHz. Higher CRU BW has very little benefit on the VCO noise and power supply nosie but significant penalty on the receiver, see ghiasi_02_0909

Response Response Status C

REJECT.
See Response to Comment # 127

CI **83B** SC **83B.2.3** P**409** L**42** # **130**
 Ghiasi, Ali Broadcom

Comment Type **TR** Comment Status **A**

FR4 trace stress not clear what it is

SuggestedRemedy

Suggest either use Frequency Dependnet Attenuator or PCB Trace

Response Response Status **C**

ACCEPT IN PRINCIPLE.
 See comment 123

CI **86A** SC **86A.4.1** P**428** L**27** # **131**
 Ghiasi, Ali Broadcom

Comment Type **TR** Comment Status **R**

With current set of specifications the SerDes transmitter may have very large amount of de-emphasis 3-5 dB resulting in signifincat distortion at TP1a and also see comment 216/218 on D2.1

SuggestedRemedy

The options here are either limit max DDJ to about 0.125 UI or max 3 dB de-emphasis, see ghiasi_03_0909

Response Response Status **U**

REJECT.
 J2 spec constrains DDJ and eye mask constrains excessive emphasis.
 Although ghiasi_03_0909 shows an example module/host combination with a near failing Tx eye mask at TP2, there is insufficient information to determine the corrective action required in the spec to avoid a potential eye-mask issue. Further work is invited.

CI **85** SC **85.2** P**241** L**9** # **132**
 DiMinico, Christopher MC Communications

Comment Type **E** Comment Status **A**

Spelling interepet

SuggestedRemedy

Change interepet to interpret

Response Response Status **C**

ACCEPT.
 See suggested remedy

CI **85** SC **85.11.1.2** P**274** L**36** # **133**
 DiMinico, Christopher MC Communications

Comment Type **E** Comment Status **A**

Spelling compatability

SuggestedRemedy

Change compatability to compatibility.

Response Response Status **C**

ACCEPT.
 See suggested remedy

CI **85** SC **85.11.2** P**275** L**41** # **134**
 DiMinico, Christopher MC Communications

Comment Type **E** Comment Status **A**

Spelling assignments

SuggestedRemedy

Change asignments to assignments

Response Response Status **C**

ACCEPT.
 See suggested remedy

CI **85A** SC **85A.2** P**421** L**11** # **135**
 DiMinico, Christopher MC Communications

Comment Type **E** Comment Status **A**

Spelling voltage

SuggestedRemedy

Change votage to voltage

Response Response Status **C**

ACCEPT.
 See suggested remedy

Cl 85A SC 85A.4 P422 L27 # 136
DiMinico, Christopher MC Communications

Comment Type E Comment Status A
Spelling transmitter

SuggestedRemedy

Change transmitter to transmitter

Response Response Status C

ACCEPT.
See suggested remedy

Cl 85A SC 85A.4 P422 L43 # 137
DiMinico, Christopher MC Communications

Comment Type E Comment Status A
Spelling insertion

SuggestedRemedy

Change inserton to insertion

Response Response Status C

ACCEPT.
See suggested remedy

Cl 85 SC 85.8.3.5 P256 L1 # 138
DiMinico, Christopher MC Communications

Comment Type E Comment Status A

Provide consistency with test fixture representation and labeling in Figure 85-5 with 85.10.10 Mated test fixtures Figure 85-11.

SuggestedRemedy

See comment

Response Response Status C

ACCEPT IN PRINCIPLE.
See suggested remedy comment#158

Cl 85 SC 85.8.4.2 P258 L21 # 139
DiMinico, Christopher MC Communications

Comment Type T Comment Status A

Comment #138 against Draft 2.1 was incorrectly implemented; a4 for test 1 values should be $a_4 = 0.03$. See response to comment#138 Draft 2.1 - (2) Limits given by polynomial coefficients (low loss $a_1=2.15, a_2=.78, a_4=.03$) (high loss $a_1=6.04, a_2=0.94, a_4=0.08$).

SuggestedRemedy

Change polynomial coefficients a4 from 0.3 to 0.03).

Response Response Status C

ACCEPT.
See suggested remedy.

Cl 85 SC 85.10.10.1 P268 L40 # 140
DiMinico, Christopher MC Communications

Comment Type T Comment Status A

Rather than using minimum insertion loss [equation 85-36] and a maximum insertion loss [equation 85-37] to specify the mated test fixtures insertion loss in 85.10.10.1, I suggest we use a fit to the mated test fixtures and an ILD to address the IL deviations from the fit. This is consistent with 85.8.4.3.1 Test channel insertion loss and 85.10.2 Cable assembly insertion loss 85.10.10.1.

SuggestedRemedy

Replace minimum insertion loss [equation 85-36] and a maximum insertion loss [equation 85-37] with a specification for a fitted cable assembly insertion loss and insertion loss deviation for the mated test fixtures insertion loss in 85.10.10.1. Presentation material will be provided in support of suggested remedy.

Response Response Status C

ACCEPT IN PRINCIPLE.
See suggested responses to comment#167, comment#177 and comment#170.

Cl 99 SC ToC P13 L26 # 141
D'Ambrosia, John Force10 Networks

Comment Type E Comment Status A

There is a wrap around error in the listing for Clause 52.

SuggestedRemedy

fix wrap-around error for Clause 52 entry.

Response Response Status C

ACCEPT IN PRINCIPLE.
Fix ToC formatting as appropriate

Cl 83 SC 83.5.2 P210 L20 # 142
D'Ambrosia, John Force10 Networks

Comment Type ER Comment Status A

There is some concern regarding the use of the term mapping and how it relates to what is illustrated in Fig 83-6. The use of the word "mapping" seems to address how input lanes are directed to output lanes, but in the commenter's opinion does not do an adequate job addressing the sequencing of bits on the output lanes, which may lead to interpretation issues.

SuggestedRemedy

Further clarifying text is needed. See presentation by dambrosia.

Note - Please discuss in Logic Sub Task Force during Sept Interim.

Response Response Status C

ACCEPT IN PRINCIPLE.

In clause 83.1.4, replace "remaps" with "maps".

Replace text in 83.5.2 and Figure 83-6 with trowbridge_01_0909.pdf.

Update PICS LANE_MAPPING to read "Maintain sequence of PCSLS on all output lanes"

Cl 74 SC 74.5 P113 L4 # 143
D'Ambrosia, John Force10 Networks

Comment Type ER Comment Status R

IEEE P802.3az is making changes Clause 74 IEEE Std 802.3-2008. These changes are specific to 10GBASE-R PHYs. IEEE P802.3ba has changed Clause 74 to address 10GBASE-R and 40/100GBASE-R PHYs. Therefore, coordination between the two projects is needed to manage the changes in that project to only the 10GBASE-R PHY section.

SuggestedRemedy

Coordinate modifications of Clause 74 with IEEE P802.3az editorial team.

Response Response Status C

REJECT.

This is a reject because no changes will be made to the 802.3ba draft as a result of this comment.

The P802.3ba editorial team recognizes that the P802.3az project is also proposing changes to Clauses 74, 45 and 69. The relevant 802.3ba editors will co-ordinate with 802.3az editors regarding this issue.

The current expectation is that 802.3ba will be published before 802.3az so it will be 802.3az that will need to take into account the changes made by 802.3ba rather than the other way round.

Cl 85 SC 85.8.3.2 P250 L4 # 144
D'Ambrosia, John Force10 Networks

Comment Type E Comment Status A

There is a reference to the cable assembly ICN prior to its introduction.

SuggestedRemedy

add reference to 85.10.8 in first sentence of 85.8.3.2.

Response Response Status C

ACCEPT.
See suggested remedy

CI 85 SC 85.8.3.2 P250 L26 # 145
D'Ambrosia, John Force10 Networks

Comment Type E Comment Status A

suggest rewording that attention is drawn to the far-edn tx output noise

SuggestedRemedy

change
The measured RMS deviation for the low loss cable assembly shall meet to
For the far-end transmitter output noise the measured RMS deviation for the low loss cable assembly shall meet:

change
For the far-end transmitter output noise the measured RMS deviation for the high loss cable assembly

Response Response Status C

ACCEPT.

Change:The measured RMS deviation for the low loss cable assembly shall meet the values determined using Equation (85-2).

To:For the low loss cable assembly, the measured RMS deviation from the cable assembly ICN due to the far-end transmitter output noise shall meet the values determined using Equation (85-2).

Change:The measured RMS deviation for the high loss cable assembly shall meet the values determined using Equation (85-3).

To:For the high loss cable assembly, the measured RMS deviation from the cable assembly ICN due to the far-end transmitter output noise shall meet the values determined using Equation (85-3).

CI 85 SC 85.10.6 P264 L48 # 146
D'Ambrosia, John Force10 Networks

Comment Type E Comment Status A

Unnecessary left parenthesis at end of sub-clause heading

SuggestedRemedy

delete parenthesis at end of 85.10.6

Response Response Status C

ACCEPT.
Suggested remedy

CI 85 SC 85.10.8 P267 L1 # 147
D'Ambrosia, John Force10 Networks

Comment Type E Comment Status R

Other figures in the draft have shown where the pass region is in relation to a stated curve

SuggestedRemedy

add text "Pass Region" to region below the curve.

Response Response Status C

REJECT.

Clause 85 does not identify pass regions in other graphs and the guidance is clear..

"The total integrated crosstalk RMS noise voltage shall be less than the value specified by Equation (85-34) illustrated in Figure 85-9."

CI 86 SC 86.8.4.6.1 P300 L24 # 148
D'Ambrosia, John Force10 Networks

Comment Type E Comment Status A

looks like spacing error between text on lines 24 /25 and Fig 86-4

SuggestedRemedy

fix.

Response Response Status C

ACCEPT.

Cl 81 SC 81.1 P144 L3 # 149
 D'Ambrosia, John Force10 Networks

Comment Type E Comment Status A

The use of the term "scalable" could be misconstrued. There are two distinct interfaces - one that supports 40Gb/s and another that supports 100 Gb/s

SuggestedRemedy

Change

- a) It is scalable and capable of supporting speeds of 40 Gb/s and 100 Gb/s.
- b) Data and delimiters are synchronous to a clock reference.
- c) It provides independent 64-bit-wide transmit and receive data paths.
- d) It provides for full duplex operation only.

to

- a) The XLGMII interface supports speeds of 40 Gb/s.
- b) The CGMII interface supports speeds of 100 Gb/s.
- c) Data and delimiters are synchronous to a clock reference.
- d) It provides independent 64-bit-wide transmit and receive data paths.
- e) It provides for full duplex operation only.

Response Response Status C

ACCEPT IN PRINCIPLE.

- a) The XLGMII interface supports a speed of 40 Gb/s.
- b) The CGMII interface supports a speed of 100 Gb/s.
- c) Data and delimiters are synchronous to a clock reference.
- d) It provides independent 64-bit-wide transmit and receive data paths.
- e) It provides for full duplex operation only.

Cl 00 SC 0 P L # 150
 D'Ambrosia, John Force10 Networks

Comment Type ER Comment Status A

Several illustrations of MDI Connectors have provided greater detail than is necessary for illustration. Readers of the draft are provided with the reference document numbers for normative details regarding the connector.

Drawings include Fig 85-16, 85-17, 85-20, 85-21, 86-6

SuggestedRemedy

Simplified illustrative drawings to be provided.

Response Response Status C

ACCEPT IN PRINCIPLE.

Reference document numbers to normative details have been provided in the associated subclauses. Substitute Figures 85-16, 85-17, 85-20, 85-21 with simpler schematic diagrams that show connector pin positions.

Figure 86-6 is already very simple. However, Figure 86-8 contains more detail than necessary (reference documents for normative specs have been provided in 86.10.3.3), so replace Figure 86-8 with a simpler diagram.

Cl **83A** SC P L # 151
 D'Ambrosia, John Force10 Networks

Comment Type **TR** Comment Status **A**

A number of equations related to insertion loss / SDD21 have been arranged where the absolute magnitude of the s-parameter (a positive number) must be less than the stated equation (which is actually a negative number). All graphs of equations have been done in positive numbers.

Previous comments have discussed nomenclature. Regardless of TF decision on nomenclature these equations are in correct.

Equations include: 83A-1 and 83A-2.

SuggestedRemedy

Change 83A-1 to
 $|SDD21| \leq -0.00086 + (0.2286 \times f^{(1/2)}) + (0.08386 \times f)$

Change 83A-2 to
 $|SDD21| \leq -0.00086 + (0.2286 \times f^{(1/2)}) + (0.08386 \times f)$

Response Response Status **W**

ACCEPT IN PRINCIPLE.

See resolution to comment #15

see also dambrosia_01_0909 for parameter naming convention

Cl **83A** SC P L # 152
 D'Ambrosia, John Force10 Networks

Comment Type **TR** Comment Status **A**

A number of equations related to return loss / Sxymn have been arranged where the absolute magnitude of the s-parameter (a positive number) must be less than the stated equation. All graphs of equations have been done in positive numbers. For Return Loss constraints the requirement should be "greater than or equal to" the equation

Previous comments have discussed nomenclature. Regardless of TF decision on nomenclature these equations are in correct.

Equations include: 83A-5, 83A-7, 83A-8, and 8A-10.

SuggestedRemedy

For noted equations change sign from "less than or equal to" to "greater than or equal to"

Response Response Status **W**

ACCEPT IN PRINCIPLE.

See suggested Remedy. Change
 Equations 83A-5, 83A-7, 83A-8, and 83A-10 to "greater than or equal to" sign.

see also dambrosia_01_0909 for parameter naming convention & equation format

Ensure consistency & suggested remedy

Cl **83A** SC P L # 153
 D'Ambrosia, John Force10 Networks

Comment Type **E** Comment Status **A**

All of the figures in this clause follow equations, but there are no statements regarding an equation being illustrated in a figure

SuggestedRemedy

add statement following equation that the equation is illustrated in Fig 83A-x.

Response Response Status **C**

ACCEPT.

Section 83A.2.1

... than the insertion loss defined in Equation (83A-1) and illustrated in Figure 83A-3.

83A.2.2

... than the insertion loss defined in Equation (83A-2) and illustrated in Figure 83A-4.

83A.3.3.3

Differential output return loss requirement is illustrated in Figure 83A-6

83A.3.3.4

Common mode output return loss is illustrated in figure 83A-7

83A.3.4.3

Differential input return loss is illustrated in figure 83A-10

83A.3.4.4

Differential- to-common mode input return loss is illustrated in figure 83A-11

83A.4

The value for insertion loss is summarized in Equation (83A-9) and illustrated in figure 83A-13. The value for minimum return loss is summarized in Equation (83A-10) and illustrated in figure 83A-14

see also dambrosia_01_0909 for parameter naming convention

Cl **83B** SC P L # 154
 D'Ambrosia, John Force10 Networks

Comment Type **TR** Comment Status **A**

A number of equations related to insertion loss / SDD21 have been arranged where the absolute magnitude of the s-parameter (a positive number) must be less than the stated equation (which is actually a negative number). All graphs of equations have been done in positive numbers.

Previous comments have discussed nomenclature. Regardless of TF decision on nomenclature these equations are in correct.

Equations include: 83B-1, 83B-2, 83B-3, and 83B-4, .

SuggestedRemedy

Change 83B-1 and 83B-2 to

$$|SDD21| \leq 0.111 + (1.046 \times f^{(1/2)}) + (1.05 \times f) \quad 0.25 \leq f \leq 7$$

$$|SDD21| \leq -11.95 + (3.15 \times f) \quad 7 \leq f \leq 11.1$$

Change 83B-3 to

$$|SDD21| \leq 0.04 + (0.33 \times f^{(1/2)}) + (0.32 \times f) \quad 0.25 \leq f \leq 7$$

$$|SDD21| \leq -3.72 + f \quad 7 \leq f \leq 11.1$$

Change 83B-4 to

$$|SDD21| \leq -0.00086 + (0.2286 \times f^{(1/2)}) + (0.08386 \times f)$$

Response Response Status **W**

ACCEPT IN PRINCIPLE.

See suggested Remedy for correction of the signs.

See resolution to comment #15

see also dambrosia_01_0909 for parameter naming convention

Cl **83B** SC P L # 155
 D'Ambrosia, John Force10 Networks

Comment Type **TR** Comment Status **A**

A number of equations related to return loss / Sxymn have been arranged where the absolute magnitude of the s-parameter (a positive number) must be less than the stated equation. All graphs of equations have been done in positive numbers.

The equations all result in negative numbers
 For Return Loss constraints the requirement should be "greater than or equal to" the equation

Previous comments have discussed nomenclature. Regardless of TF decision on nomenclature these equations are in correct.

Equations include: 83B-5, 83B-6, 83B-8, and 83B-9.

SuggestedRemedy

Change Eqs 83B-5, 83B-9 to
 $|SDD11| \geq 12 - (2 * f)$ $0.01 \leq f \leq 2.19$
 $5.56 - (8.76 * \log_{10}(f/5.5))$ $2.19 \leq F \leq 11.1$

Change Eqs 83B-6, 83B-8 to
 $|SDD22| \geq 12 - (2 * f)$ $0.01 \leq f \leq 2.19$
 $5.56 - (8.76 * \log_{10}(f/5.5))$ $2.19 \leq F \leq 11.1$

For noted equations change sign from "less than or equal to" to "greater than or equal to"

Response Response Status **W**

ACCEPT IN PRINCIPLE.

See suggested Remedy for correction of the signs.

See resolution to comment #15

see also dambrosia_01_0909 for parameter naming convention

Cl **83B** SC P L # 156
 D'Ambrosia, John Force10 Networks

Comment Type **E** Comment Status **A**

All of the figures in this clause follow equations, but there are no statements regarding an equation being illustrated in a figure

SuggestedRemedy

add statement following equation that the equation is illustrated in Fig 83B-x.

Response Response Status **C**

ACCEPT.

Add the following to 83B.1:

Equation 83B-1 is illustrated in Figure 83B-1 and Equation 83B-2 is illustrated in Figure 83B-2.

Modify the following sentence in 83B.2:

The differential insertion loss, expressed in decibels, for the HCB shall be less than the insertion loss defined by Equation (83B-3) and illustrated in Figure 83B-3

Modify the following sentence in 83B-2:

The differential insertion loss, expressed in decibels, for the MCB shall be less than the insertion loss defined by Equation (83B-4) and illustrated in Figure 83B-6

83B.2.1

Modify the following:

where f is the frequency in GHz. Maximum module input reflection is illustrated in figure 83B-8

Modify the following:

where f is the frequency in GHz. Maximum module output reflection is illustrated in figure 83B-8

Make similar changes to 83B.2.2

CI 04 SC 4.4.2 P31 L31 # 157
 Dudek, Mike QLogic

Comment Type T Comment Status R

The English is strange. "...can have a minimum value due torequirements".

SuggestedRemedy

Option 1 Replace "can" with "may"

Option 2 Replace "clock tolerance and lane alignment requirements" with "clock and lane alignment allowed variations"

Do the same in Annex 4A page 369 line 24

Response Response Status C

REJECT.

The existing sentence provides better clarity than the suggested remedy.

The use of "can have" is consistent with rest of the notes in 4.4.2 of base document

CI 85 SC 85.7.1 P244 L7 # 158
 Dudek, Mike QLogic

Comment Type TR Comment Status A

This paragraph (85.7.1) says that TP2 is at the output end of the mated connector and defines this as TP2. Table 85-4 says that the specifications are at TP2, but 85.8.3.5 says that the measurements are at the output of the test fixture.

SuggestedRemedy

Change "The electrical transmit signal is defined at the output end of the mated connector TP2. Unless specified otherwise, all transmitter measurements and tests defined in Table 85-4 are made at TP2." to "The electrical transmit signal is defined at TP2 the output of the test fixture described in 85.8.3.5 mated to the connector in place of the cable. Unless specified otherwise, all transmitter measurements and tests defined in Table 85-4 are made at TP2."

In Figure 85-5 Show the connector and PCB traces to the left of TP2 or TP3.

To clarify things make the Test fixture impedance 85.8.3.6 and Test fixture insertion loss 85.8.3.7 sub-sections of 85.8.3.5.

Response Response Status C

ACCEPT IN PRINCIPLE.

(1)In Figure 85-5 illustrate Figure 85-11 TP2 or TP3 test fixture attached to TP2 or TP3 test points.

(2)Change:The electrical transmit signal is defined at the output end of the mated connector TP2. Unless specified otherwise, all transmitter measurements and tests defined in Table 85-4 are made at TP2.
 To:The electrical transmit signal is defined at TP2.
 Unless specified otherwise, all transmitter measurements and tests defined in Table 85-4 are made at TP2 utilizing the test fixture specified in 85.8.3.5.

CI 85 SC 85.8.3.2 P250 L29 # 159
 Dudek, Mike QLogic

Comment Type TR Comment Status A

The transmitter noise will add to the ICN in an RMS fashion, not a linear fashion.

SuggestedRemedy

Change Equation 85-2 and 85-3 to use RMS addition ($\sqrt{a^2 + b^2}$) not linear ($a + b$)

Response Response Status C

ACCEPT IN PRINCIPLE.

See response comment#50.

Cl 85 SC 85.8.3.3.4 P253 L42 # 160
Dudek, Mike QLogic

Comment Type T Comment Status A
Wrong reference (85.7.3.2.3 doesn't exist.)

SuggestedRemedy

Change 85.7.3.2.3 to 85.8.3.3.3

Response Response Status C
ACCEPT.
See suggested remedy.

Cl 85 SC 85.8.4.3.1 P258 L50 # 161
Dudek, Mike QLogic

Comment Type TR Comment Status A
The test cables attenuation for the interference tolerance test should have a specified value (not just a max value).

SuggestedRemedy

Delete the words "maximum allowable".

Response Response Status C
ACCEPT IN PRINCIPLE.

See response comment#91.

Cl 85 SC 85.8.4.6 P259 L18 # 162
Dudek, Mike QLogic

Comment Type T Comment Status A
We should be more explicit and normative about the location of the AC coupling capacitors

SuggestedRemedy

Replace "AC-coupling is considered to be part of the receive function for Style-2 40GBASE-CR4 connectors." with "AC-coupling shall be included in the receive function for Style-2 40GBASE-CR4 connectors."

Add an extra sub-clause in 85.10 (suggest at 85.10.9) Heading "Cable Assembly AC coupling."

"Cable assemblies for 40GBASE-CR4 using style 1 connectors and 100GBASE-CR10 shall include AC coupling capacitors see 85.11.1.1.2 and 85.11.3. Cable assemblies for 40GBASE-CR4 using style 2 connectors do not require AC coupling."

Response Response Status C
ACCEPT IN PRINCIPLE.

Replace:"The 40GBASE-CR4 and 100GBASE-CR10 receiver shall be AC-coupled to the cable assembly to allow for maximum interoperability. AC-coupling is considered to be part of the receive function for Style-2 40GBASE-CR4 connectors. For Style-1 40GBASE-CR4 and 100GBASE-CR10 plug connectors the receive lanes are AC-coupled; the coupling capacitors are contained within the plug connectors."

With:"The 40GBASE-CR4 and 100GBASE-CR10 receivers are AC-coupled. AC-coupling shall be part of the receive function for Style-2 40GBASE-CR4 connectors. For Style-1 40GBASE-CR4 and 100GBASE-CR10 plug connectors the receive lanes are AC-coupled; the coupling capacitors shall be within the plug connectors."

In 85.11.3 100GBASE-CR10 MDI AC-Coupling and 85.11.1.1.2 Style-1 AC-coupling
After: For plug connectors the receive lanes are AC-coupled; the coupling capacitors are contained within the plug connectors..add reference to 85.8.4.6. delete paragraphs below and notes.

Update: PICS

Cl 85 SC 85.8.4.2 P258 L 26 # 163
Dudek, Mike QLogic

Comment Type TR Comment Status A

For the Inteferece tolerance test the results will depend on the rise/fall times of the pattern generator. This section refers to clause 69A which calls out the max rise/fall times specified for the port under test, however we haven't specified the max Tx rise/fall time in clause 85

SuggestedRemedy

Insert an extra row in Table 85-7. "Pattern Generator Rise/Fall time". Value to be 47ps for both test 1 and test 2.

Response Response Status C

ACCEPT IN PRINCIPLE.
See response comment#91.

Cl 85 SC 85.10 P260 L 10 # 164
Dudek, Mike QLogic

Comment Type TR Comment Status A

The parameters in Table 85-8 do not adequately specify the cable as there are no insertion loss or insertion loss deviation specifications at frequencies other than 5.15625GHz. Resonances can occur that meet the specfication at this one frequency but cause problems at other frequencies. Also the return loss specification is too relaxed.

SuggestedRemedy

Change the parameter for the first row of table 85-8 to "Maximum fitted insertion loss at 5.15625 GHz". For insertion loss deviation delete "at 5.15625GHz and change the value to "see 85.10.3". Delete at 5.15625 GHz from the return loss specification and change the specification to "see equation 85-1". or "see 85.10.4"

Response Response Status C

ACCEPT IN PRINCIPLE.
Add text after: These cable assembly specifications are based upon twinaxial cable characteristics, but other cable types are acceptable if the specifications of 85.10 are met.
>>>Table 85-8 provides a summary of the cable assembly differential characteristics at 5.15625 GHz and references to the subclauses addressing each parameter.

Cl 85 SC 85.10.2 P261 L 5 # 165
Dudek, Mike QLogic

Comment Type T Comment Status A

Due to the restrictions on a1, a2 and a4, caused by the maximum insertion loss at 5.125625GHz the curve in Figure 85-6 is only one example and doesn't show the maximum insertion loss at any specific frequency. Also the reference to Figure 85-6 is duplicated on page 262 line 5

SuggestedRemedy

Change the sentence from "The fitted insertion loss corresponding to the maximum insertion loss at 5.15625 GHz and the maximum allowed values of a1, a2, and a4 is illustrated in Figure 85-6." to "The fitted insertion loss corresponding to the maximum insertion loss at 5.15625 GHz and one example of the maximum allowed values of a1, a2, and a4 is illustrated in Figure 85-6."
Change the title of figure 85-6 to "Example maximum cable assembly insertion loss".
Delete the duplicate sentence on page 262 line 5.

Response Response Status C

ACCEPT.
See suggested remedy.

Cl 85A SC 85A.2 P421 L 18 # 166
Dudek, Mike QLogic

Comment Type T Comment Status A

It is confusing that the sentence states that the specs are KR except for the transmitter characteristics in 85.8.3.8. 85.8.3.8 is the 10.3125G data rate specification which is the correct rate so doesn't need to be excluded.

SuggestedRemedy

Use the same style as is used for the Rx. ie replace the sentence with. "The transmitter characteristics are summarized in Table 85A-1".

Response Response Status C

ACCEPT IN PRINCIPLE.

Change: The specifications at TP0 are summarized in Table 85A-1 and detailed in 72.7.1.1 through 72.7.1.11 with the exception of the transmitter characteristics specified in 85.8.3.8.
To:The transmitter characteristics at TP0 are summarized in Table 85A-1.

Change:TP5 receiver characteristics are summarized in Table 85A-2.
To:The receiver characteristics at TP5 are summarized in Table 85A-2.

Cl 85 SC 85.10.9 P267 L 29 # 167
 Dudek, Mike QLogic

Comment Type TR Comment Status A

Results will vary depending on the fixture insertion loss. We should not allow this amount of ambiguity in the specifications. (otherwise we will need to guard band all the specifications by this specification ambiguity). We should also make the loss of the test fixture the same as in clause 86A. It would also be good to specify exactly what is included in the Test fixture loss. Also the test fixture loss is not matching what was used to derive the link budget (The link budget was derived in Healey_03a_0709 has the same PCB test fixture loss as clause 86A)

SuggestedRemedy

Change "The maximum test fixture insertion loss shall meet the values determined using Equation (85-35) . The values for the coefficients b1 ,b2,b3 b4 and e are given in Equation (85-16)" to ""

The reference test fixture insertion loss shall meet the values determined using Equation (85-35). Make Equation 85-35 match the loss of the MCB in 86A Also add a sentence at the end of the end of 85.10.9 "The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss should be accounted for in the measurements." Also state whether the connector loss is included in the test fixture loss or not.

Response Response Status C

ACCEPT IN PRINCIPLE.

Change "The maximum test fixture insertion loss shall meet the values determined using Equation (85-35) . The values for the coefficients b1 ,b2,b3 b4 and e are given in Equation (85-16)" to ""

The reference test fixture PCB insertion loss is given in Equation (85-35). The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss should be accounted for in the measurements.

Make Equation 85-35 match the loss of the MCB in 86A-5.

Cl 85A SC 85A.4 P422 L 46 # 168
 Dudek, Mike QLogic

Comment Type T Comment Status A

maximum used where it should be minimum

SuggestedRemedy

change maximum to minimum

Response Response Status C

ACCEPT IN PRINCIPLE.

Change: (i.e., the maximum insertion loss between TP0-TP1 and TP4-TP5) are determined..

To:(i.e., the minimum value of the sum of the insertion losses from TP0 to MDI receptacle and TP5 to MDI are determined..

Resolve with comment#180

Cl 85A SC 85A.5 P423 L 16 # 169
 Dudek, Mike QLogic

Comment Type T Comment Status A

It would help understanding if IL(Camax) were better defined.

SuggestedRemedy

Change IL(Camax) definition to "The maximum cable assembly insertion loss as measured with the cable assembly test fixtures using Equation (85-19)"

Response Response Status C

ACCEPT IN PRINCIPLE.

Change IL(Camax) definition to "The maximum cable assembly insertion loss using Equation (85-19) defined between TP1 and TP4."

Cl 85A SC 85A.5 P423 L19 # 170
Dudek, Mike QLogic

Comment Type T Comment Status D

Assuming my other comments are accepted to change to a reference loss for the test fixtures. The IL(mated) definition should be changed from maximum insertion loss to reference insertion loss

SuggestedRemedy

Change the definition of IL(mated) to "The reference insertion loss of the mated test fixture using equation (85-37)

Proposed Response Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

Despite having references for the independent test fixture insertion losses it's good to limit the insertion loss of the actual mated test fixture.

Cl 85A SC 85A.5 P423 L21 # 171
Dudek, Mike QLogic

Comment Type T Comment Status A

ILChmax(f) is a single named variable but it has been given two different curves. (equations 85A-3 and 85A-4) which is bad practice. In any case the maximum channel loss at 0.5m is not a very interesting characteristic.

SuggestedRemedy

Delete the text between lines 21 and 35. As an alternative that would perhaps have more interest consider changing this section to minimum channel loss.

Response Response Status C

ACCEPT IN PRINCIPLE.

Change: The maximum channel insertion loss with a cable assembly of 0.5 m between TP1 and TP4 is determined using Equation (85A-4).

To: The minimum channel insertion loss between TP1 and TP4 is determined using Equation (85A-4).

Change: (85A-4)

$ILCh(f) = ILChmax(f) = (0.05 \times ILCamax(f)) + (2 \times ILHost(f)) - (2 \times ILMatedTF(f))$

To: $ILCh(f) \geq (0.2 \times ILCamax(f)) + (2 \times (ILHost(f)) - (2 \times ILMatedTF(f)))$

Cl 85A SC 85A.5 P423 L20 # 172
Dudek, Mike QLogic

Comment Type T Comment Status A

It would be very helpful to better define the test points and the losses and show where equation 85A-3 comes from

SuggestedRemedy

Insert at line 20. "The losses are shown diagamatically in NEW FIG"

Use slide 14 from Healey_03a_0709 as the basis of NEW FIG. Title the figure as "Illustration of loss budget" Labelling TP1 to TP4 as "IL(camax) (17.04dB)" TP0 to TP2 and TP3 to TP5 as "IL(host)(3.25dB)" and label the mated test fixture loss as "ILMatedTF (2.8dB)"

Response Response Status C

ACCEPT IN PRINCIPLE.

Insert at line 20. "The channel insertion loss budget is illustrated in Figure-85A-xx"

Use slide 2 from diminico_05_0909.pdf as the basis for a figure illustrating loss budget. Title the figure as "Illustration of channel insertion loss budget"

Cl 85 SC 85.8.4.3.1 P258 L43 # 173
Dudek, Mike QLogic

Comment Type T Comment Status A

The units are wrong

SuggestedRemedy

It should state "Where f is the frequency in GHz."

Response Response Status C

ACCEPT. See suggested remedy.

Cl 85 SC 85.10.2 P261 L12 # 174
Dudek, Mike QLogic

Comment Type T Comment Status A

The units are wrong

SuggestedRemedy

Change to "Where f is the frequency in GHz."

Response Response Status C

ACCEPT.
See suggested remedy.

Cl 85 SC 85.8.3.6 P256 L38 # 175
Dudek, Mike QLogic

Comment Type ER Comment Status D

There are multiple equations and graphs in the clause that are functions of frequency. Most use GHz, some use MHz, Hz also occurs. It would be good to standardize them all. This specific instance obviously applies to line 42 as well. Other instances are this page lines 48 and 49 with page 257 lines 1 to 6 and related change on page 267 lines 33 and 38, and related changes in 85A page 422 line 40 and page 423 line 1
Page 262 lines 44 to 52
Figure 85-7

SuggestedRemedy

Change all the equations and graphs covering the GHz range to use GHz as listed in the comment(no technical change.)
Also do the same in Annex 85A (page 423 lines 30 and 53), (page 424 lines 43 and 46 and fig 85A-1)

Proposed Response Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

Cl 86A SC 86A.5.1.1.1 P431 L39 # 176
Dudek, Mike QLogic

Comment Type T Comment Status D

The MCB SDD21 is expected to be approximately half the loss of the HCB, but the frequency independent term ratio is far larger.

SuggestedRemedy

Change MCB frequency independent term from -0.0006 to -0.006

Proposed Response Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

Cl 85 SC 85.8.3.7 P256 L46 # 177
Dudek, Mike QLogic

Comment Type TR Comment Status A

Results will vary depending on the fixture insertion loss and 85.8.3.7 gives a maximum test fixture insertion loss (and no minimum). We should not allow this amount of ambiguity in the specifications. (otherwise we will need to guard band all the specifications by this specification ambiguity). We should also make the loss of the test fixture the same as in clause 86A for commonality. Note that the PCB loss of the test fixture of clause 86a is what was used to derive the budget in Healey_03a_0709 (which doesn't match what is here). We should also specify exactly what is included in the insertion loss.

SuggestedRemedy

Change the Test Fixture insertion loss to a reference insertion loss (not just max) and use the same equations as 86A. Also add a sentence at the end of the Test Fixture insertion loss "The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss should be accounted for in the measurements."

State in 85.8.3.6.7 that the connector loss is not included in the test fixture insertion loss.

Response Response Status C

ACCEPT IN PRINCIPLE.

Delete:The maximum test fixture insertion loss shall meet the values determined using Equation (85-16).

Add: The reference test fixture PCB insertion loss is given in Equation (85-16). The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss should be accounted for in the measurements.

Make Equation 85-16 match the loss of the HCB in 86A-4 from 0.05 GHz to 10 GHz.

Cl 85 SC 85.8.4.3.1 P258 L38 # 178
Dudek, Mike QLogic

Comment Type TR Comment Status A

We should state specifically where the test channel insertion loss is measured.

SuggestedRemedy

Change "The fitted test channel 1 or test channel 2 insertion loss ILTC(f)..." to "The fitted test channel 1 or test channel 2 insertion loss between the pattern generator and the output of the test fixture described in 85.10.9 ILTC(f)..."

Response Response Status C

ACCEPT IN PRINCIPLE.
See response comment#91

Cl 86A SC 86A.6 P446 L45 # 179
 Dudek, Mike QLogic

Comment Type TR Comment Status A

Equation 86A-20 is wrong. (requires gain at high frequency and has a discontinuity) and doesn't match Figure 86-12

Also with the correction the minimum loss at Nyquist from TP0 to TP2 is only 2.08dB based on equation 86A-20. The HCB PCB loss is 1.26dB without the connector (equation 86A-4) leaving only 0.82dB for the connector and host PCB. ie this minimum recommended loss is not really doing anything.

SuggestedRemedy

Add a row to the equation
 $0.01 < f < 1$ value 0
 Change the existing first row to $+0.5 - 0.5 * f$

Consider also increasing the minimum loss at Nyquist by approx 0.5dB by changing this existing first row to $0.6 - 0.6 * f$ and changing the second row to -3.7

Response Response Status C

ACCEPT IN PRINCIPLE.
 Change sign to make the first row
 $+0.5 - 0.5 * f$
 Note: Comment 15 has changed the overall sign of this equation.
 Also, add a row to the equation
 $0.01 < f < 1$ value 0

The minimum loss issue has been overtaken by events. The Host PCB min loss in Clause 85 has been reduced to 0.67 dB, which does not require the TP0 to TP2 min loss to change.

Cl 85A SC 85A.4 P422 L31 # 180
 Dudek, Mike QLogic

Comment Type TR Comment Status A

The definition of TP1 has been adjusted (per Healey_03a_0709) to be at the input to the cable test fixture so it does not include all the PCB, resulting in an ambiguity. The loss specified on line 33 matches the loss we have in the budget for TP0 to TP1 (not for the complete PCB) but does not match the loss in equation 85A-1 which is only 5.18dB at Nyquist. Also Clause 86A allows a max 2x4.4dB for the total PCB loss on the assumption a host might use a lower loss connector.

SuggestedRemedy

Either
 1 Delete "(ie the maximum insertion loss between TP0-TP1 and TP4-TP5)." and change the multiplier in equation 85A-1 from 0.3 to 0.508.
 2 Change the paragraph to "The maximum insertion loss allocation for the transmitter plus receiver differential controlled impedance printed circuit boards for each differential lane between TP0-TP1 and TP4-TP5 is determined using Equation (85A-1) and the coefficients b1 through b4 are given in Equation (85-16). The maximum insertion loss allocation for the transmitter and receiver differential controlled impedance printed circuit boards between these test points is 7 dB at 5.15625 GHz. Note that there is an additional 1.4dB allowance in the PCB loss for the equivalent PCB loss between TP1 and TP4 and the connectors." Change the multiplier in equation 85A-1 from 0.3 to 0.405

Response Response Status C

ACCEPT IN PRINCIPLE.

Change: The maximum insertion loss allocation for the transmitter and receiver differential controlled impedance printed circuit boards for each differential lane (i.e., the maximum insertion loss between TP0-TP1 and TP4-TP5) are determined using Equation (85A-1) and the coefficients b1 through b4 are given in Equation (85-16). The maximum insertion loss allocation for the transmitter and receiver differential controlled impedance printed circuit boards is 7 dB at 5.15625 GHz

TO: Based on 85.8.3.4 insertion loss TP0 to TP2 or TP3 to TP5 and a assumed connector los of 1.74 dB, the maximum insertion loss allocation for the transmitter and receiver differential controlled impedance printed circuit boards for each differential lane (i.e., the maximum value of the sum of the insertion losses from TP0 to the MDI host receptacle and from TP5 to the MDI host receptacle are determined using Equation (85A-1) and the coefficients b1 through b4 are given in Equation (85-16). The maximum insertion loss allocation for the transmitter and receiver differential controlled impedance printed circuit boards is 7 dB at 5.15625 GHz

Response to D2.1 comment#96 is to use gustlin_04_0709 as reach objective guidance and subsequent input for insertion loss allocation as well as clause 85 comment resolution below. In gustlin_04_0709.pdf slide 12 "to reflect 3.5 dB (Host trace)".

Cl 86A **SC 86A.6** **P 446** **L 44** # 181
Dudek, Mike QLogic

Comment Type **T** **Comment Status** **A**

The minimum loss at Nyquist from TP0 to TP2 is only 2.08dB based on equation 86A-20. The HCB PCB loss is 1.26dB without the connector (equation 86A-4) leaving only 0.82dB for the connector and host PCB. ie this minimum recommended loss is not really doing anything.

SuggestedRemedy

Response **Response Status** **C**
ACCEPT IN PRINCIPLE.
Duplicate Comment see comment 179.

Cl 83A **SC 83A.2.1** **P 383** **L 23** # 182
Dudek, Mike QLogic

Comment Type **T** **Comment Status** **A**

I seem to remember that there is a style guide rule that all figures must be referred to by some text. Even if it is not in the style guide rules it is good practice. There are a number of figures in this annex that do not have references. Figure 83A-3 is the first one.

This also applies to figure 83A-4, 83A-6, 83A-7, 83A-10, 83A-11, 83A-13, 83A-14

SuggestedRemedy

If I am correct then add "and illustrated in figure 83A-3" to the end of line 23, and a similar remedy for the other figures.

Response **Response Status** **C**
ACCEPT IN PRINCIPLE.

See comment 153

Cl 83A **SC 83A.3.3.1** **P 386** **L 8** # 183
Dudek, Mike QLogic

Comment Type **T** **Comment Status** **A**

In equations 83A-3 and 83A-4 there is a variable Vth-demph. However in table 83A-1 and Figure 83A-5 the same variable is called Vtx-demph.

SuggestedRemedy

Change Vth-demph to Vtx-demph in equations 83A-4 and 83A-4.

Response **Response Status** **C**
ACCEPT IN PRINCIPLE.

Change Vth-demph to Vtx-demph in equations 83A-3 and 83A-4.

Cl 83A **SC 83A.3.4** **P 389** **L 35** # 184
Dudek, Mike QLogic

Comment Type **T** **Comment Status** **A**

Table 83A-2 is actually a mixture of receiver characteristics (eg return losses) and specifications of the most degraded signal the receiver has to tolerate (eg total jitter.). The receiver does not have a maximum total jitter. It's characteristic is a minimum total jitter tolerance.

SuggestedRemedy

Split table 83A-2 into two tables. Table A labelled "Receiver input tolerance requirements" with everything in the existing table except the return losses. Table B labelled "Receiver characteristics" with just the return loss lines.

The sentence on page 389 line 26 then becomes. "The receiver shall tolerate signals with the characteristics given in Table A. The receiver shall also have the characteristics given in Table B".

An alternative remedy keeping one table is changing the maximum values of the input signal into minimum input tolerances as done in table 86A-4

Response **Response Status** **C**
ACCEPT IN PRINCIPLE.

Rename the following:
Maximum Total Jitter to
"Minimum Total Input Jitter Tolerance"
Maximum Deterministic Jitter to:
"Minimum Deterministic Input Jitter Tolerance"

Add row above Minimum total input jitter tolerance and have the following text:
"Stressed Receiver Tolerance"

Modify section 83A.3.4.6 accordingly (maximum becomes minimum)

Cl **83B** SC **83B.2.1** P**407** L**27** # **185**
 Dudek, Mike QLogic

Comment Type **T** Comment Status **A**

Vth-demph is used in equation 83B-7 however Vtx-demph is used in table 83B-3

SuggestedRemedy

Change Vth-demph to Vtx-demph in equation 83B-7.

Response Response Status **C**

ACCEPT.

See suggested remedy

Cl **83B** SC **83B.2** P**403** L**19** # **186**
 Dudek, Mike QLogic

Comment Type **TR** Comment Status **A**

The loss of the host compliance board is allowed to vary from zero to 2.1dB at Nyquist.
 This will significantly change the results of measurements.

SuggestedRemedy

Either

1 Change the sentence on line 19 to "The differential insertion loss, CPIL, expressed in decibels, for the reference HCB shall be CPIL, as defined by Equation (83B-3). Differences between this reference loss and the loss of an actual HCB shall be accounted for in the measurements.
 Change the inequality in equation 83B-3 into =.
 Change figure 83B-5 to HCB PCB 2.1dB

or

2 add a minimum loss for the HCB with this minimum loss scaled to 1.1dB at the Nyquist rate
 Change figure 83B-5 to HCB PCB between 1.1 and 2.1dB

Response Response Status **C**

ACCEPT IN PRINCIPLE.

Delete text: "The differential insertion loss, CPIL, expressed in decibels, for the HCB shall be less than CPILmax, as defined by Equation (83B-3)"
 Replace with:"

The reference HCB test fixture PCB insertion loss is given in Equation (83B-3-[note change <= to =]). The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss should be accounted for in the measurements.

Cl **86** SC **86.7.3** P**294** L**42** # **187**
 Petrilla, John Avago Technologies

Comment Type **ER** Comment Status **A**

Footnote b in Table 86-8 states,"Measured with conformance test signal at TP3 (see 86.8.4.7) for BER = 10-12.", yet the setup conditions are J2 and J9 and, at least where the nPPI interface is exposed, see item e of 86.8.4.8, the output criteria is an eye mask with a 5E-5 hit ratio. No where is BER = 1E-12 mentioned. This apparent conflict can be confusing. Since 86.8.4.7 references 52.9.9 which calls for operation, "with BER less than 10-12", there is no need to mention BER in note b and the apparent conflict is removed.

SuggestedRemedy

Change Footnote b from "Measured with conformance test signal at TP3 (see 86.8.4.7) for BER = 10-12." to "Measured with conformance test signal at TP3 (see 86.8.4.7)."

Response Response Status **C**

ACCEPT.

The stressed receiver test refers to 52.9.9 for the test method which explicitly calls for a BER of 10^-12.

Cl **86** SC **86.7.3** P**294** L**33** # **188**
 Petrilla, John Avago Technologies

Comment Type **ER** Comment Status **A**

In table 86-8, the attribute, "Receiver jitter tolerance signal level in OMA, each lane" is really a test condition and as such should be included with the other jitter tolerance test conditions.

SuggestedRemedy

In table 86-8, move the attribute, "Receiver jitter tolerance signal level in OMA, each lane" so that it is included with the other jitter tolerance test conditions.

Response Response Status **C**

ACCEPT IN PRINCIPLE.

Change the "Type" entry for "Receiver jitter tolerance signal level in OMA, each lane" in Table 86-8 from "-" to "Max"

The "Receiver jitter tolerance signal level in OMA, each lane" is the test in the same way as "Stressed receiver sensitivity in OMA, each lane" is a test. If the optical power required to give 10^-12 BER in the presence of the specified jitter is above this limit, the device fails.

Cl 86 SC 86.7.3 P294 L35 # 189
 Petrilla, John Avago Technologies

Comment Type TR Comment Status A

In table 86.8, unlike the case for Stressed receiver sensitivity which has an explicit entry for the attribute, there is no entry for a receiver tolerance attribute, only conditions for such. Further, there is no explicit link to the test definition in 86.8.4.8 which may compound the confusion of the missing test entry. Finally, since this is a test of the ability of a system to track low frequency jitter, it would be helpful to note (similar helpful information are included in footnotes a & c) that the test is not intended for subsystems where CDR and/or bit-error-detector functions is/are not included. See figure 86-14 which shows a System under test, SUT, comprising a PCS, PMA and PMD. Without the CDR and bit-error-detector of the PMA and/or PCS, equipment external to the SUT would be needed and the test would become, primarily, a test of this external equipment.

SuggestedRemedy

In Table 86-8, insert an entry, "Receiver jitter tolerance in BER, each lane" above the "Conditions of receiver tolerance test". Append a footnote indicator at the end of the entry. In the Type column enter "Max". In the value column enter "10-12" and leave a blank in the units column. For the footnote, insert, "Measured with conformance test signal at TP3. See 86.8.4.8. This is test of the system receiver's ability to track low frequency jitter and is inappropriate for any subsystem that does not include CDR and/or bit-error-detector function(s)."

Response Response Status C

ACCEPT IN PRINCIPLE.

In table 86-8 add a note to "Receiver jitter tolerance signal level in OMA, each lane" to say: "This is test of the optical receiver's ability to track low frequency jitter and is inappropriate for any subsystem that does not include a CRU."

See also response to comment #188

Cl 86 SC 86.8.4.8 P301 L33 # 190
 Petrilla, John Avago Technologies

Comment Type TR Comment Status A

Clause 68.6.11 is referenced with exceptions. There is no exception declared for the requirement in 68.6.11, "The optical waveform is connected ... and mode-conditioning patch cord suitable for 62.5/125 um fiber". The "mode-conditioning patch cord suitable for 62.5/125 um fiber" does not seem necessary for SR and, if not, is an unnecessary burden. If such a mode-conditioning patch cord is required, then further definition of its characteristics and use are required.

SuggestedRemedy

In 68.6.11 add another exception, f), to the list that states, 'the mode-conditioning patch cord suitable for 62.5/125 um fiber is not used'.

Response Response Status C

ACCEPT IN PRINCIPLE.

In 86.8.4.8 add another exception to the list: 'f) The mode-conditioning patch cord suitable for 62.5/125 um fiber is not used.'

Cl 86A SC 86A.4.1.1 P429 L1 # 191
 Petrilla, John Avago Technologies

Comment Type ER Comment Status A

Figure 86A-1 does not declare the units for the y-axis. While the units may be inferred from the associated equations, the y-axis title lists SDD11 and similar terms but the equations are '20 log (...) = ...', so there's not a one-to-one match. For consistency, if the '20 log (...) remains in the equation it should be in the axis title. Otherwise we appear to be saying that $20\log_{10}(|SDD11|) = SDD11$. Further, while the units for the x-axis could also be inferred from the equations they are explicit in the x-axis title. Similar cases occur for figures 86A-2, 3, 4, 5 & 6.

SuggestedRemedy

1, If the 20 log(...) terms remain in the reflection and response equations, then they should be included in the associated y-axis titles for figures 86A-1, 2, 3, 4, 5 & 6.

2, dB should be included as the y-axis units for figures 86A-1, 2, 3 & 4.

Response Response Status C

ACCEPT IN PRINCIPLE.

The response to comment 15 has modified the y-axis titles of these figures. Include "dB" as the units for these.

CI 86A SC 86A.1 P427 L15 # 192
Petrilla, John Avago Technologies

Comment Type E Comment Status R

In the overview it's said about PPI that, "It allows the construction of compact optical transceiver modules for 40GBASE-SR4 or 100GBASE-SR10 with no clock and data recovery circuits inside." As PPI can similarly support 40GBASE-LR4 modules, the overview should make that visible. Further PPI does not preclude use of CDRs within a module.

SuggestedRemedy

Change from, "It allows the construction of compact optical transceiver modules for 40GBASE-SR4 or 100GBASE-SR10 with no clock and data recovery circuits inside." to "It allows the construction of compact optical transceiver modules for 40GBASE-SR4, 40GBASE-LR4 or 100GBASE-SR10 with no clock and data recovery circuits required inside."

Response Response Status C

REJECT.
Draft 2.2 says "allows" so the "required" isn't needed.
The suitability of PPI for 40GBASE-LR4 has not been shown; the expected link induced eye closure penalty for LR4 is significantly worse than for SR4.

CI 86A SC 86A.4.2 P431 L16 # 193
Petrilla, John Avago Technologies

Comment Type ER Comment Status D

In Table 86A-4, unlike table 86-8, there is no explicit indication of a low frequency SJ jitter tolerance requirement, although there is much detail in the associated 86A.5.3.8, specifically the template in 86A.5.3.8.6. It doesn't seem good practice where a table of requirements is available not to identify all significant attributes.

SuggestedRemedy

In table 86A-4, add a row, 'Applied sinusoidal jitter', for low frequency SJ to the receiver signal tolerance test conditions. Enter 'TP4' in the Test Point column, 'See 86A.5.3.8' in the Spec.values column, and leave the Units and Conditions columns blank.

Proposed Response Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

Response to comment 194, gives pointer to 86A.5.3.8.

However, there is no need to add all of the test details to the table. This type of added jitter is not called out in the table in several other places in the draft and also in the base standard.

CI 86A SC 86A.4.2 P431 L16 # 194
Petrilla, John Avago Technologies

Comment Type ER Comment Status A

In Table 86A-4, as in table 86-8, there is no explicit entry for a signal or jitter tolerance attribute, only the conditions are listed.

SuggestedRemedy

In Table 86A-4, insert an entry, "Host receiver signal tolerance in BER, each lane" above the "Conditions of host electrical receiver signal tolerance test:". Append a footnote indicator at the end of the entry. In the Type column enter "Max". In the value column enter "10-12" and leave a blank in the units column. For the footnote, insert, "Measured with conformance test signal at TP4. See 86A.5.3.8. The eye mask, DDPWS, J2 and J9 are test conditions for measuring signal tolerance and are not characteristics of the host receiver."

Response Response Status C

ACCEPT IN PRINCIPLE.
Add a row for "Receiver signal tolerance, each lane (BER)", "-", "10^12", "-"
Add footnote for "Conditions of host electrical receiver signal tolerance test:": "The specification values are test conditions for measuring signal tolerance and are not characteristics of the host receiver (see 86A.5.3.8)."

CI 86A SC 86A.4.2 P431 L21 # 195
Petrilla, John Avago Technologies

Comment Type TR Comment Status R

In Table 86A-4, the value for the Transition time value is shown as, "34 TBC". A pre-determined transition time value may preclude generating a stressed signal that reaches all of the eye mask coordinates, J2, J9 and DDWPS simultaneously. Since there appears to be more value having an input signal that simultaneously stresses min and max signal levels, eye mask corners, J2, J9 and DDPWS, a transition time spec may be redundant.

SuggestedRemedy

Delete the Transition time requirement from Table 86A-4 and in 86A.5.3.8.5 append to the end of the sentence, "The vertical eye opening and peak level specifications are verified." 'such that eye mask coordinates X1, X2, Y1, Y2, and jitter values DDPWS, J2, J9 are all simultaneously met.' In 86A.5.3.8.5 page 444, line 12, change the phrase, "... the amplitude and the transition time are as given in Table 86A-4." to "... and the amplitude are as given in Table 86A-4."

Response Response Status C

REJECT.
Commenter invited to submit material which justifies removing the Transition time spec.

The task force believes that it is more important to stress the minimum signal levels than the maximum, so there is no need to remove the rise time requirement.

Cl **86A** SC **86A.5.3.3** P**439** L**33** # **196**
 Petrilla, John Avago Technologies

Comment Type **T** Comment Status **A**

Is the position of bit 1 in PRBS9 defined in 802.3? If so please cite a reference? If not delete, "These are bits 10 to 18 and 1 to 14, respectively." or create a definition for bit 1.

SuggestedRemedy

Unless a definition that permits locating bit 1 exists, delete the sentence, "These are bits 10 to 18 and 1 to 14, respectively.". Otherwise cite the definition.

Response Response Status **C**

ACCEPT IN PRINCIPLE.

Change "These are bits 10 to 18 and 1 to 14, respectively." to "These are bits 10 to 18 and 1 to 14, respectively, where bits 1 to 9 are the run of nine zeros."

Cl **86A** SC **86A.5.3.8** P**441** L**23** # **197**
 Petrilla, John Avago Technologies

Comment Type **E** Comment Status **A**

The 'shall' in "Host electrical receiver signal tolerance shall be defined by the procedures and requirements of 86A.5.3.8.1 to 86A.5.3.8.6." seems more an instruction to the editors than to implementers.

SuggestedRemedy

Change, "Host electrical receiver signal tolerance shall be defined by the procedures and requirements of 86A.5.3.8.1 to 86A.5.3.8.6." to "Host electrical receiver signal tolerance is defined by the procedures and requirements of 86A.5.3.8.1 to 86A.5.3.8.6." or if a shall statement is desired to "To be compliant a host electrical receiver signal tolerance shall satisfy the requirements defined by the procedures and requirements of 86A.5.3.8.1 to 86A.5.3.8.6."

Response Response Status **C**

ACCEPT IN PRINCIPLE.

Change, "Host electrical receiver signal tolerance shall be defined by the procedures and requirements of 86A.5.3.8.1 to 86A.5.3.8.6." to:

"To be compliant a host electrical receiver signal tolerance shall satisfy the requirements of 86A.5.3.8.1 to 86A.5.3.8.6."

Cl **86A** SC **86A.5.3.8.6** P**445** L**16** # **198**
 Petrilla, John Avago Technologies

Comment Type **T** Comment Status **A**

The term LB in figure 86A-11 is not defined. Assuming it's the same LB as in 87 and 88, the definition in 88.8.10, "LB = loop bandwidth; Upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested." can be referenced or copied and pasted below figure 86A-11.

SuggestedRemedy

Insert after figure 86A-11, the definition for LB, "LB = loop bandwidth; Upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested."

Response Response Status **C**

ACCEPT IN PRINCIPLE.

Add table with appropriate expressions to describe figure 86A-11, following the style of table 87-13, with editorial licence to make it look smashing !

add footnote to table:

"LB = loop bandwidth; upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested."

See king_01_0909 for example table and text

Cl **86A** SC **86A.4.1.1** P**429** L**28** # **199**
 Petrilla, John Avago Technologies

Comment Type **E** Comment Status **R**

The title for figure 86A-1 is, "Reflection specifications" but is more properly, 'Reflection specifications illustrations' as the specifications are in the associated table and equations. Even the text, see page 428, line 44 states, "the limit given in Equation 86A-2 and illustrated in Figure 86A-1." Similar issues exist with Figures 86A-2, 3, 4, 5 & 6.

SuggestedRemedy

Change the title for figure 86A-1 from, "Reflection specifications", to 'Reflection specifications illustrations'. Do likewise for figures 86A-2, 3, 4, 5 & 6 .

Response Response Status **C**

REJECT.

The title follows the precedent set in the rest of the document and in clause 52.

Cl **83B** SC **83B.1** P**402** L**34** # **200**
 Petrilla, John Avago Technologies

Comment Type **ER** Comment Status **A**

Repeating comment 159 of D2.1, Figure 83A-1 is similar to Figure 83B-3 but the names on what may be identical items are different, e.g. XLAUI/CAUI Component vs XLAUI/CAUI IC, Driver vs Transmitter, Input vs Receiver. It's not good practice where block diagrams showing the same level of detail use different names for the same item. If these block diagram elements are actually the same, please use the same terminology, otherwise this is inconsistent and can be confusing. See also Figs 83B-5 & 7.

SuggestedRemedy

If the XLAUI/CAUI Component & XLAUI/CAUI IC are the same use the same name. Likewise for Driver & Transmitter use Transmitter and for Input & Receiver use Receiver.

Response Response Status **C**

ACCEPT IN PRINCIPLE.

For Driver use Transmitter and for Input use Receiver and use Component instead of IC in figure 83B-3, 83B-5, 83B-7

Cl **83A** SC **83A.3.3.5** P**388** L**32** # **201**
 Petrilla, John Avago Technologies

Comment Type **ER** Comment Status **A**

Requirements for TJ and DJ are found in a subclause titled, "Transmitter eye mask definition". This can make these definitions difficult to find and seems unnecessary as a subclause can easily be added for jitter definition.

SuggestedRemedy

Create a subclause, '83A.3.3.6 Transmitter jitter definition'. Cut the sentence, "The measured jitter at the transmit compliance point shall be less than the maximum Total Jitter as defined in Table 83A-1 and a maximum Deterministic Jitter as defined in 83A-1." from 83A.3.3.5 and paste it into 83A.3.3.6 as the first sentence. From 83A.3.3.5 copy the sentence "Jitter and eye mask measurement requirements are described in 83A.5.1, and are conducted with de-emphasis off." and paste it into 83A.3.3.6 deleting the words, 'and eye mask'. Then in 83A.3.3.5, in the last sentence delete the words, 'Jitter and'. Update the references in tables 83B-3 and 83B-5 to refer to 83A.3.3.6 for TJ and DJ.

Response Response Status **W**

ACCEPT IN PRINCIPLE.

Modify title to "Transmitter eye mask and transmitter jitter definition"

Cl **83A** SC **83A.3.4.6** P**393** L**4** # **202**
 Petrilla, John Avago Technologies

Comment Type **T** Comment Status **A**

In figure 83A-12 the template for SJ tolerance includes the region below 40 kHz while similar templates in clauses 87 and 86A do not. Clause 87 explicitly defines this region as not specified. These low freq jitter tolerance tests all have the same objective and there seems no reason for a difference in 83A.

SuggestedRemedy

Redraw the template in 83A-12 to stop below 40 kHz. For reference, see figure 87-5 or 86A-11.

Response Response Status **C**

ACCEPT.

See suggested remedy

Cl **83B** SC **83B.2.1** P**405** L**40** # **203**
 Petrilla, John Avago Technologies

Comment Type **ER** Comment Status **D**

In table 83B-2, compliance point terms TP1, TP1a and TP4 are used without definition or reference. If these are the same points as in clause 86 or 86A, then 86 should be cited. (Clause 85 also defines a TP1 and TP4 but no TP1a) If not, there should be a figure defining these points.

SuggestedRemedy

If TP1, TP1a and TP4 are the same as in clause 86, add a note to table 83B-2 citing clause 86, figure 86-3, for the definition of these points.

Proposed Response Response Status **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Following statement is currently present in 83B.2.1:

"Table 83B-2 also lists the equivalent test points for the XLPPI/CPPI (see Figure 86-3)."

Cl **83B** SC **83B.2.1** P**407** L **20** # **204**
 Petrilla, John Avago Technologies

Comment Type **E** Comment Status **A**

Table 83B-3 footnote a is redundant with the entry in the subclause column and can be deleted. This also occurs in Table 83B-5

SuggestedRemedy

In table 83B-3 and 83B-5, delete footnotes a.

Response Response Status **C**

ACCEPT.

Cl **80** SC **80.1.4** P**127** L **29** # **205**
 Trowbridge, Stephen Alcatel-Lucent

Comment Type **E** Comment Status **A**

The optical interfaces listed in the table give their respective reaches while the electrical interfaces do not.

SuggestedRemedy

For 40GBASE-KR4, add "with reach up to at least 1m"

For 40GBASE-CR4 and 100GBASE-KR4, add "with reach up to at least 7m"

Response Response Status **C**

ACCEPT IN PRINCIPLE.

In Table 80-1 and clause 1.4

For 40GBASE-KR4, add "with reach up to at least 1m"

For 40GBASE-CR4 and 100GBASE-CR10, add "with reach up to at least 7m"

Cl **80** SC **80.2.3** P**128** L **17** # **206**
 Trowbridge, Stephen Alcatel-Lucent

Comment Type **E** Comment Status **A**

Runon sentence (too many "ands")

SuggestedRemedy

Replace

"The FEC sublayer can be placed in between the PCS and PMA sublayers or between two PMA sublayers and is instantiated for each PCS lane, and operates autonomously on a per PCS lane basis."

with

"The FEC sublayer can be placed in between the PCS and PMA sublayers or between two PMA sublayers, is instantiated for each PCS lane, and operates autonomously on a per PCS lane basis."

Response Response Status **C**

ACCEPT.

Cl **81** SC **81.5** P**158** L **50** # **207**
 Trowbridge, Stephen Alcatel-Lucent

Comment Type **T** Comment Status **A**

The specification of which sequence ordered set values is reserved is not specified clearly. It appears that lane one or lane two can be anything ($\geq 0x00$) but that lane 3 must be $\geq 0x03$ for it to be a reserved value. But a value like 0x01 0x00, 0x00 in lanes 1-2-3 are probably also in the group that are considered to be reserved even though it doesn't meet the lane 3 inequality.

SuggestedRemedy

Consider showing three rows for reserved:

lane 1 $\geq 0x01$, lane 2 $\geq 0x00$, lane 3 $\geq 0x00$

lane 1 $\geq 0x00$, lane 2 $\geq 0x01$, lane 3 $\geq 0x00$

lane 1 $\geq 0x00$, lane 2 $> 0x00$, lane 3 $\geq 0x03$ (the existing one)

Lane 3 can be 0x01 or 0x02 if lane 1 or lane 2 is $\geq 0x01$ and it is still reserved

Response Response Status **C**

ACCEPT IN PRINCIPLE.

Delete this row and add a note:

"All other values in lanes 1-3 not shown in this table are reserved."

Cl 83 SC 83.5.10 P L 23 # 208
 Nicholl, Gary Cisco

Comment Type TR Comment Status D

"If supported, when send TX PRBS31 test pattern is enabled by the PRBS31_enable and PRBS_TX_gen_enable control variables, the PMA shall generate a PRBS31 pattern (as defined in 49.2.8) on each of the lanes toward the service interface below the PMA via the inst:IS_UNITDATA_i.request primitive."

Suggest adding a referenece to Figure 83-5 to make it clear in which direction the PRBS signal is being generated.

SuggestedRemedy

Change sentence to read:

"If supported, when send TX PRBS31 test pattern is enabled by the PRBS31_enable and PRBS_TX_gen_enable control variables, the PMA shall generate a PRBS31 pattern (as defined in 49.2.8) on each of the lanes toward the service interface below the PMA via the inst:IS_UNITDATA_i.request primitive (see Figure 83-5)"

Proposed Response Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

Cl 45 SC 45.2.3.16a P74 L51 # 209
 Nicholl, Gary Cisco

Comment Type TR Comment Status D

I think the following sentence on line 51 is incorrect:

"The 20 bit counter shall be reset to all zeros when register 3.33 is read or upon PCS reset."

This means the upper 14 bits in register 3.44 would immediately be cleared when software reads the lower 6 bits in register 3.33. This means that software would likely always read all zeros from register 3.44.

SuggestedRemedy

I think the sentenace should say:

"The lower 6 bits of the 20 bit counter shall be reset to all zeros when register 3.33 is read or upon PCS reset and the upper 14 bits of the 20 counter shall be reset to all zeros when register 3.44 is read or upon PCS reset".

Also is the assumption that while the upper 14 bits of register 3.44 are in a latched state (due to a software read of the lower 6 bits in register 3.33) that errors continue to be accumulated in the background and are not simply ignored ? I guess what I am getting at here is if there is any time requirement or constraint between software reading 3.33 and subsequently reading 3.44 to ensure that no errors are missed ? For example if after reading 3.33 software has to read 3.44 before 3.33 overflows at a count of $2^6=64$ errors, then this would place a constraint that software would have to read 3.44 no later than ~211us after reading 3.33 ... this seems fairly tight. Perhaps we need a note to clarify the behavior or expectations a little more clearly ?

Proposed Response Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

[Editor's note: The commenter did not indicate Comment Type. So assigned Comment Type: TR]

Cl 45 *SC* 45.2.3.37 *P*84 *L*8 # 210
 Nicholl, Gary Cisco

Comment Type **TR** *Comment Status* **A**

Table 45-114a defines an 8 bit BIT counter for each PCS lane.

Slide 6 in http://www.ieee802.org/3/ba/public/jan09/nicholl_01_0109.pdf, recommended that:

"A suitably sized counter shall be allocated in the MDIO memory space for each PCS lane, to ensure that the counter will not saturate (overflow) even if polled at a rate of once per second."

This proposal was accepted by the group as documented in the response to comment #374 in http://www.ieee802.org/3/ba/public/jan09/P8023ba-D11_Final_Resolution_byClause.pdf.

An 8 bit counter is not a 'suitably size' counter.

A suitably sized counter would be 14 bits.

SuggestedRemedy

Update all PCS lane BIP counters to be at least 14 bits. The simplest approach would be to assign a full 16 bit register to each PCS lane BIP counter.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

[Editor's note: The commenter did not indicate Comment Type. So assigned Comment Type: TR]

Change all PCS BIP counters to 16 bit.

Cl 83 *SC* 83.5.2 *P*211 *L*51 # 211
 Nicholl, Gary Cisco

Comment Type **E** *Comment Status* **A**

Note on Fig 83-6 is incorrect. Note reads:

"NOTE: i.k indicates bit i on PCSL k. Skew may exist between PCSLs"

The i and k are reversed from what is shown in the figure.

SuggestedRemedy

Change note to read:

NOTE: i.k indicates bit k on PCSL i. Skew may exist between PCSLs

Response *Response Status* **C**

ACCEPT.

CI 83 SC 83.3 P208 L29 # 212
 Nicholl, Gary Cisco

Comment Type E Comment Status D

See the following note under Figure 83-5:

"inst PMD, PMA, or FEC, depending on which sublayer is below this PMA SIL Signal."

The paramter 'inst' appears to be there to address the fact that the sublayer below the PMA can be either a PMD,PMA or FEC.

No such convention appears to be adopted on the same figure for the interface above the PMA. In this case the service interface primitives are 'hard coded' with the name PMA, even though the sublayer above the PMA can be either a PMA, FEC or PCS.

SuggestedRemedy

Suggest adopting a similar naming convention for the service interface primitives for the interface above the PMA (i.e. at the top of the figure), to reflect that the sublayer above the PMA can be either a PMA, FEC or PCS.

Proposed Response Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

The service interface is named according to the sublayer that provides the service. The problem with the sublayer below is that you know that the sublayer provides the generic service interface, but you don't know which sublayer it is (PMD, PMA, or FEC) that is providing it. To describe the PMA service interface, the sublayer providing the service is always the PMA, so you can name the primitives, e.g., PMA:IS_UNITDATA_i.request(tx_bit) without having to know whether it is the PCS, FEC, or another PMA invoking that primitive

CI 82 SC 82.2 P170 L42 # 213
 Nicholl, Gary Cisco

Comment Type E Comment Status R

Figure 82-2 does not show any indication of the PCS lane BIP error check (although it does show the BER monitor based on sync header errors)

SuggestedRemedy

Update Figure 82-2 to show BIP error monitoring.

Response Response Status C

REJECT.

BIP insertion and removal are part of the alignment and removal blocks. Consensus of the logic sub-TF is not to clutter the diagram.

CI 82 SC 82.2.14 P183 L13 # 214
 Nicholl, Gary Cisco

Comment Type E Comment Status A

I know what is meant, but I still find that the phrase "for each 8-bit BIP value in error" in the last sentence is not as clear as it could be.

SuggestedRemedy

Suggest replacing the last sentence with:

"If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register is incremented by one, each time the calculated BIP value does not exactly match the BIP value received in the BIP3 field (registers 3.90 through 3.99)."

Response Response Status C

ACCEPT IN PRINCIPLE.

Change:

"If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register is incremented for each 8-bit BIP value in error (registers 3.90 through 3.99)."

To:

"If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register (registers 3.90 through 3.99) is incremented by one each time the calculated BIP value does not equal the value received in the BIP3 field."

Cl 45 SC 45.2.3.37 P84 L19 # 215
Nicholl, Gary Cisco

Comment Type E Comment Status R

Text does not make it clear that as agreed to at the last meeting we changed from counting bit to block errors.

SuggestedRemedy

Update text to reflect the fact that these counters are now counting block errors as described in section 82.2.14 and associated comment against the same section that I submitted this time against D2.2.

Response Response Status C

REJECT.

82.2.14 was changed by comment #270 against draft 2.1. It is now clear that block errors are counted, not bit errors. Nothing in 45.2.3.37 contradicts this.

Cl 45 SC 45.2.1.98 P66 L6 # 216
Nicholl, Gary Cisco

Comment Type T Comment Status A

Table 45-65d.

The PRBS error counter is only sized at 12 bits. This means the counter will saturate at a count of 2^{12} or 4096 errors. Assuming the host is polling the counters at a rate of once per second, then the counter will saturate at an error rate of $\sim 1.6e-7$ for a 25G lane rate. To facilitate optical waterfall curve testing it would be preferable for the counter not to saturate up to an error rate of $1e-4$.

SuggestedRemedy

As an absolute minimum I see no reason why all 16 bits of the register cannot be assigned to the PRBS error count (why leave the upper 4 bits as reserved and not use them?). This would move the saturation point up to $2.6e-6$ for a 25G lane rate. Ideally I would like to see the PRBS error counters sized to 24 bits or greater, so they would not saturate even up to $1e-4$.

Response Response Status C

ACCEPT IN PRINCIPLE.

Change all PRBS error counters to 16 bits.

Cl 45 SC 45.2.3.16a P74 L49 # 217
Nicholl, Gary Cisco

Comment Type T Comment Status A

This section defines a 20 bit BER counter. It was my understanding that we agreed to increase the size of the BER counter to at least 24 bits as defined in http://www.ieee802.org/3/ba/public/may08/nicholl_02_0508.pdf.

Reading through the proposed implementation in this section I can understand the reluctance to increase the counter to the full 24 bits, as this would require assigning another full 16 bit register. However given this an aggregate BER counter (i.e. one single count for the interface) then adding one extra register would not appear to be a huge overhead.

SuggestedRemedy

Consider increasing the size of the BER counter to be 24 bits as recommended in http://www.ieee802.org/3/ba/public/may08/nicholl_02_0508.pdf, or as a minimum use all 16 bits in the higher order register for the BER count, resulting in a 22 bit aggregate counter (lower 6 bits in reg 3.33 and the upper 16 bits in reg 3.44).

Response Response Status C

ACCEPT IN PRINCIPLE.

Increase the total counter size to 22 bits.

Cl 85 SC 85.8.3 P251 L2531 # 218
Li, Mike Altera

Comment Type TR Comment Status A

data dependent jitter (DDJ) is not given

SuggestedRemedy

Give the data dependent jitter (DDJ) definition: DDJ is the zero-crossing time deviation referenced to the ideal bit clock timing derived from an averaged differential waveform where uncorrelated signal components have been removed.

Response Response Status C

ACCEPT IN PRINCIPLE.

Expand footnote c in Table 85-4 to add definition for DDJ:

DDJ is a jitter component where jitter that is not correlated to the data pattern has been removed.

Resolve with comment#98.

Cl 85 SC 85.8.3 P251 L 2531 # 219
Li, Mike Altera

Comment Type TR Comment Status A

DDJ should be specified. With the TJ being uncorrelated TJ (namely TJ with DDJ removed) in D2.2, DDJ is now not bounded and this needs to be fixed.

SuggestedRemedy

Needs to give a DDJ up limit.

Response Response Status C

ACCEPT IN PRINCIPLE.

DDJ limit not needed with response to comment#90.

Cl 85 SC 85.8.3 P251 L 2531 # 220
Li, Mike Altera

Comment Type TR Comment Status A

Tx jitter testing method and procedure is not defined.

SuggestedRemedy

Needs to give the Tx jitter testing method, including Tx equalization setting and receiver CDR condition.

Response Response Status C

ACCEPT.

See response to comment#98

Cl 85 SC 85.8.3 P251 L 2531 # 221
Li, Mike Altera

Comment Type TR Comment Status D

"Total jitter excluding DDJ" is a confusing and self-inconsistent name. Total jitter is not "total" anymore if DDJ is removed.

SuggestedRemedy

Change "Total jitter excluding DDJ" to uncorrelated total jitter (uTJ).

Proposed Response Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

Total jitter excluding DDJ sufficiently characterizes the parameter.

Cl 85 SC 85.8.3 P251 L 2531 # 222
Li, Mike Altera

Comment Type TR Comment Status A

Amplitude pk-to-pk (line 19) and Far-end transmit output noise (line 22-23) are max values and are not specified

SuggestedRemedy

Add (max) after those parameters.

Response Response Status C

ACCEPT.

See suggested remedy and remedy to comment#87

Cl 83A SC 83A.3.3.2 P386 L 42 # 223
Latchman, Ryan Gennum Corp

Comment Type T Comment Status A

"Rise/fall time is measured with de-emphasis off" should include a reference to 83A.5.1

SuggestedRemedy

"Rise/fall time is measured with de-emphasis off as defined in 83A.5.1"

Response Response Status C

ACCEPT.

See suggested remedy

Cl 83B SC 83B.1 P402 L 3 # 224
Latchman, Ryan Gennum Corp

Comment Type T Comment Status A

Equation for module loss not correctly scaled

SuggestedRemedy

correctly scale

$SDD22 = 3.2 - 0.84f$ $7 < f < 11$

Response Response Status C

ACCEPT IN PRINCIPLE.

$SDD21 \leq 3.2 - 0.84f$ $7 \leq f \leq 11$

Cl 85 SC 85.8.3.5 P254 L1 # 225
Palkert, Tom Xilinx/Luxtera

Comment Type T Comment Status A

There is not a clear diagram of the compliance points and the test boards.

SuggestedRemedy

Add diagrams similar to Fig 86-3 showing HCB, MCB and test points.

Response Response Status C

ACCEPT IN PRINCIPLE.
See response comment#168.

Remove TP3 form figure 85-5
2. Refer to mated test fixture illustration for TP-TF in 85-11 for Rx.

Cl 85 SC 85.8.3.5 P254 L10 # 226
Palkert, Tom Xilinx/Luxtera

Comment Type TR Comment Status A

PPI and CR will share a common interface when using the Type 1 connector. Therefore the test fixtures should have the same parameters.

SuggestedRemedy

The test fixture parameters in Annex 86A 5.1.1 should either be duplicated here or referenced.

Response Response Status C

ACCEPT IN PRINCIPLE.
See response to comment #43

Cl 85 SC 85.10.2 P259 L47 # 227
Palkert, Tom Xilinx/Luxtera

Comment Type TR Comment Status D

Cable assembly insertion loss is not consistent with 24.4dB total loss budget

SuggestedRemedy

Change 17.04 to 11

Proposed Response Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

The maximum channel insertion loss is determined using Equation (85A-3). The maximum channel insertion loss is 24.44 dB at 5.15625 GHz (dB) (85A-3) for 50 MHz = f = 6000 MHz.

$ILCh(f) = ILCmax(f) + (2 \times ILHost(f)) - (2 \times ILMatedTF(f))$ (85-A3) where

f is the frequency in MHz.

$ILCamax(f)$ (17.04 dB)>> The maximum cable assembly insertion loss using Equation (85-19) and Table 85-9 coefficients.

$ILHost(f)$ (6.5 dB)>> The maximum insertion loss from TP0 to TP2 or TP3 to TP5 using Equation (85-14).

$ILMatedTF(f)$ (2.8 dB)>> The maximum insertion loss of the mated test fixture using Equation (85-37).

$ILCh(f) = ILCmax(f) = 17.04 + (2 \times 6.5) - (2 \times 2.8) = 24.44$ dB

Cl 85 SC P L # 228
Misek, Brian Avago Technologies

Comment Type T Comment Status A

The rest of the document uses linear frequency for plots of Insertion loss, Return Loss ect. this section does not. It has the tendency to give too much visual weight to the low frequencies.

SuggestedRemedy

All plots of this nature changed to linear frequency.

Response Response Status C

ACCEPT IN PRINCIPLE. [Editor's note: Late comment for consideration by the Task Force] see resolution comment#88

Cl 85A SC 85A.7 P424 L5 # 229
 Misek, Brian Avago Technologies

Comment Type T Comment Status R

The channel, TP0 to TP5 can not have the same ILD as the cable assembly. If we are going to keep with the RL budgets from D2.2 then this number will need to be increased to allow for interactions between the hosts and the cable.

SuggestedRemedy

change the high frequency target from +/-1.7 to +/- 2.3 to account for this effect.

Response Response Status C

REJECT. [Editor's note: Late comment for consideration by the Task Force]
 Response: The commenter has not provided a sufficiently complete proposal in this comment that would enable the implementation of suggested remedy.

Cl 85A SC 85A.8 P424 L9 # 230
 Misek, Brian Avago Technologies

Comment Type T Comment Status A

This whole section seems to be not in sync with methods agreed to in the last meeting and should be expressed in ICN vs channel loss to be consistent with the way the cable is being described and tested.

SuggestedRemedy

Convert to ICN like was done for section 85.10.8

Response Response Status C

ACCEPT IN PRINCIPLE. See response comment#57

Cl 86A SC 86A.4 P431 L27 # 231
 Misek, Brian Avago Technologies

Comment Type T Comment Status A

The inclusion of DDPWS for host Rx testing makes no sense at all to me. I have tried to find the reason behind this inclusion and can not find the rational. In fact I can find no comment or comment response that calls for this in the comments on 2.0 which led to this being inserted as a TBD. The only comment resolution I can find for the value has no technical backing for the number.

This type of jitter, is no more difficult to deal with for an electrical host Rx in a limiting application than jitter induced by ISI behind the limiter function. The inclusion in the spec only serves to make the test harder to create. The test system must have a second Sine generator and wideband noise source, to modulate the amplitude of a signal only to have it clipped with a limiter. I think that burdening the host vendors with this test for no proven benefit is not in the best interest of this group. If there is some proven benefit to this test parameter I would like to see it, which should of been in the record for why it was included. Simultaneous meeting of J2 and J9 can be done in a more straight forward manner with edge modulation by random interference for J9 control(if needed) and the existing ISI for J2 control.

SuggestedRemedy

Remove DDPWS from Table 86A-4
 Remove line 48 components dealing with this
 "sinusoidal interference (SI), and random interference (RI), all"
 Remove line 51 on page 442
 "The test signal at TP4 has DDPWS as defined by Table 86A-4."

Remove Voltage stress block from Figure 86A-9

Remove paragraph at line 11 page 443
 "A voltage stress is to be applied before the limiter function. This stress is composed of a single tone sinusoidal interferer (SI) in the frequency range 100 MHz to 2 GHz and a broadband noise source (RI) with a minimum power spectrum -3 dB point of 6 GHz and minimum crest factor of 7. It is the intent that this combination of voltage stress and limiting function introduce pulse-shrinkage jitter behavior. However no more than 20% of the J2 Jitter is created by the sinusoidal interferer."

Change line 5 page 444 from 80% to 100% and remove the following 2 lines.
 "The sinusoidal interferer amplitude is then turned on and adjusted until the required level of J2 Jitter is achieved. The frequency of any sinusoidal interferer is asynchronous to the characteristic frequencies of the signal."

remove lines 9 to 11 page 444
 "A compliant test signal exhibits Data Dependent Pulse Width Shrinkage (defined in 86A.5.3.4) as specified in Table 86A-4. This is measured with noise and clock-jitter sources turned off."

Remove remove line 15-21 page 444
 "Then the RI (random interference) voltage stress is added until the specified value of J9

Jitter is achieved. If necessary the sine interferer is readjusted to obtain the required level of J2 Jitter and if the sinusoidal interferer is changed then the random interferer is readjusted to obtain the required level of J9 Jitter. Iterative adjustments of the sinusoidal interferer and random interferer are made until the required values of both J2 Jitter and J9 Jitter are achieved."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The DDPWS spec constrains the variety of test stressor eyes that would be allowed if just J2 and J9 specs were in place.

The test configuration shown in figure 86A-9 is an example of a test configuration that could be used to generate a test signal conforming to table 86A-4; In order to make this clearer, change title of figure 86A-9 to "Example jitter tolerance test configuration". Also make the "BT4 7.5 GHz" fit within the box.

[Editor's note: Late comment for consideration by the Task Force]

CI 86A **SC 86A.6** **P446** **L37** # **232**
 Misek, Brian Avago Technologies

Comment Type **T** *Comment Status* **A**

Sign erro in equation 86A-19
 "+ 0.846f" should be "- 0.846f"

SuggestedRemedy

change
 "+ 0.846f" should be "- 0.846f"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
 see comments 44 and 68

[Editor's note: Late comment for consideration by the Task Force]

CI 83A **SC 83A.5.1** **P395** **L16** # **233**
 Misek, Brian Avago Technologies

Comment Type **T** *Comment Status* **R**

In the process of implementing my previous comment about this "off" state I think this is too ambiguous. The off state was agreed to be the state where the Tx equilization could be set to compensate for the comlience point not being at the pins of the package. I don't think the text conveys that clearly.

SuggestedRemedy

Change line 15: from
 "Transmit de-emphasis off state is the optimal setting for transmitter jitter and eye mask evaluation."

""Transmit de-emphasis off state allows for the application of an optimal Tx de-emphasis setting to compensate for the channel present in the transmitter jitter and eye mask evaluation."

Response *Response Status* **C**

REJECT.

Current definition is adequate

[Editor's note: Late comment for consideration by the Task Force]

CI 85 **SC 85.8.3** **P249** **L23** # **234**
 Misek, Brian Avago Technologies

Comment Type **T** *Comment Status* **A**

Collect up the transmit parameters derived from the wave form analysis into the table. They are sprinkled in the text.

SuggestedRemedy

Table 85-4
 Under Transmitted wave form add lines

min amplitude(linear fit), "p"	5.8.3.3	0.24	V	
normalized error(linear fit), "e"	5.8.3.3	0.037		
abs coefficient step size)	5.8.3.3.1	min 0.0083	max 0.05	
minimum precursor fullscale range	85.8.3.3.2	1.54		
minimum post cursor fullscale range	85.8.3.3.2	4		

Response *Response Status* **C**

ACCEPT IN PRINCIPLE. [Editor's note: Late comment for consideration by the Task Force]
 Editor given license to implement suggested remedy with changes to values as approved in other comments.