Synchronizing CRU BW and Jitter Tolerance for 100GBase-LR4/ER4

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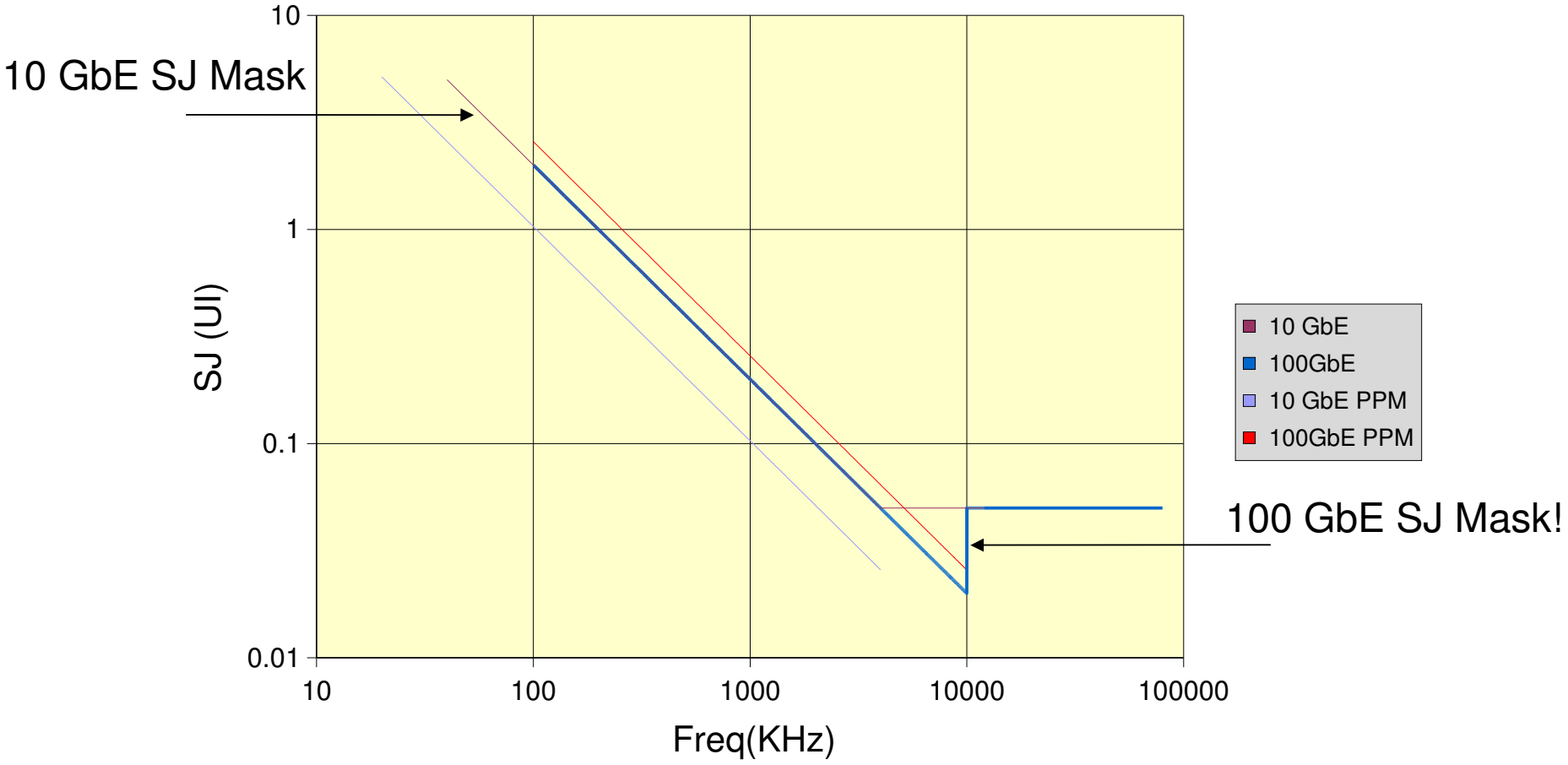
Problem Statement

- 88.8.5.3 Reference Receiver, defines CRU used for TDP measurement has 10 MHz BW
- 88.8.8 Transmitter optical waveform, is defined with CRU with 10 MHz corner frequency
- 88.8.10 Stress receiver sensitivity, table 88-13 effectively defines a 4 MHz CDR corner frequency
- The corner frequency for TDP, transmitter optical waveform, and stress receiver must be the same.
- Current definition allow more stress into the link but the receiver is not fully tested to the maximum SJ stress.
  - With current definition just the +/-100 PPM offset can exceed the SJ tolerance mask.

10 GbE/100GbE Jitter Tolerance Masks

- **Current 100 GbE mask is broken and even the PPM offset exceeds the mask**

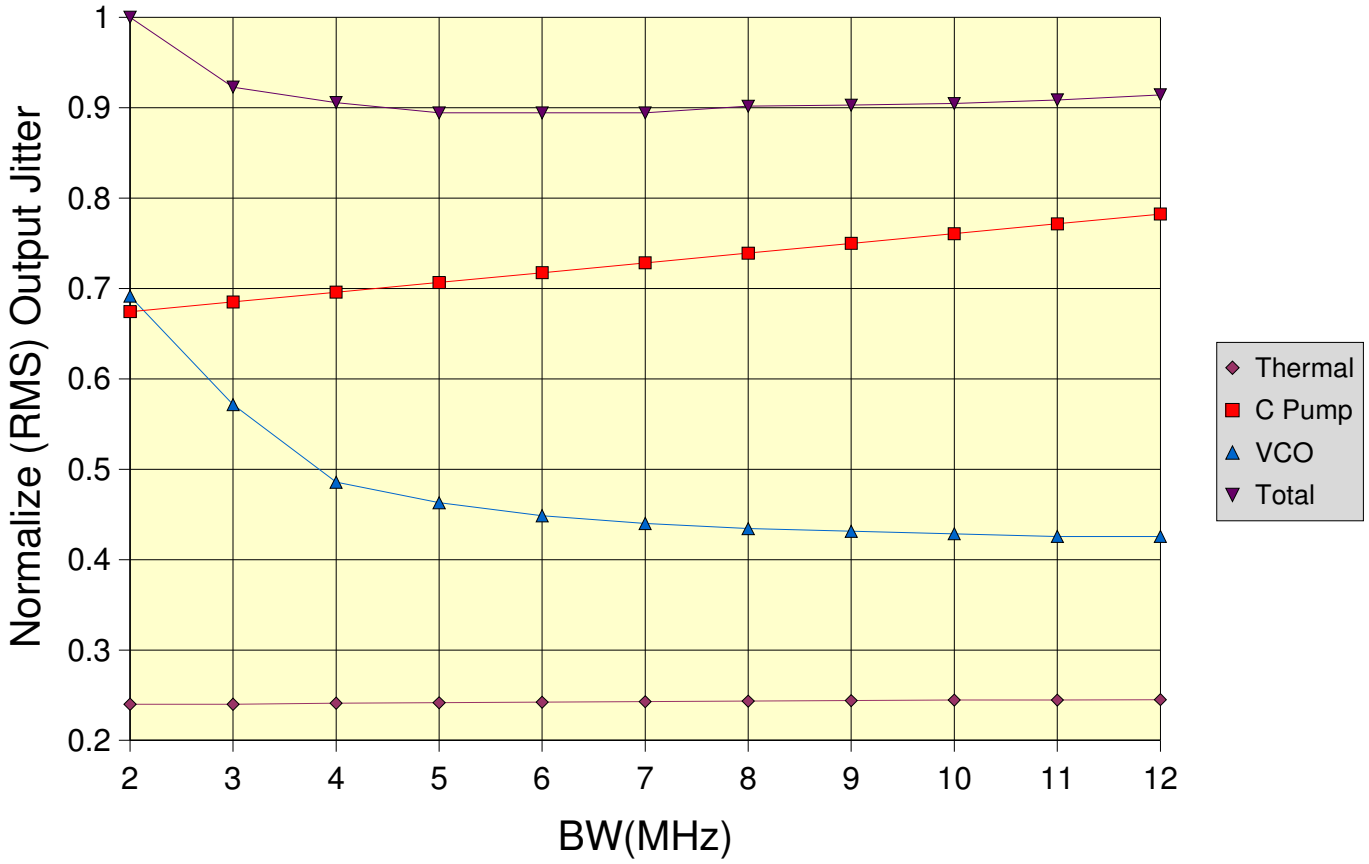


Options For Moving Forward

- **The current specifications is clearly broken!**
- **What are the options**
  - **Use 10 GbE mask with 4 MHz corner frequency for transmitter CRU and jitter tolerance, “4 MHz Option”**
  - **Change table 88-13 2x10^5 coefficient with 5x10^5, “10 MHz option”**
  - **Take a compromise position with 7 MHz corner frequency for the CRU and jitter tolerance, “7 MHz option”**
    - **Lowest transmitter jitter was for BW of 5 to 7 MHz**

SerDes Transmitter Relative Jitter

- **Thermal, charge pump, VCO, and total relative output jitter as function of BW**
  - **BW of 5-7 MHz gives best total output jitter**



Pro and Cons of the 4 MHz CRU

- **Pro**
  - **More flexible SerDes receiver implementations**
  - **Will not impact existing SerDes receiver or test equipments designed with 4 MHz BW**
- **Cons**
  - **Reducing the CRU BW from 10 MHz to 4 MHz could increase SerDes transmitter output jitter slightly**

Pro and Cons of the 10 MHz CRU

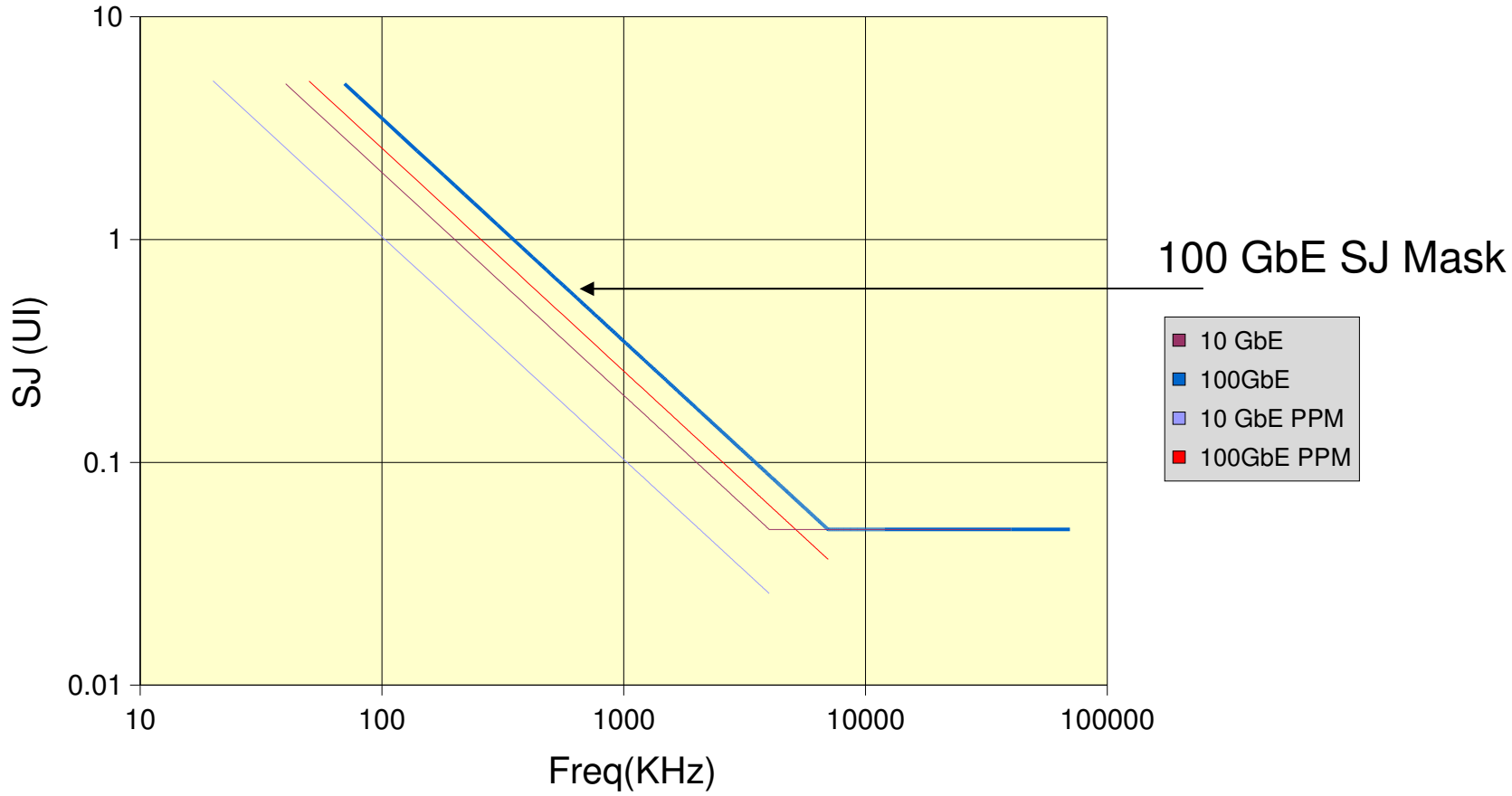
- **Pro**
  - **No real good reason**
    - **It is foreseeable under some circumstances transmitter to have slightly lower jitter with 10 MHz CRU BW but not the case in our simulation**
- **Cons**
  - **Increases SerDes transmitter jitter slightly**
  - **Would eliminated lower cost, power, digital CDR implementation as the loop has to operate 2.5x faster than current 10G SerDes**
    - **It will burden future 4x25G electrical interface and ASICs**

Pro and Cons of the 7 MHz CRU

- **Pro**
  - **Allows lower cost and power digital CDR implementation by increasing the loop BW by 75% over 10 GbE implementation instead of 250%!**
  - **Simulation results show 5-7 MHz BW results in lowest output jitter**
  - **Share pain between transmitter and receiver**
- **Cons**
  - **No real concern**
    - **It is foreseeable under some circumstances transmitter to have slightly lower jitter with 10 MHz CRU BW but not the case for our simulation**

10 GbE SJ Mask and Proposed 100 GbE Mask

- **100 GbE mask with proposed compromised 7 GHz BW**



Summary

- The combination of current CRU+SJ specifications is busted and must be changed!
- The 7 MHz CRU and SJ corner frequency is a compromise between the current 10 MHz CRU BW and 4 MHz SJ corner frequency
  - 5-7 MHz BW results in the lowest output jitter
  - SJ corner frequency of <=7 MHz allow lower cost and power de-serializer options
- Proposed resolution assuming 7 MHz for CRU and SJ corner frequency
  - Change 88.8.5.3 and 88.8.8 CRU BW from 10 MHz to 7 MHz
  - Change 88.8.10 SJ corner frequency from 4 MHz to 7 MHz
    - f<70 KHz $\Rightarrow$ not specified
    - 70 KHz $\leq$ f $\leq$ 7 MHz $\Rightarrow$ 3.5x10^5/f + s – 0.05
    - 7 MHz < f <10 LB $\Rightarrow$ 0.05 $\leq$ S $\leq$ 0.15