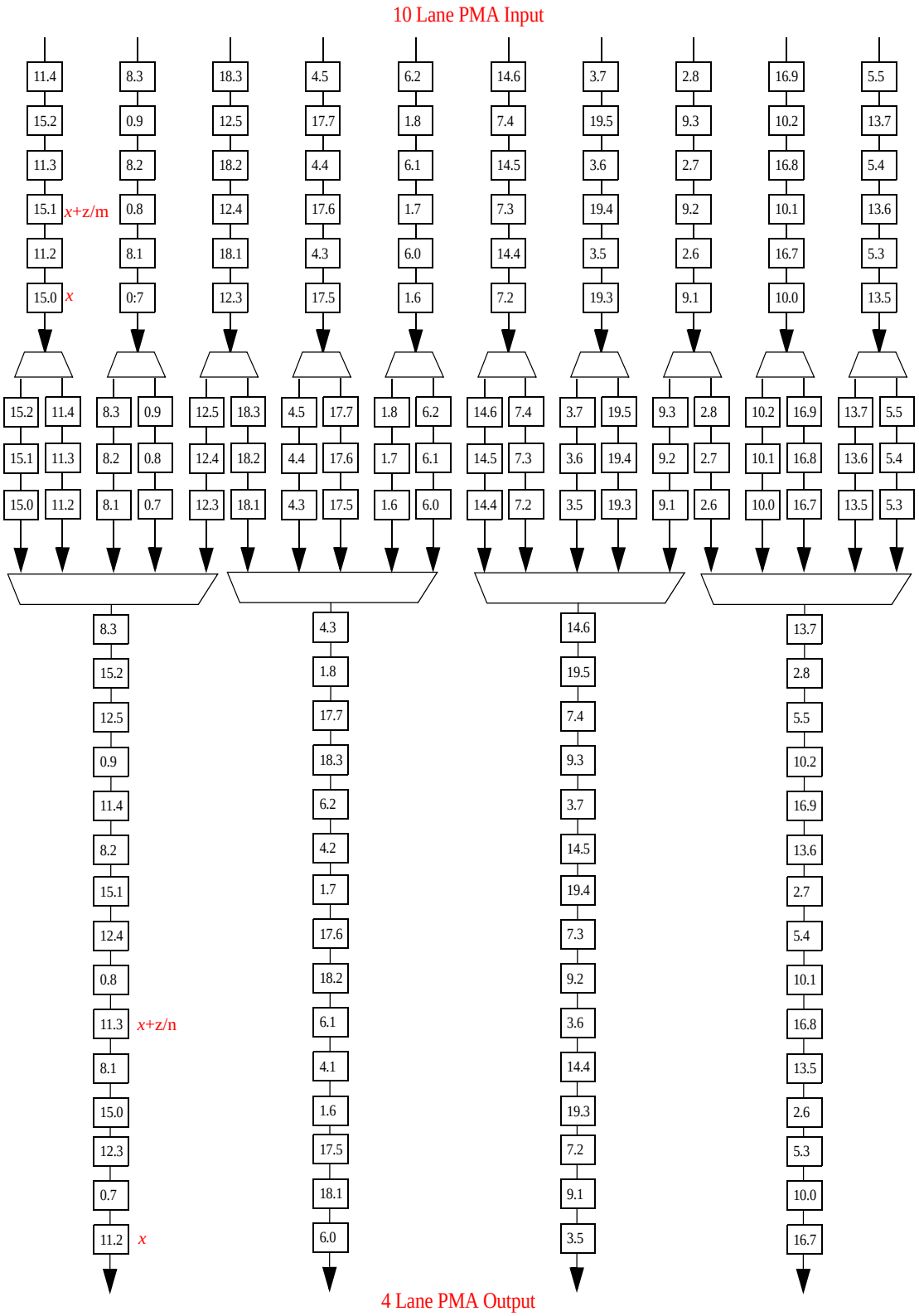
tives (for PMA client lanes *i*=0 to p-1) with the result sent to the service interface below the PMA using the *inst*:IS_UNITDATA_*i*.request primitives (for service interface lanes *i*=0 to q-1), referencing the functional block diagram shown in Figure 83–5. The bit multiplexing behavior is illustrated in Figure 83–4.

The aggregate signal carried by the group of input lanes or the group of output lanes is arranged as a set of PCSLs. For PMA sublayers supporting 40GBASE-R interfaces, the number of PCSLs z is 4, and the nominal signaling rate R of each PCSL is 10.3125 GBd. For PMA sublayers supporting 100GBASE-R interfaces, the number of PCSLs z is 20, and the nominal signaling rate R of each PCSL is 5.15625 GBd.

For a PMA with m input lanes (TX or RX direction), each input lane carries, bit multiplexed, z/m PCSLs. Each input lane has a nominal signaling rate of R × z/m. If bit *x* received on an input lane belongs to a particular PCSL, the next bit of that same PCSL is received on the same input lane at bit position *x*+(z/m). ~~If the input lane carries more than one PCSL, bit position *x*+1 belongs to another PCSL, and bit *x*+1+(z/*m*) is the next bit from that same PCSL~~. The z/m PCSLs may arrive in any sequence on a given input lane.

For a PMA with n output lanes (TX or RX direction), each output lane carries, bit multiplexed, z/n PCSLs. Each output lane has a nominal signaling rate of R × z/n. Each PCSL is mapped from a position in the sequence on one of the z/m input lanes to a position in the sequence on one of the z/n output lanes. If bit *x* sent on an output lane belongs to a particular PCSL, the next bit of that same PCSL is sent on the same output lane at bit position *x*+(z/n). The PMA shall maintain the chosen sequence of PCSLs on all output lanes while it is receiving a valid stream of bits on all input lanes.

Each PCSL received in any temporal position on an input lane is transferred into a temporal position on an output lane. As the PCS (see Clause 82) has fully flexible receive logic, an implementation is free to perform the mapping of PCSLs from input lanes to output lanes without constraint. ~~From the time the link is brought up, the mapping of each PCSL from an input lane to a particular output lane shall be maintained.~~ Figure 83–6 illustrates one possible bit ordering for a 10:4 PMA bit mux. Other bit orderings are also valid.



NOTE: i.k indicates bit ~~i~~k on PCSL ~~k~~i. Skew may exist between PCSLs.

Figure 83–6—Example 10:4 PMA bit mux