

Title: Package Model Update with 40GHz data

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Abstract: Package models previously proposed on December 2007 are updated with up to 40GHz data to provide a sufficient frequency data bandwidth for 25 to 28Gbps signaling analysis.

Agenda

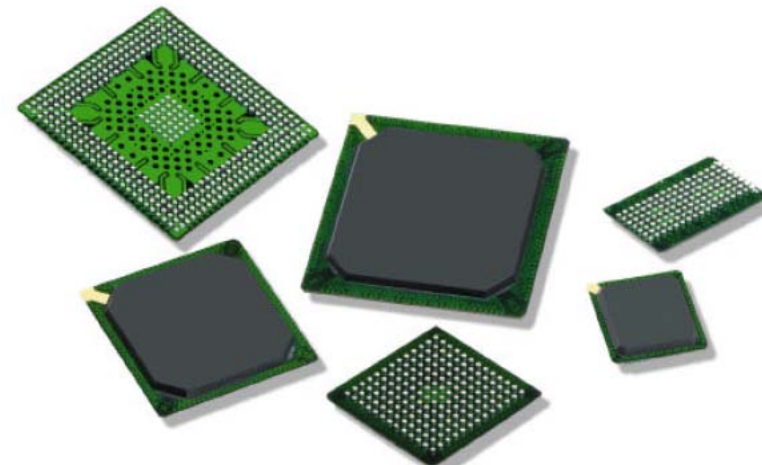
- High speed packaging and modeling challenges
- Package behaviors in measured S-parameters
- Package behavior in existing IEEE package models
- 3D EM modeling of package structures
- New models proposed (Dec 1007, 20GHz)
- Models updated with 40GHz data (Mar 10, 2008)

High speed packaging and modeling challenges

- Greater impact of high frequency package behavior on signal integrity of Multi-Gbps and up
 - Various discontinuity components exist in package signal path and impact package behavior at high frequencies
 - **Using real world package model with high frequency well characterized is critical to reasonable channel analysis and realization**
 - **3D package modeling vital to capturing accurate high frequency behavior**
- Manufacturing process and environmental factors to high frequency performance
 - Process variation; impedance tolerance
 - Surface roughness – higher loss at high frequencies
 - Material loss – higher loss factor at high frequencies
 - Temperature/humidity effect on high frequency loss
- Design factors for performance as cost-performance tradeoff
 - Design development for high frequency performance improvement
 - Signal behavior is affected by wiring scheme associated with wiring density
 - Impedance control along discontinuity paths

Packaging for ASIC high speed applications

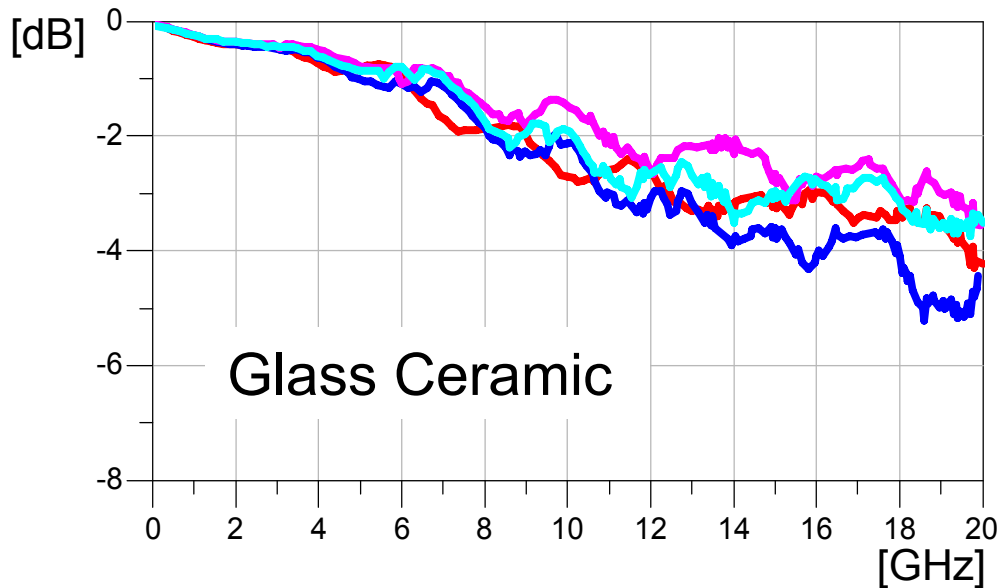
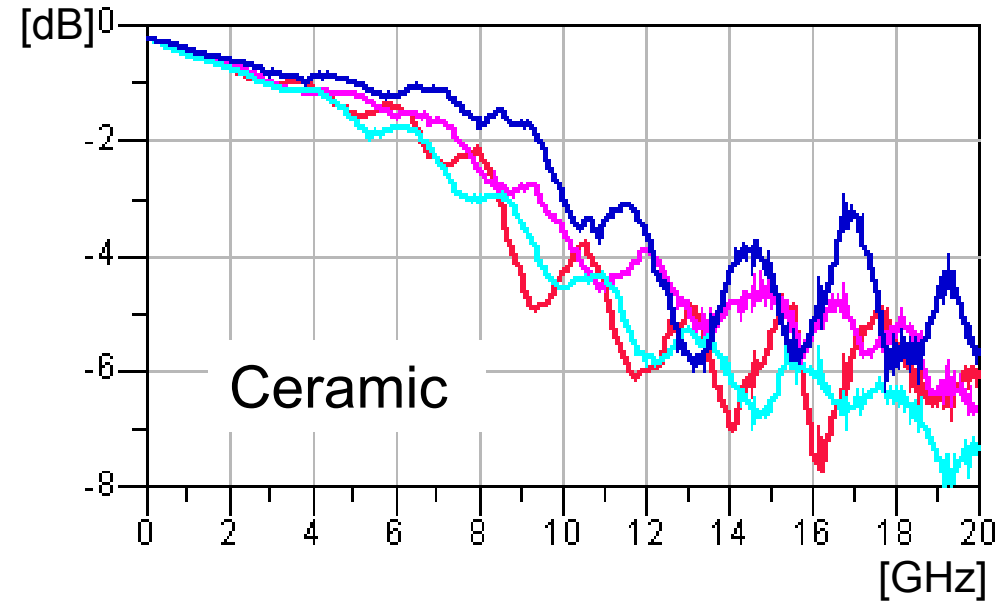
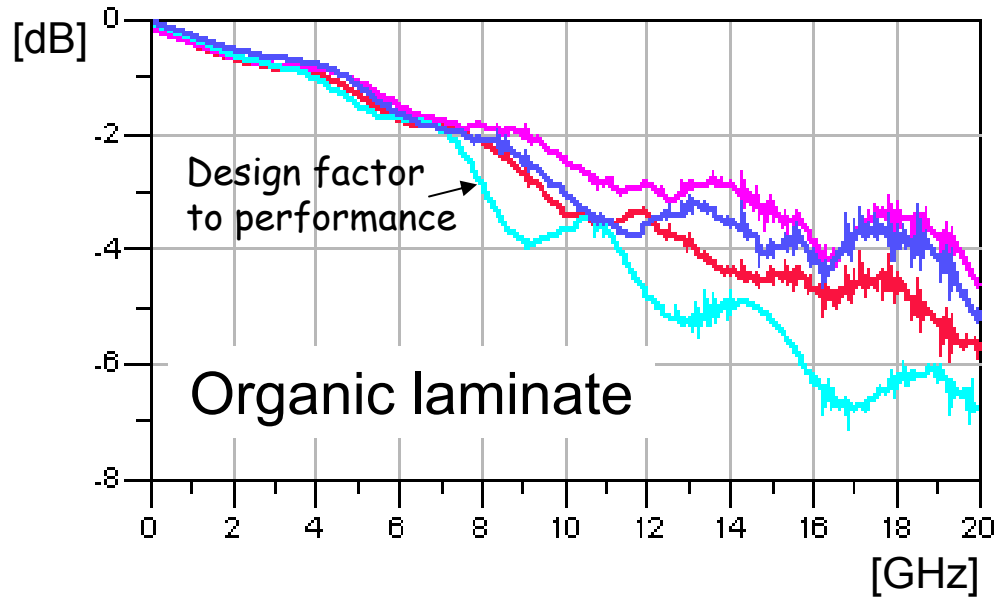
- Cost-performance as primary factor for package selection in average ASIC networking market space
 - Increasing bandwidth demand: link density to noise isolation
 - Package size-layer count versus loss-coupling
- **Organic laminates are prevailingly popular with its cost-performance effectiveness** – matured technology
 - Various with layer build-up construction technologies; thin core/thick core/coreless
 - limited layer count but high wiring density per layer enabled by low dielectric constant with manufacturing technology advancement
 - Relatively lossy material
- Ceramic – matured technology
 - Excellent reliability and low loss material
 - Poor cost-performance competitiveness
 - Shrinking application space
- Other packaging developments for general ASIC networking applications
 - Process/material NOT developed or matured to make performance leap in any visible future



Package high frequency behavior characterized in measured S-parameters and TDR waveforms

- Measurements on actual product packages of a high speed link application
- Compared with existing IEEE package models for real package responses

Insertion loss measured on 35mm packages

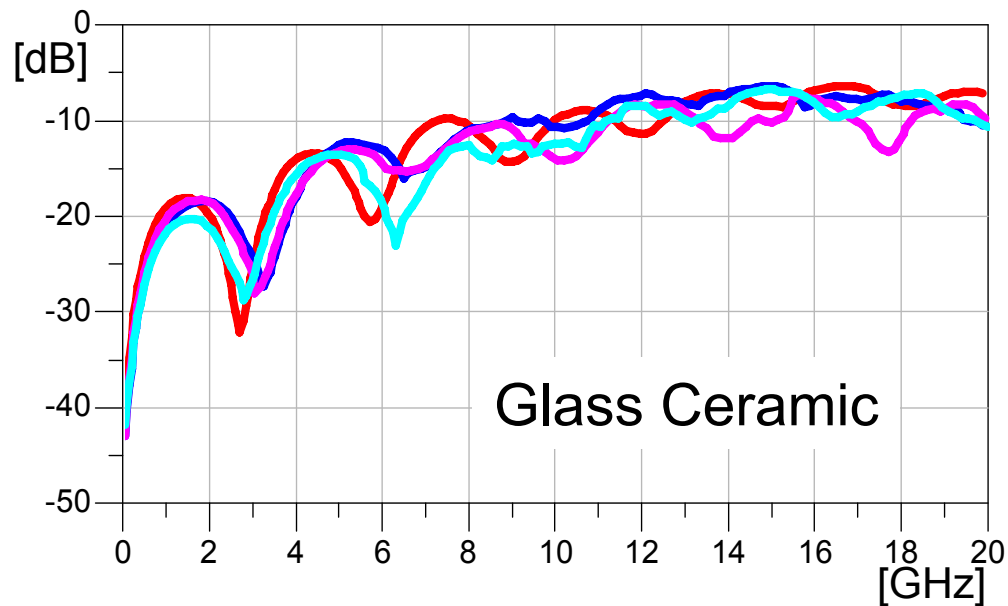
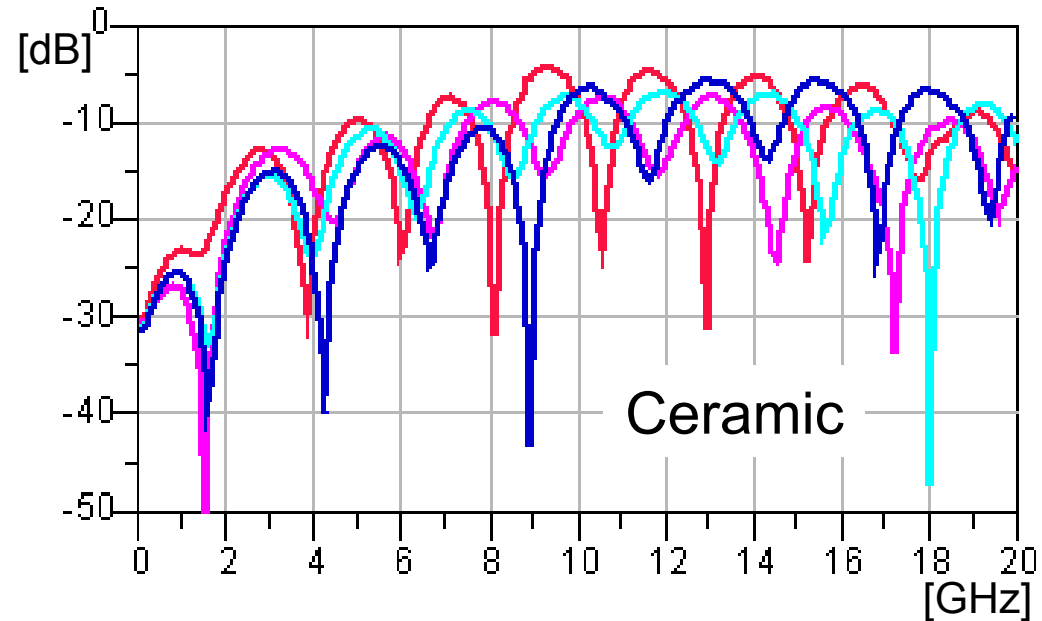
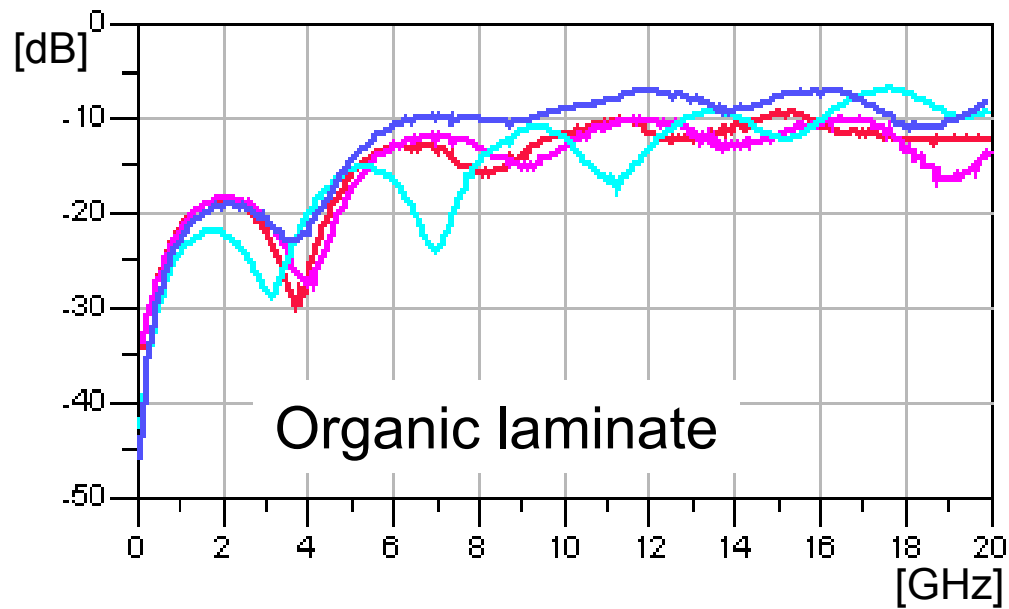


Differential insertion loss displayed

Various design nets measured in each package

Transmission varies with trace length, routing via configuration and reflection of the structure (next slide)

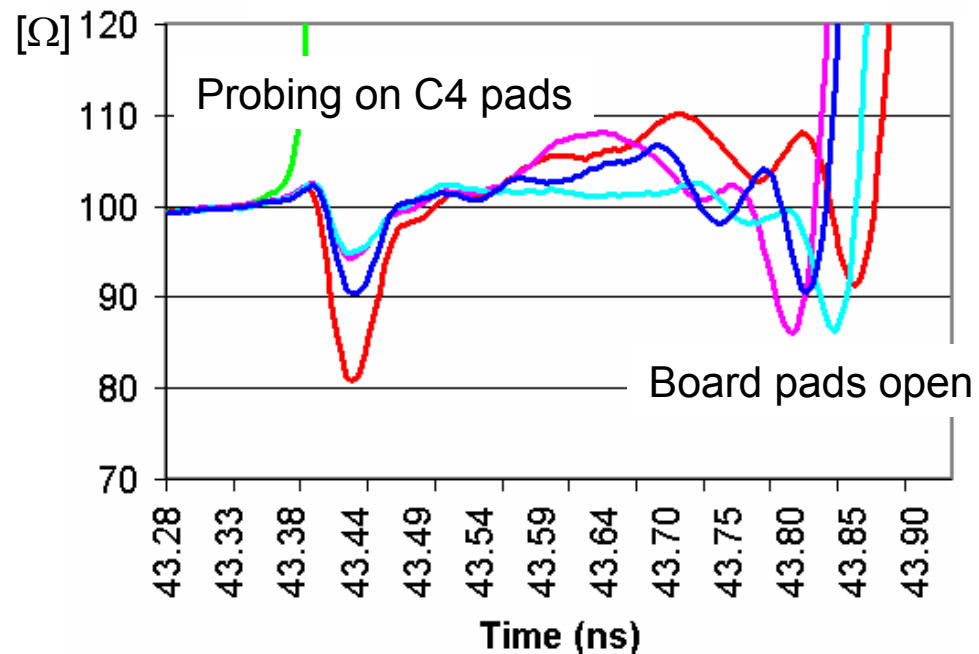
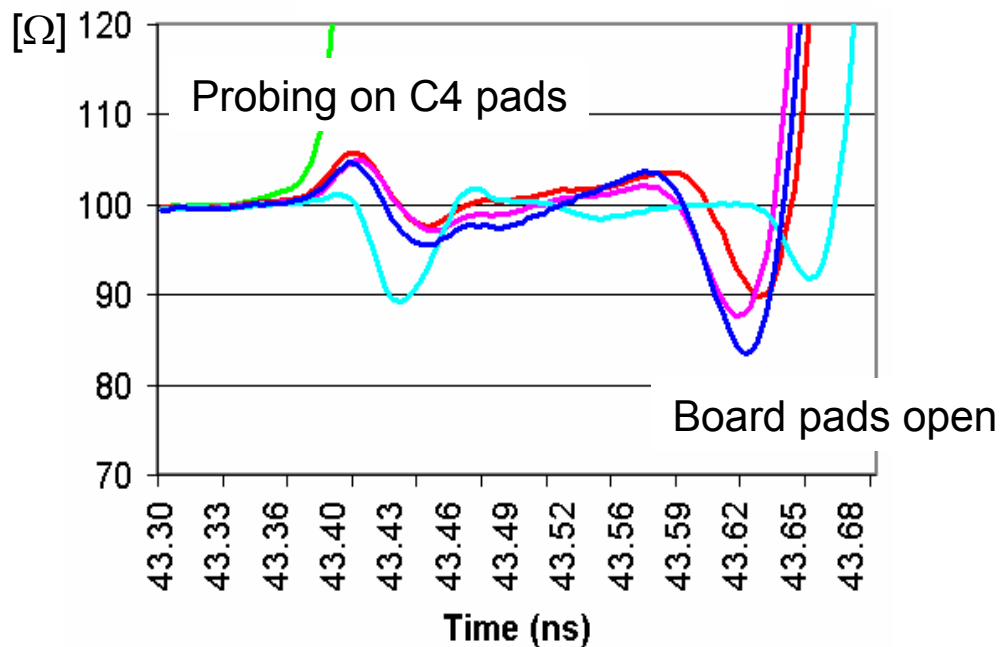
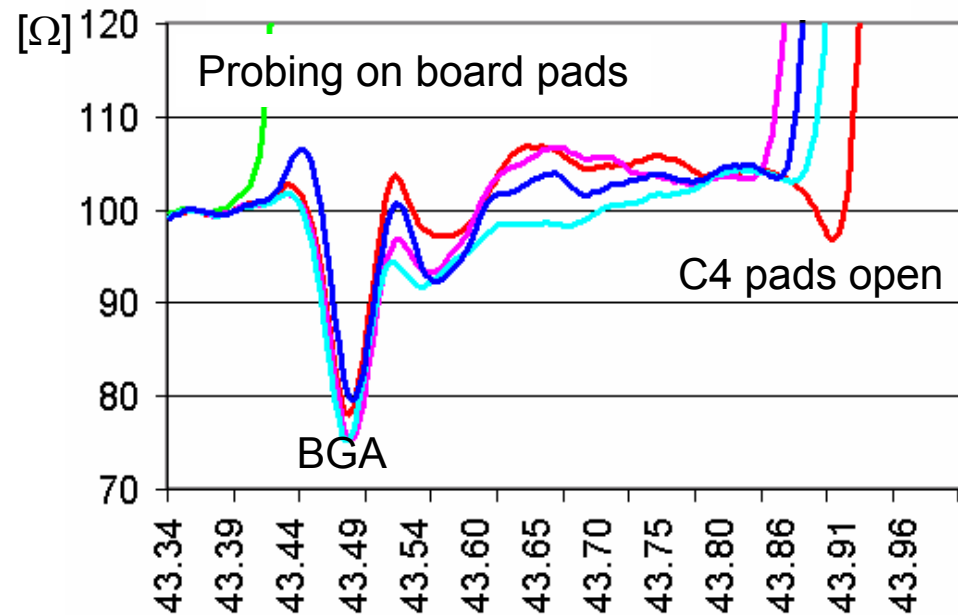
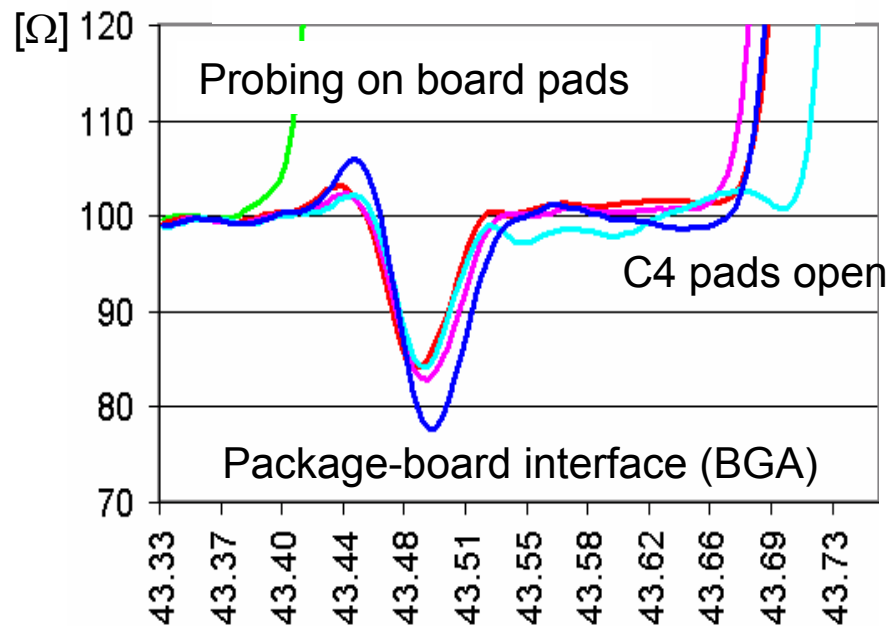
Return loss measured on 35mm packages



Differential return loss displayed

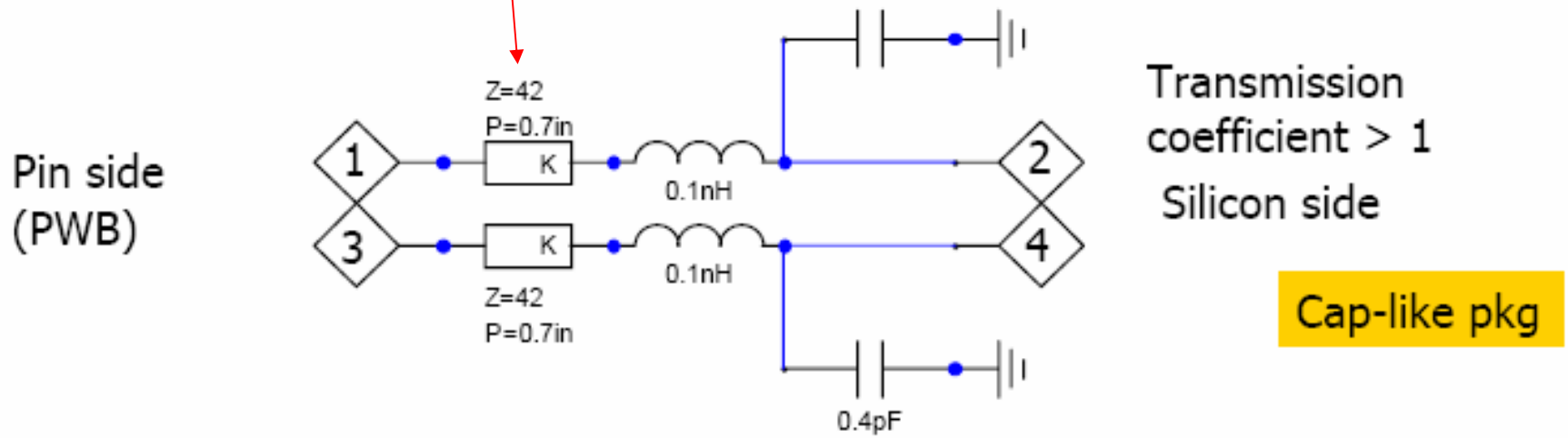
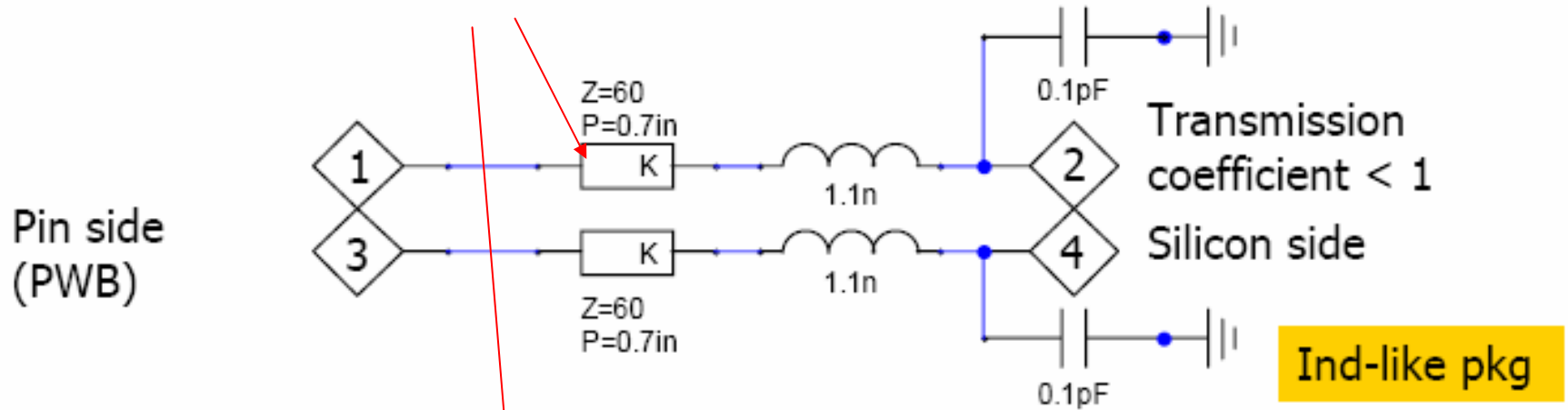
Reflection pattern differs with routing paths/configurations in each package

Package discontinuities in measured TDR waveforms



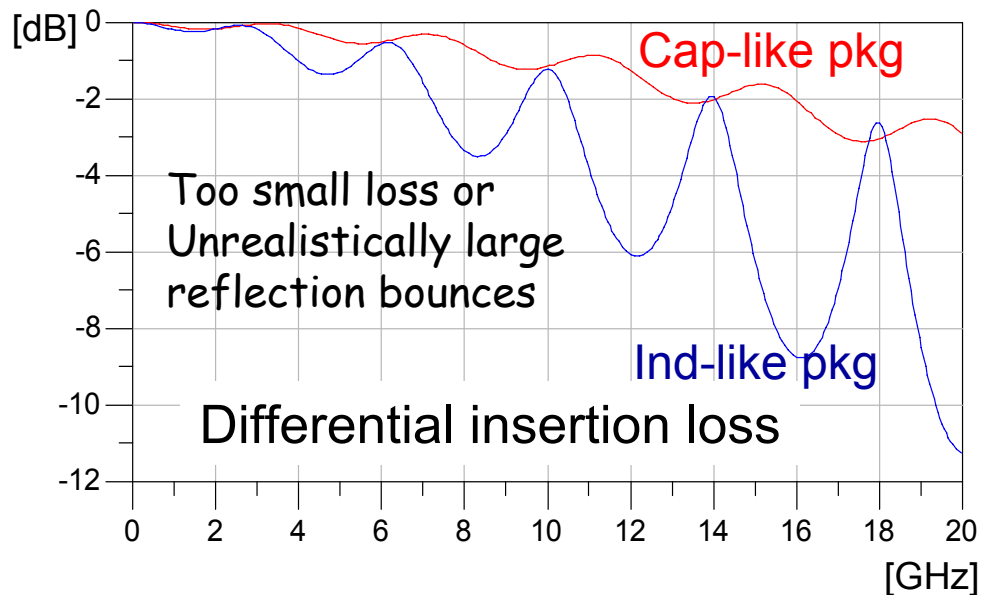
Existing IEEE package models

Lossless transmission line??



*product packages are lossy.

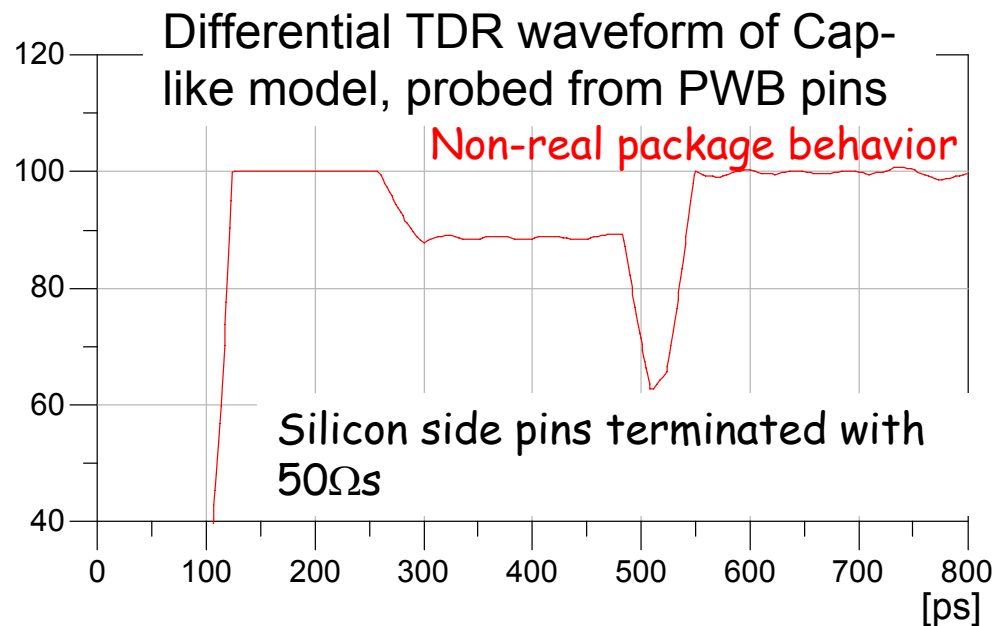
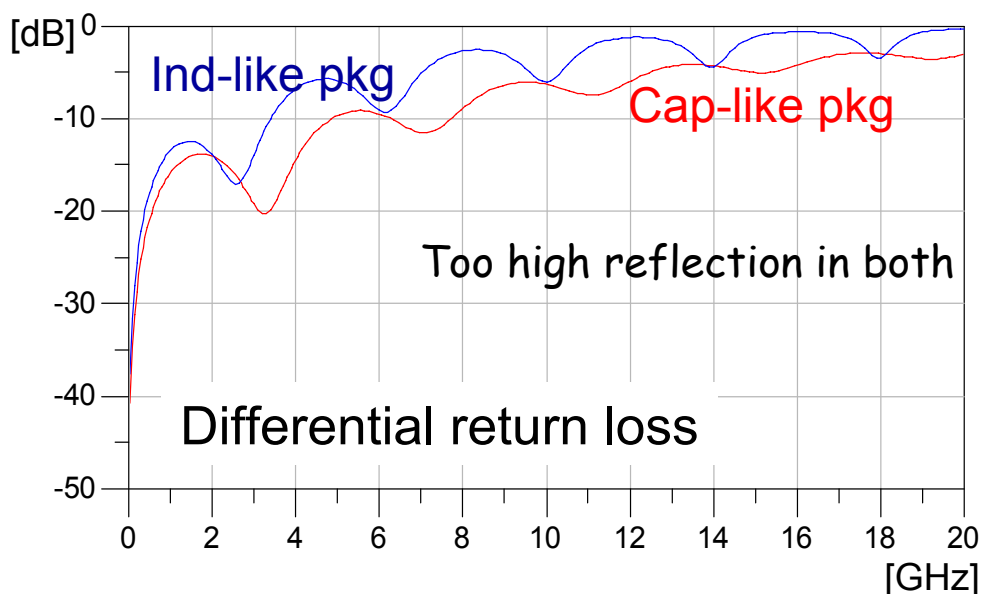
Non-representative package behavior of IEEE models



Modeled using lossless transmission lines (??) while physical packages are lossy.

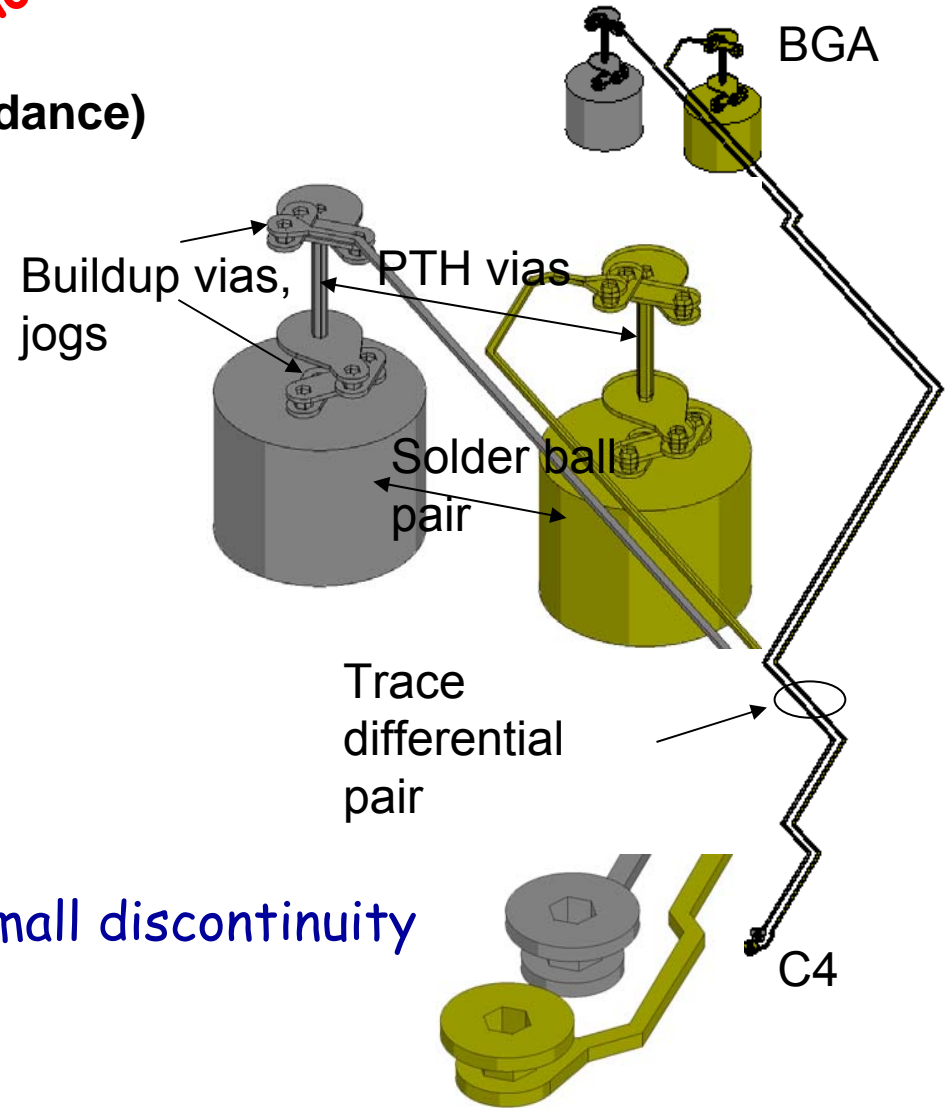
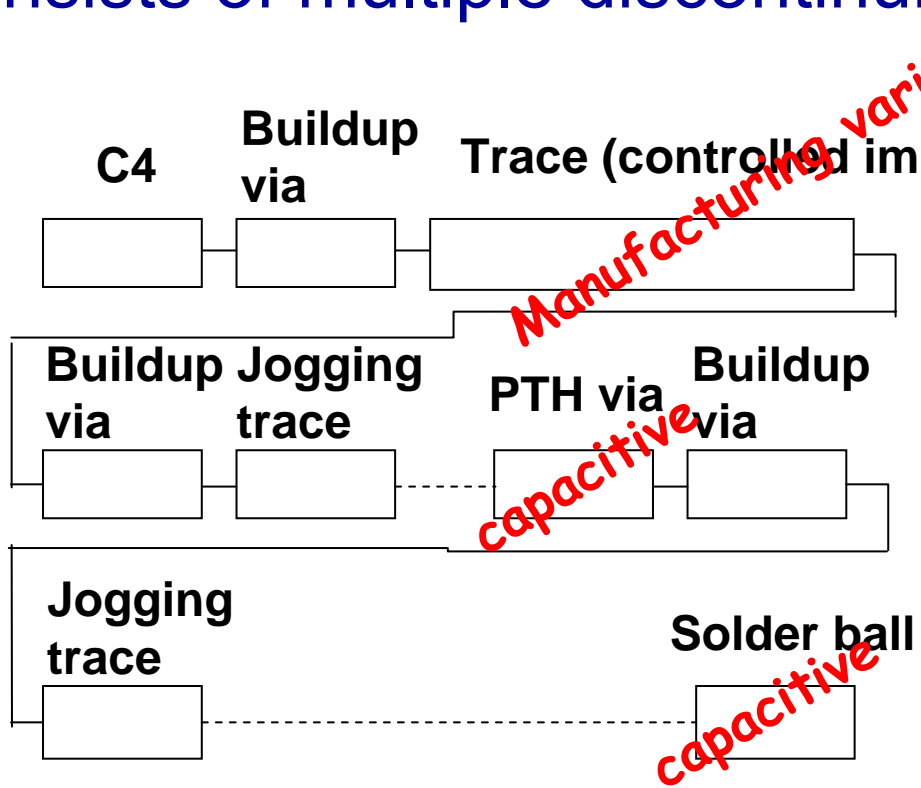
Extremely exotic behavior of inductor-like package model which is not plausible in real packages.

Too high return loss in both models



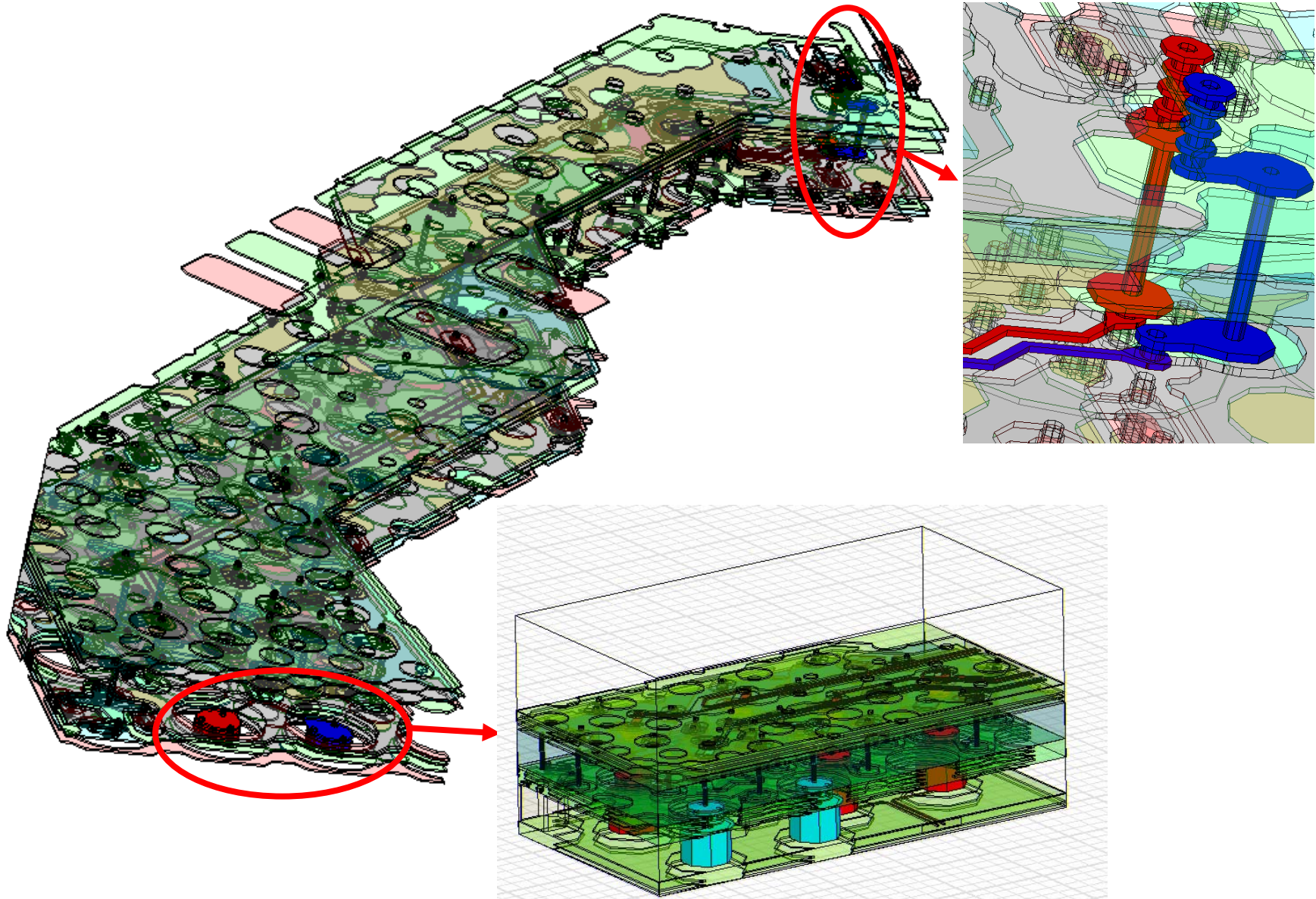
3D electromagnetic modeling can capture high frequency behavior of package physical structures with multiple discontinuities

Typical signal path in organic flip-chip BGA packages consists of multiple discontinuities



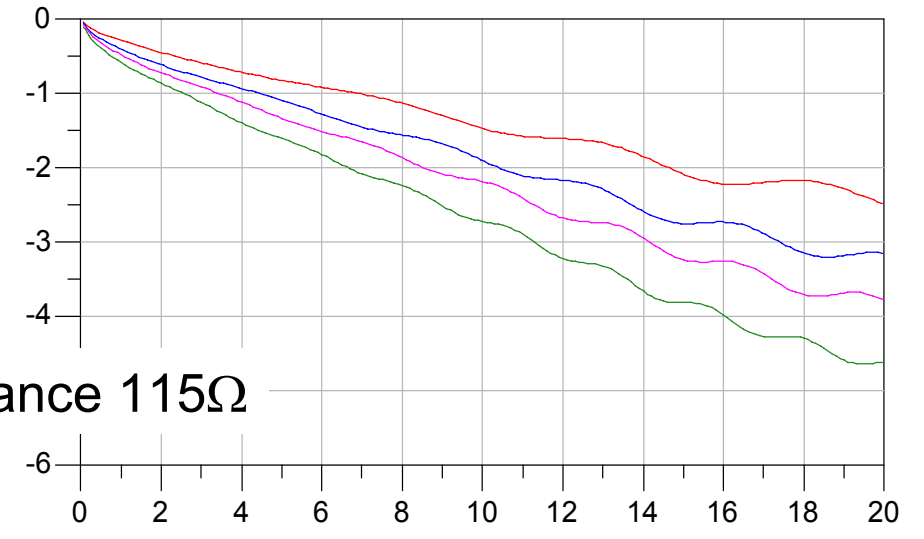
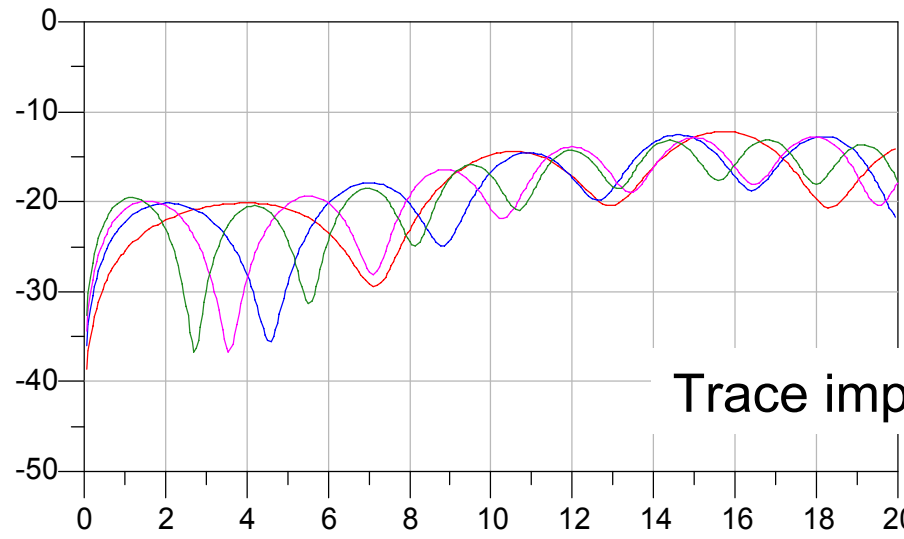
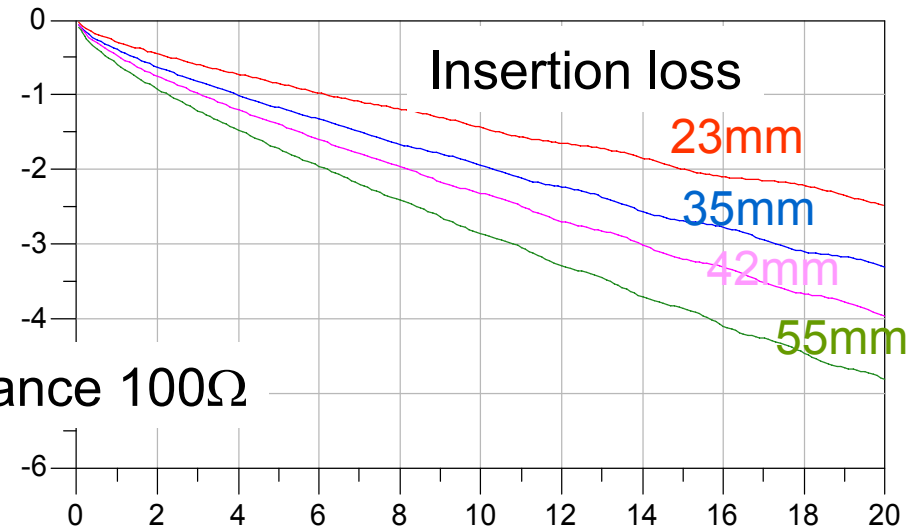
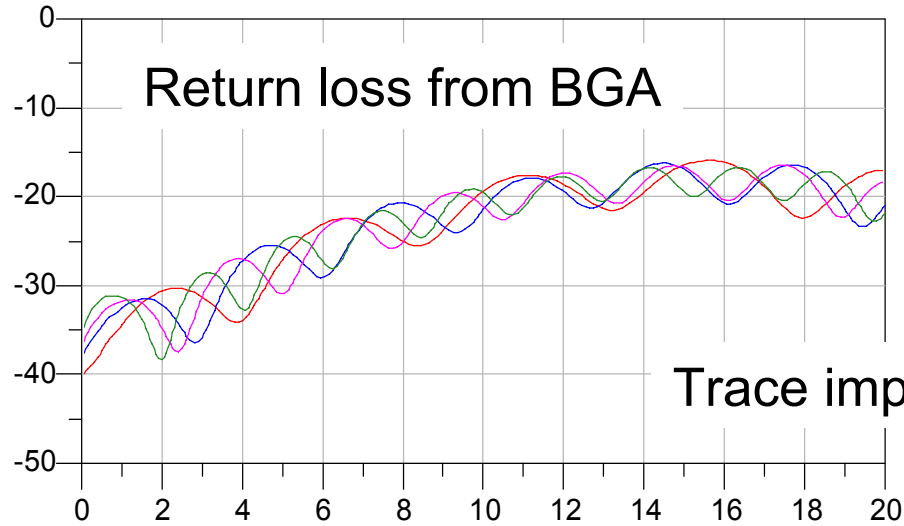
Each transition introduces large or small discontinuity and adds reflection and loss

3D EM modeling captures high frequency behavior of physical structures



Package loss increases with size: 23/35/42/55mm

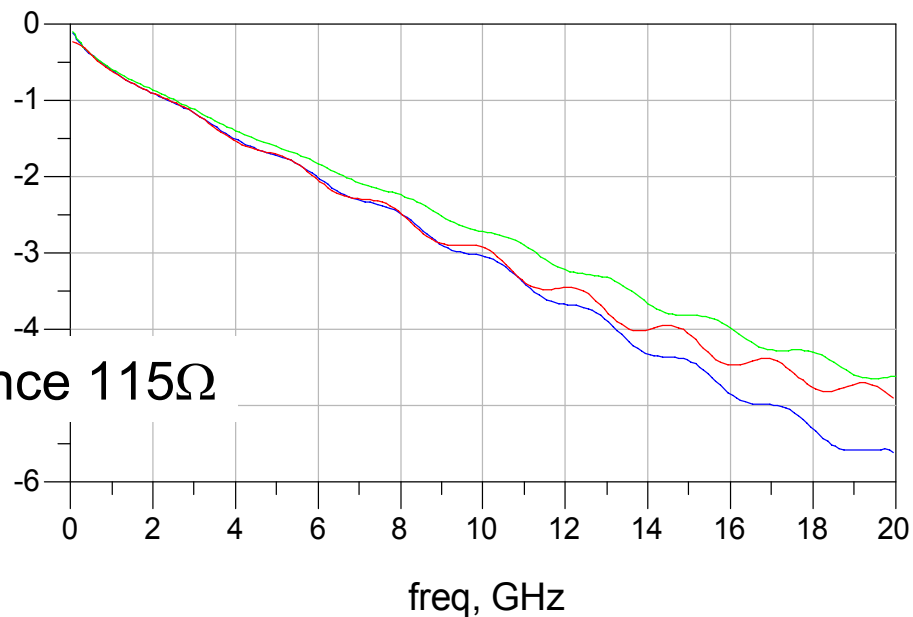
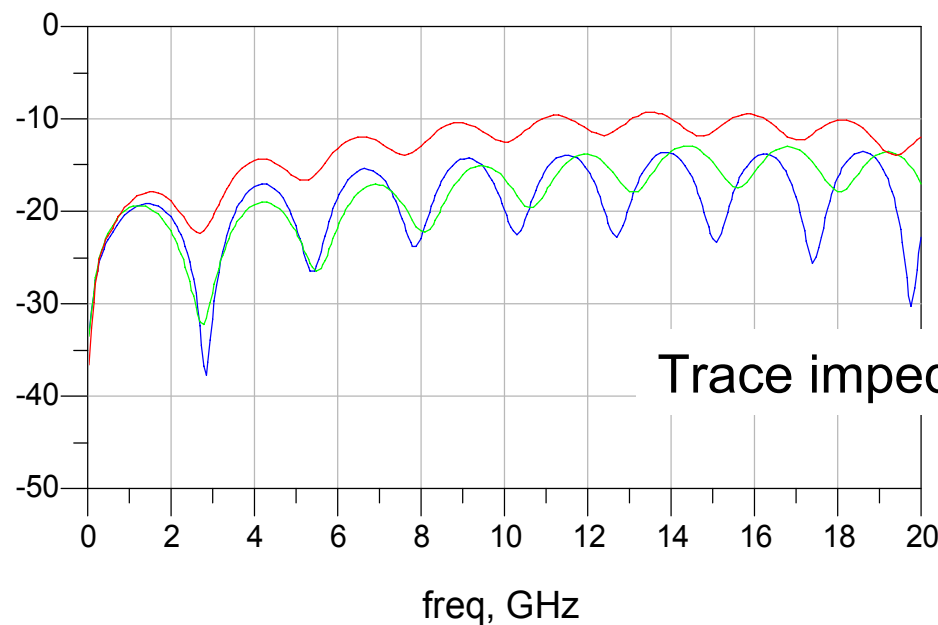
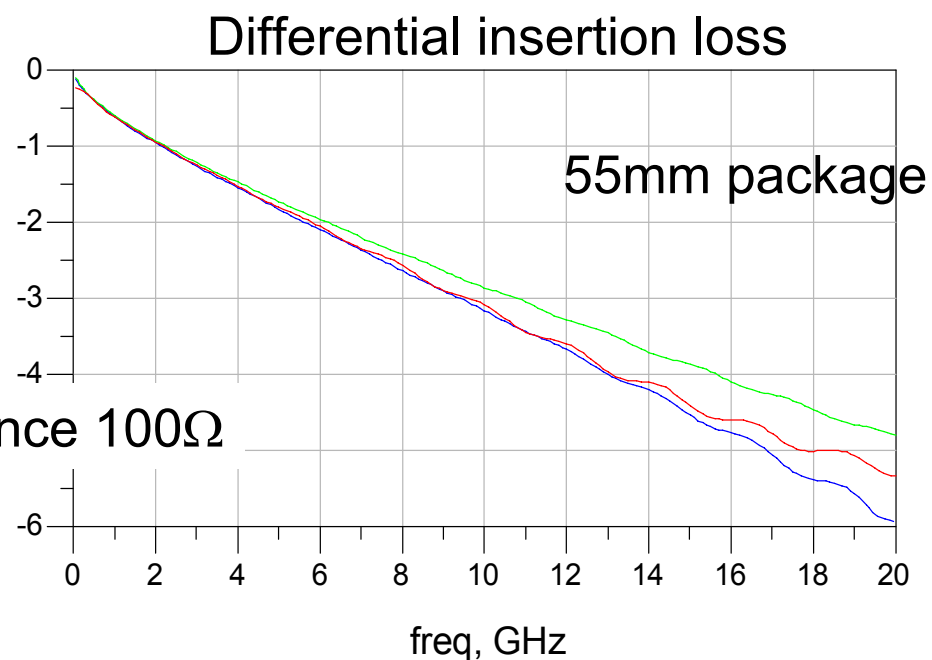
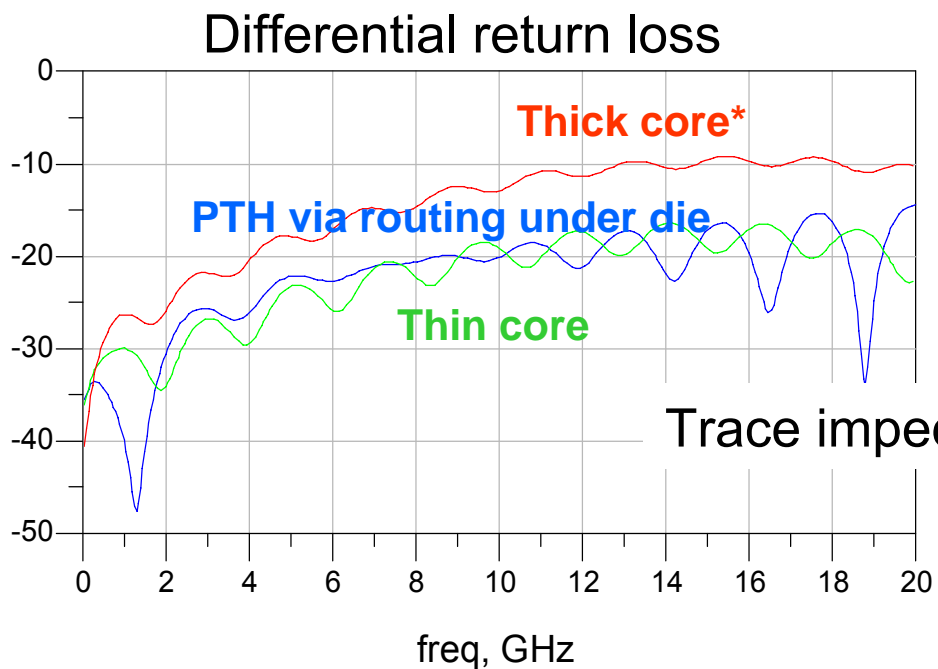
Up to **55mm** by JEDEC standard for BGA package
 Longer interconnect assumed for larger package size



freq, GHz

freq, GHz

Performance varies with design and physical layer construction

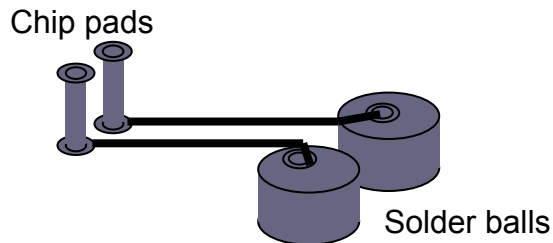


Performance varies with routing scheme/design strategy

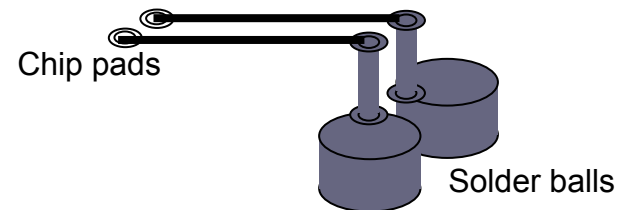
There is design trade-off in wiring density-performance

High performance design option is preferable for high speed data transmission.

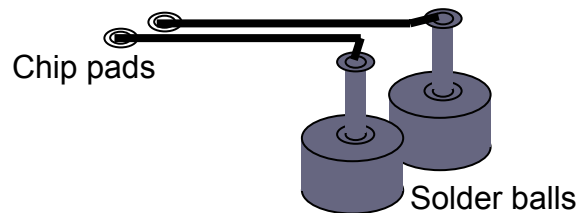
(1) Small PTH via pitch under die



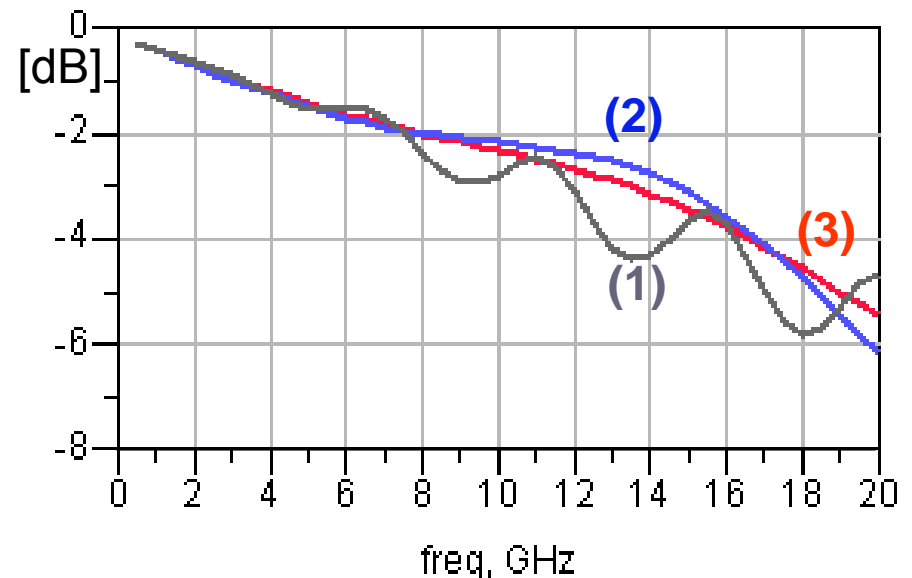
(2) Small PTH via pitch above BGA



(3) PTH vias aligned with BGA



Differential insertion loss

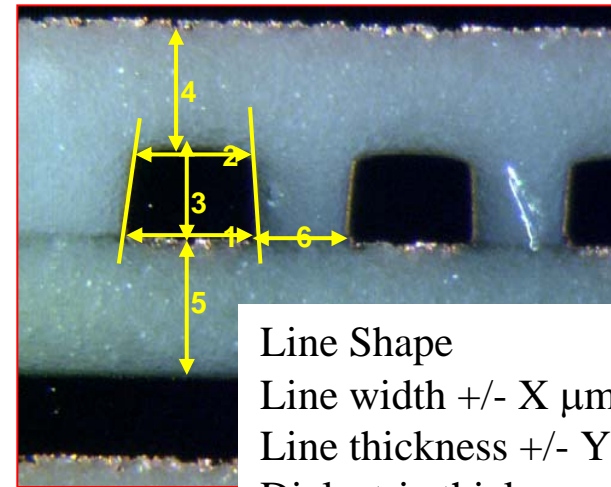


Ref: Nanju Na et. al., "Discontinuity impacts and design considerations of high speed differential signals in FC-PBGA packages with high wiring density", IEEE 14th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 107-110, Austin, Texas, Oct. 24-26, 2005.

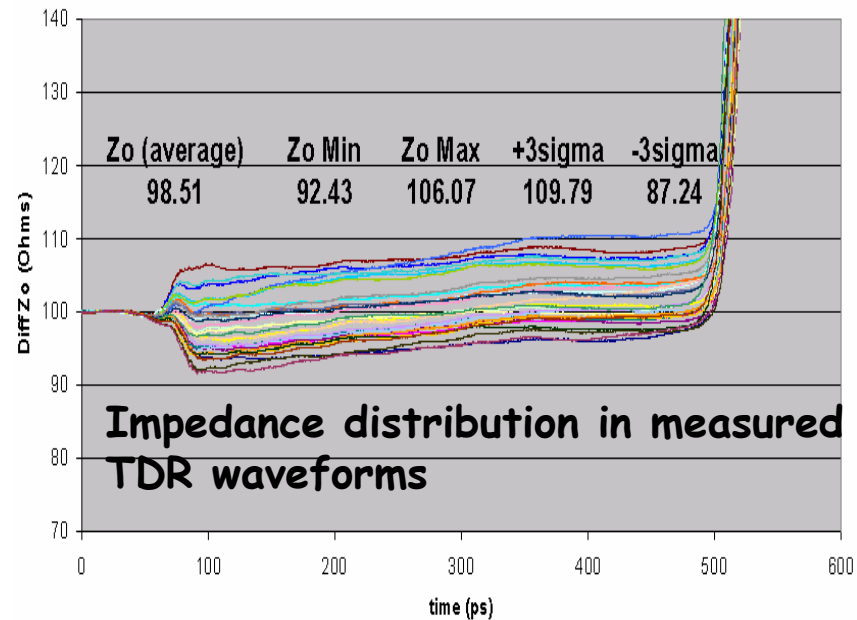
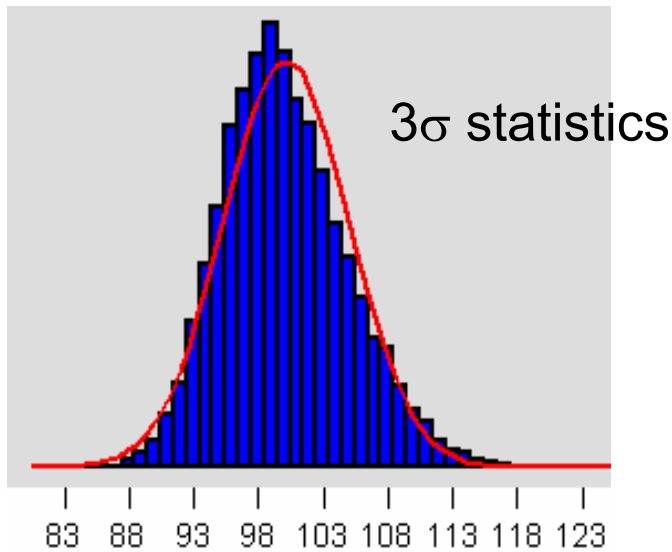
Impedance tolerance 15% is achievable

Design target impedance of differential pairs is 100Ω .

$\pm 15\%$ impedance variation after manufacturing is manageable with current packaging technology $\rightarrow 85\Omega$ to 115Ω at 3σ distribution



Line Shape
 Line width +/- X μm
 Line thickness +/- Y μm
 Dielectric thickness +/- Z μm

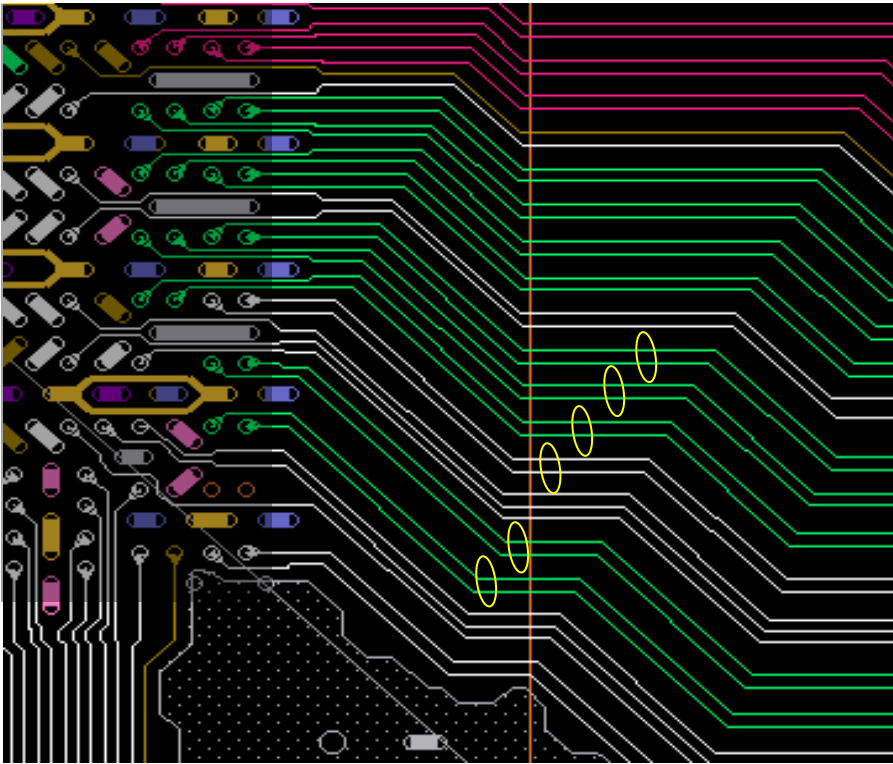


Ref: Jean Audet et. al, "Manufacturing Impedance Tolerance Control for High Speed Data Link Applications", IEEE 56th Electronic Components and Technology Conference, pp. 1023-1028, 2006.

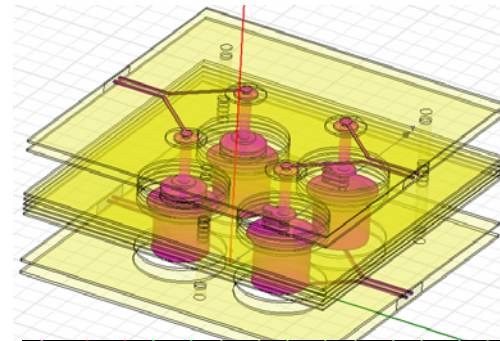
Package coupling cannot be ignored in moderate to high density packages and needs to be considered in channel analysis

Package coupling as part of package behavior

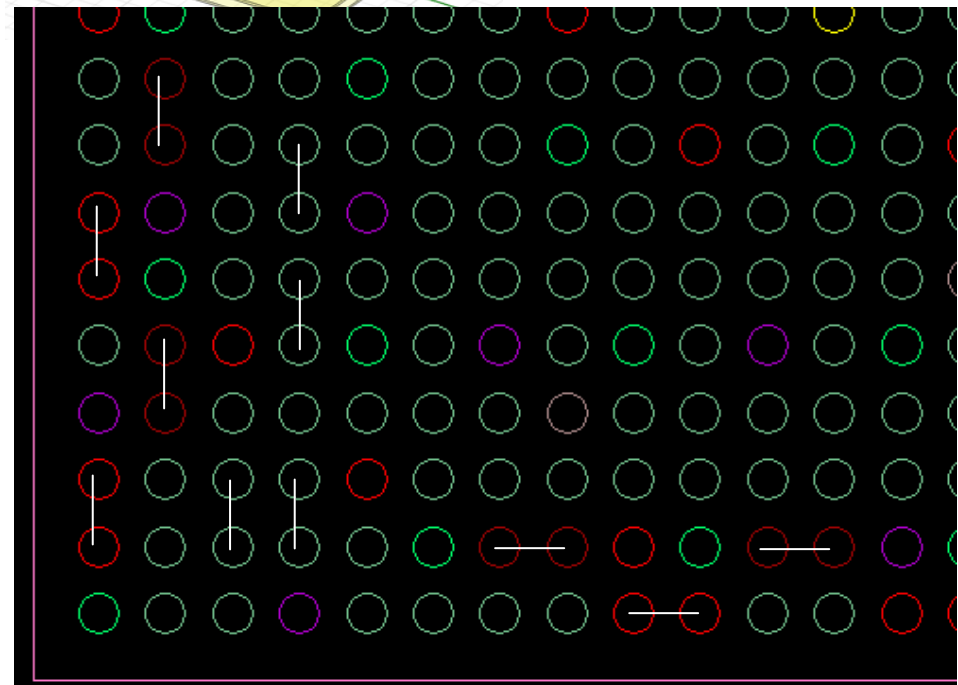
Wiring density-isolation is an ASIC cost-performance factor



Trace coupling involved in moderate to high package wiring density, moderately manageable



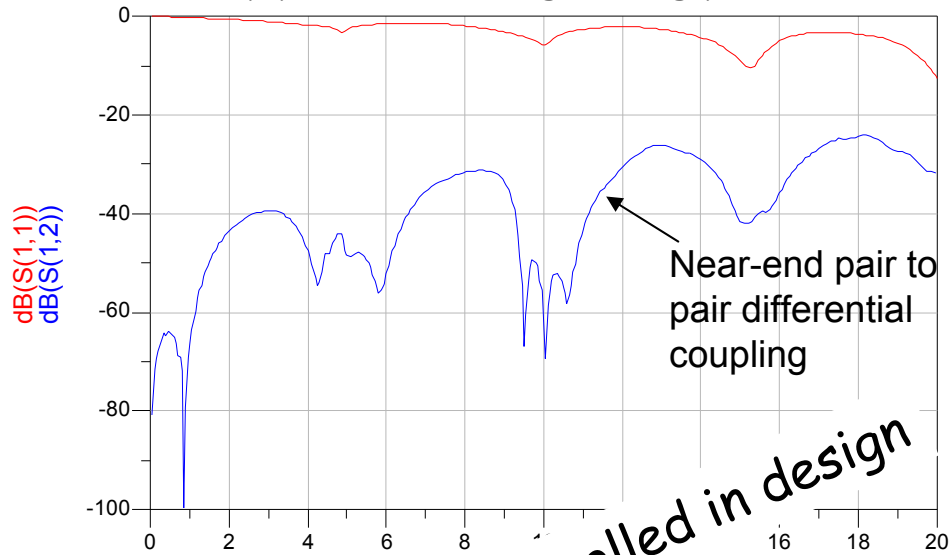
PTH via/ BGA coupling factor to BGA assignments - package size



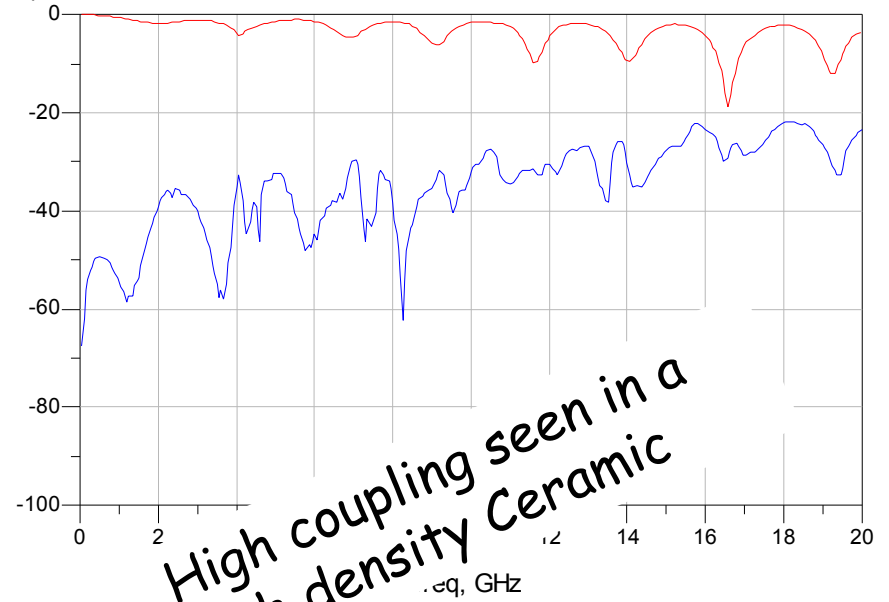
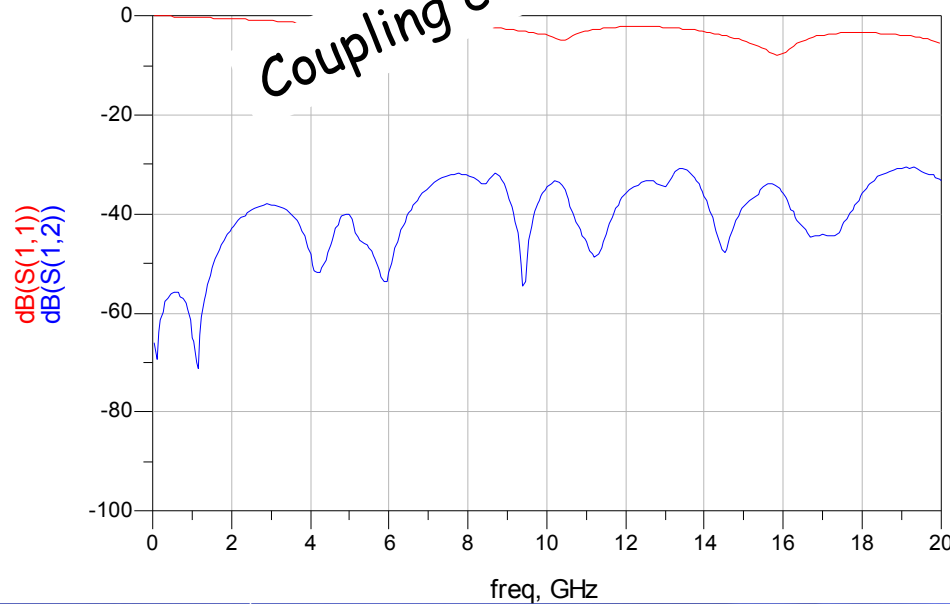
Ref: Nanju Na, et. al., "Design Optimization for Isolation in High Wiring Density Packages with High Speed SerDes Links", IEEE 56th Electronic Components and Technology Conference, pp. 187-193, San Diego, Cal. May 30-June 2, 2006.

Measured near-end crosstalk in high density packages

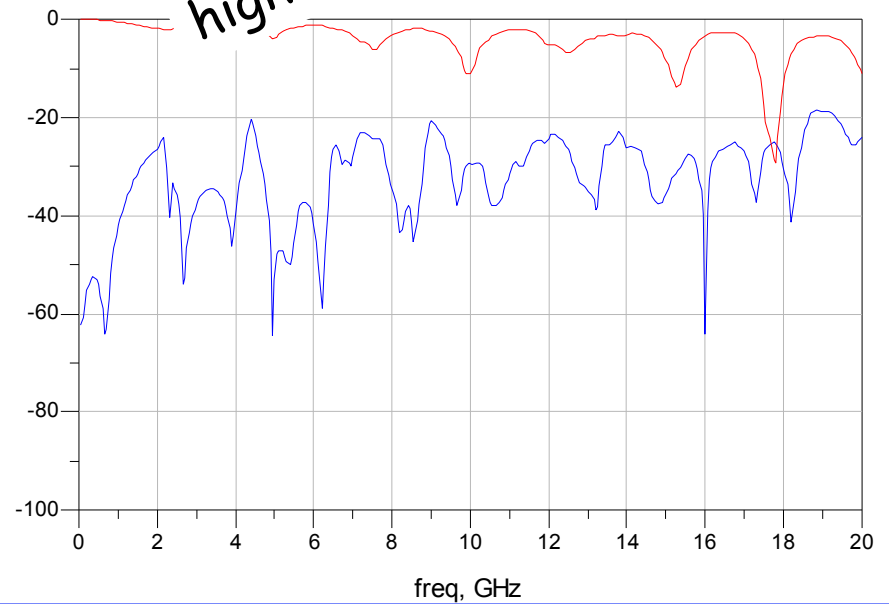
Probed on chip pads of two neighboring pairs with solder balls open



Coupling controlled in design



High coupling seen in a high density Ceramic



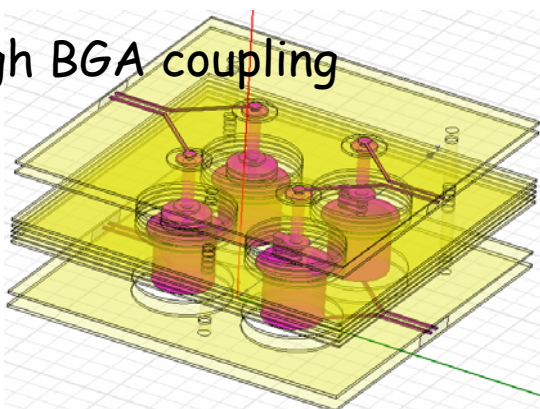
Package model proposal

- Organic flip-chip package modeled as a representative package
 - cost-performance effective and readily available with matured technology
 - most popular in SerDes application space
 - performance comparable among different organic package types
 - design routing option for better transmission
- Size: 23mm/55mm (as max. specified by JEDEC)
- Impedance tolerance $\pm 15\%$ for packaging industry reality
- Coupling consideration for reasonable ASIC wiring density

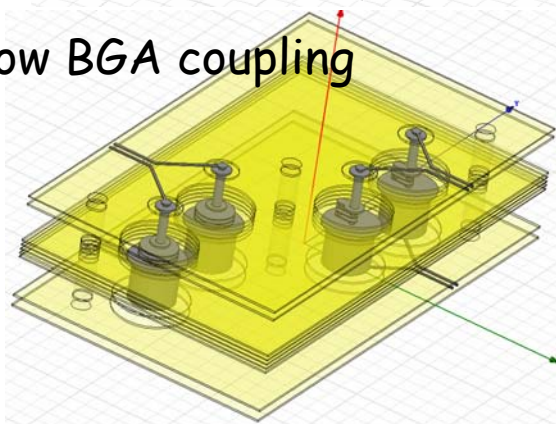
Package model construction of two pairs in coupling

HFSS model:
PTH vias/BGA balls

High BGA coupling



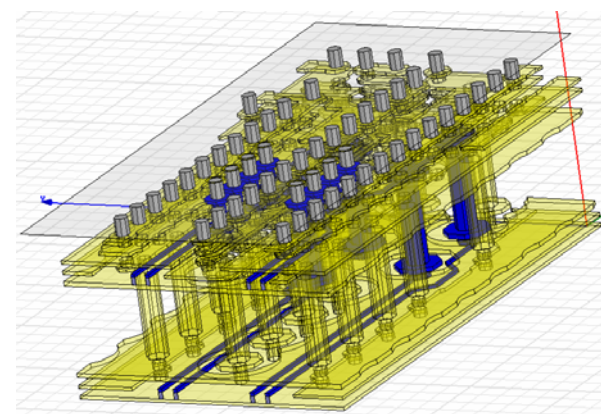
Low BGA coupling



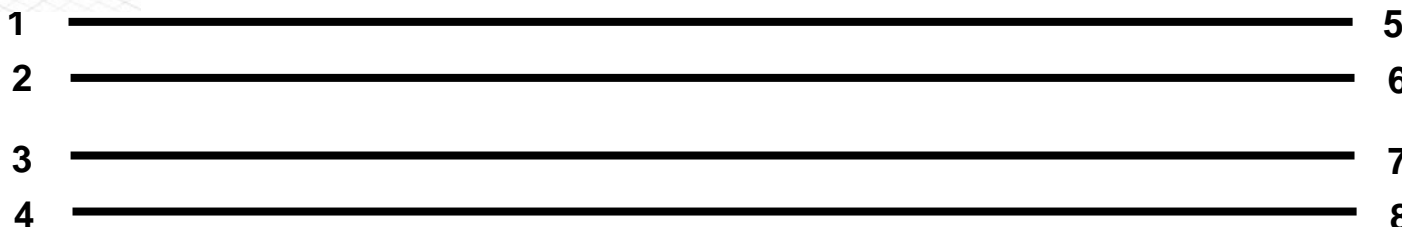
HFSS model:
 $Z_d = 115\Omega$,
33mm trace for 55mm package (JEDEC max)
Or 21mm trace



HFSS model:
extracted C4 escape



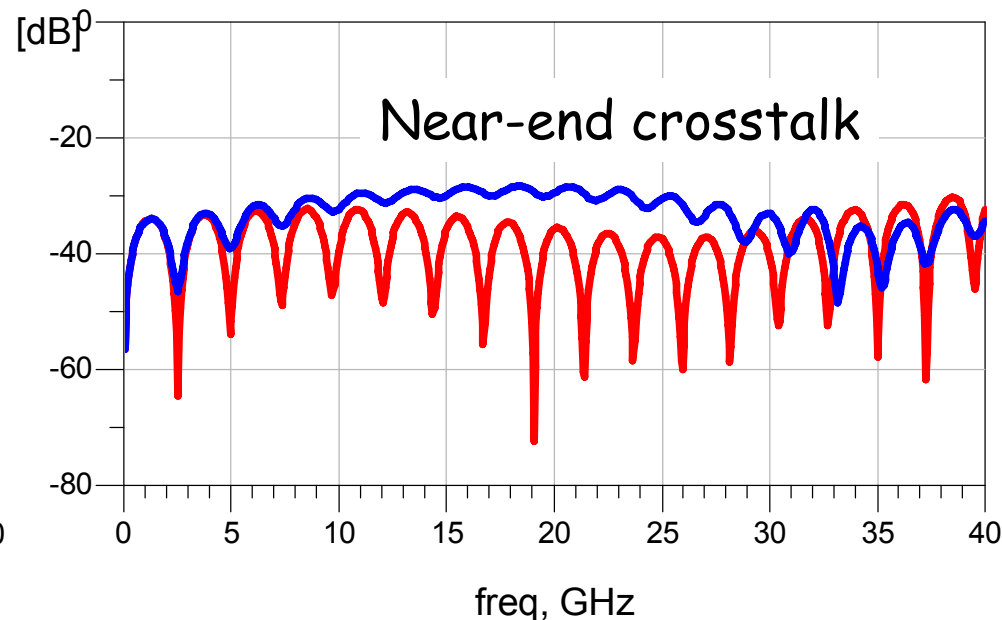
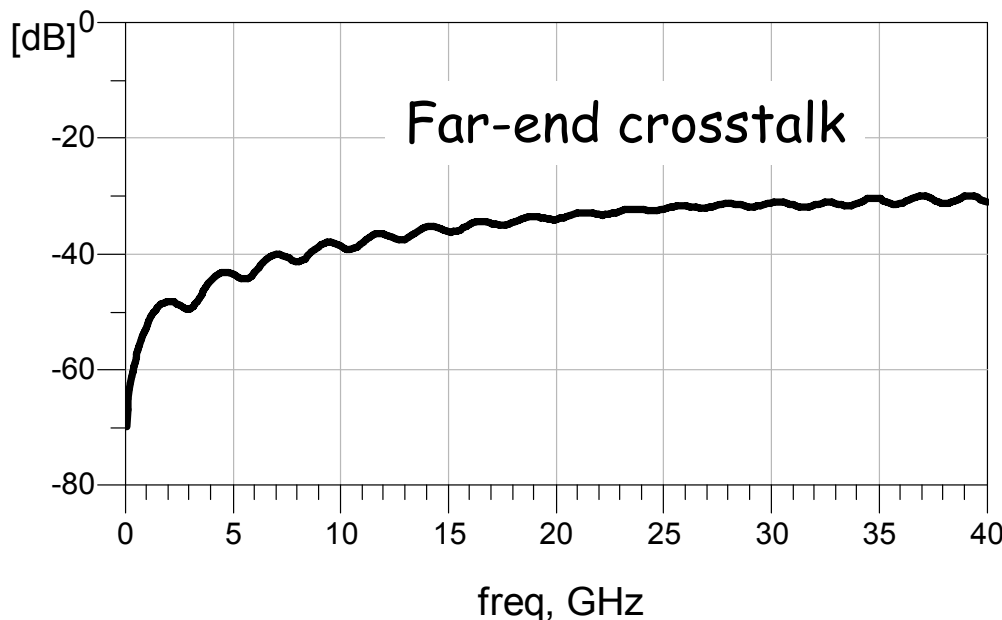
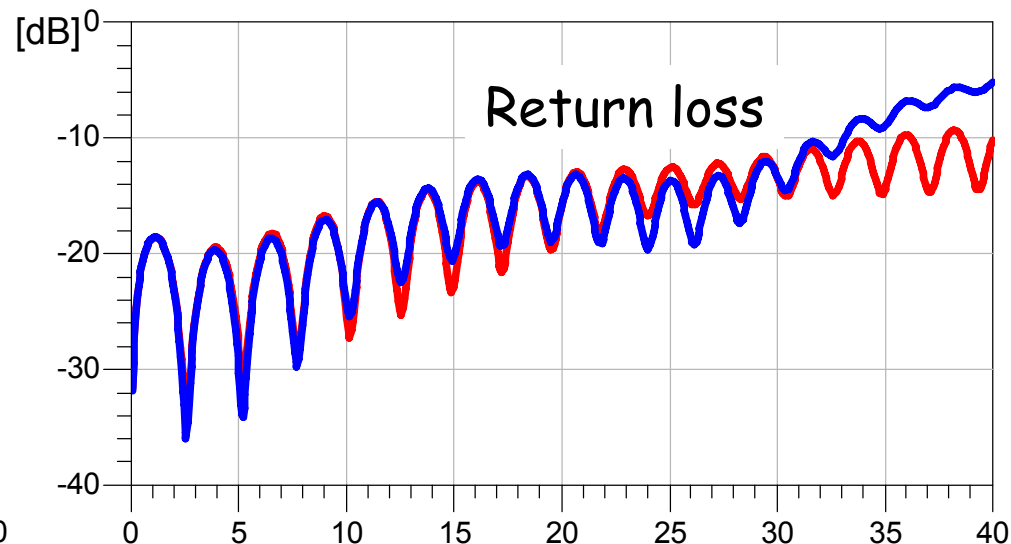
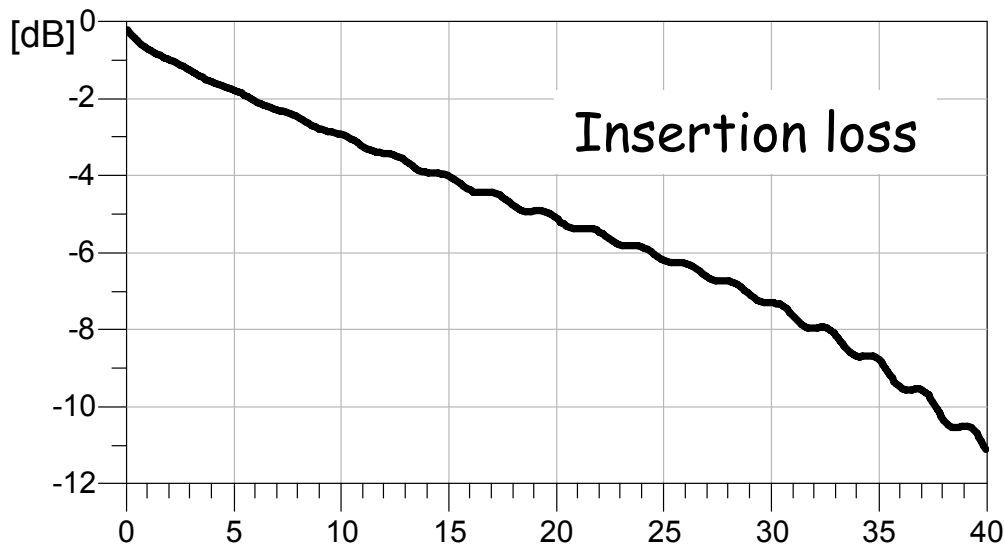
High trace coupling (small pair-to-pair space)
Or low trace coupling (large pair-to-pair space)



S-parameters of package models up to 40GHz

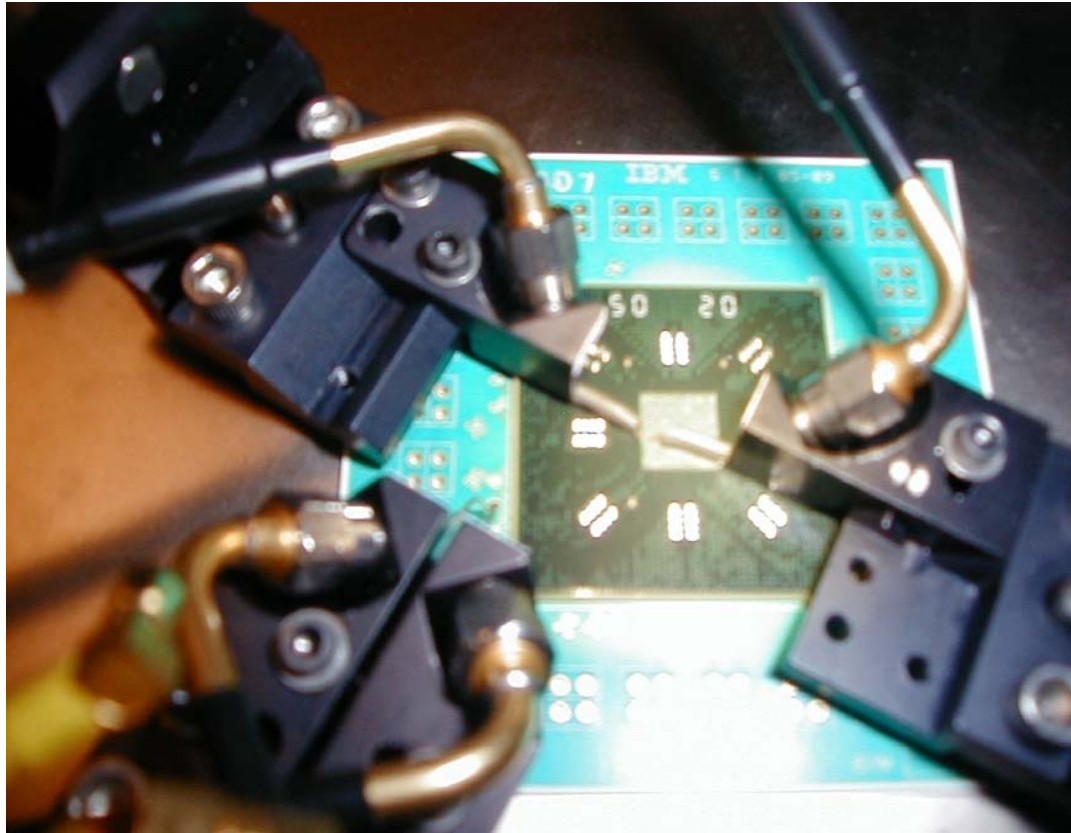
- Pkg55mm_T33mm115ohmHiXtalk_BGAHiXtalk.s8p
Trace 33mm with $Z_d=115\Omega$ and HIGH pair-to-pair coupling
BGA balls in HIGH coupling
- Pkg55mm_T33mm115ohmHiXtalk_BGALoXtalk.s8p
Trace 33mm with $Z_d=115\Omega$ and HIGH pair-to-pair coupling
BGA balls in LOW coupling
- Pkg55mm_T33mm115ohmLoXtalk_BGAHiXtalk.s8p
Trace 33mm with $Z_d=115\Omega$ and LOW pair-to-pair coupling
BGA balls in HIGH coupling
- Pkg55mm_T33mm115ohmLoXtalk_BGALoXtalk.s8p
Trace 33mm with $Z_d=115\Omega$ and LOW pair-to-pair coupling
BGA balls in LOW coupling
- Pkg35mm_T21mm115ohmHiXtalk_BGAHiXtalk.s8p
Trace 21mm with $Z_d=115\Omega$ and HIGH pair-to-pair coupling
BGA balls in HIGH coupling
- Pkg35mm_T21mm115ohmLoXtalk_BGALoXtalk.s8p
Trace 21mm with $Z_d=115\Omega$ and LOW pair-to-pair coupling
BGA balls in LOW coupling

Differential pair behavior: Pkg55mm_T33mm115ohmHiXtalk_BGALoXtalk



Back-up

Probing for package net measurements



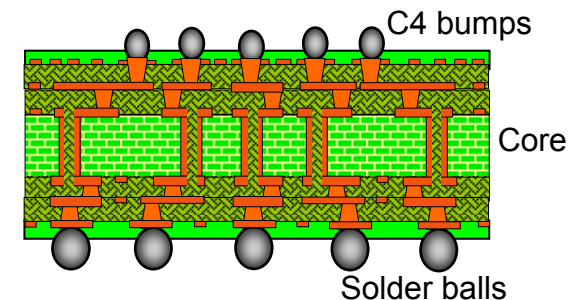
Major design-performance components in organic laminates

■ Trace

- Electrically long – significant impact if not controlled well
- Impedance control with manufacturing tolerance
- Design for impedance vs coupling in die escaping region

■ PTH vias

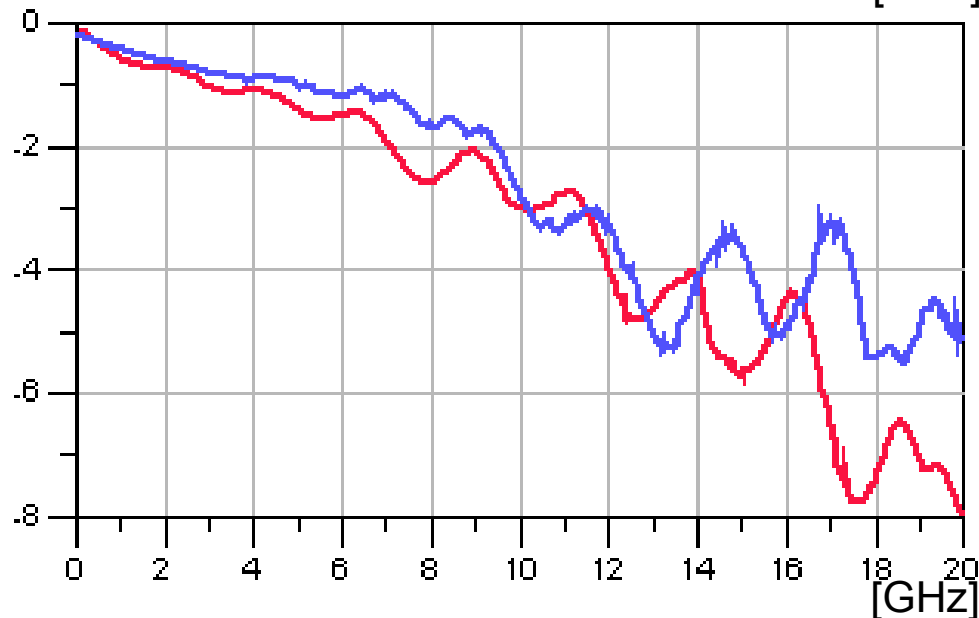
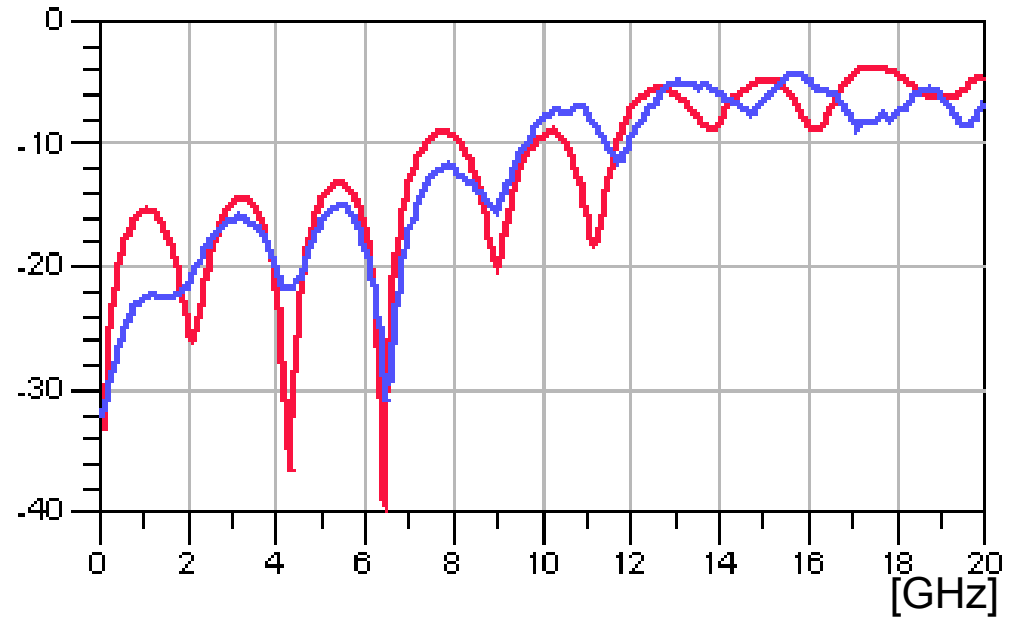
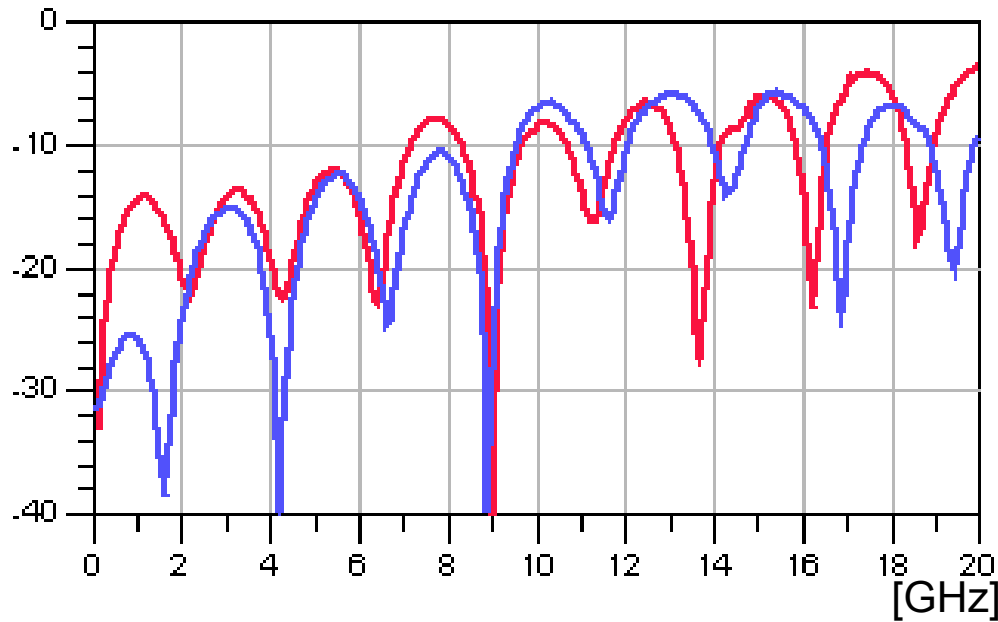
- Relatively large discontinuity path along vertical signal transition through high dielectric core
- Impedance effect of via hole/land/pitch
- Coupling effect with various pair patterns



■ BGA

- Very low impedance and high coupling path due to large geometric volume of the structure interacting with surrounding power/ground
- I/O assignment pattern for isolation

Simulation to measurement correlation



Red: simulation

Blue: measurement, includes 3mm board microstrip

Top left: return loss from C4 pads

Top right: return loss from BGAs

Bottom: insertion loss