SFP+ Host Chip and PMD Chip S4P Models

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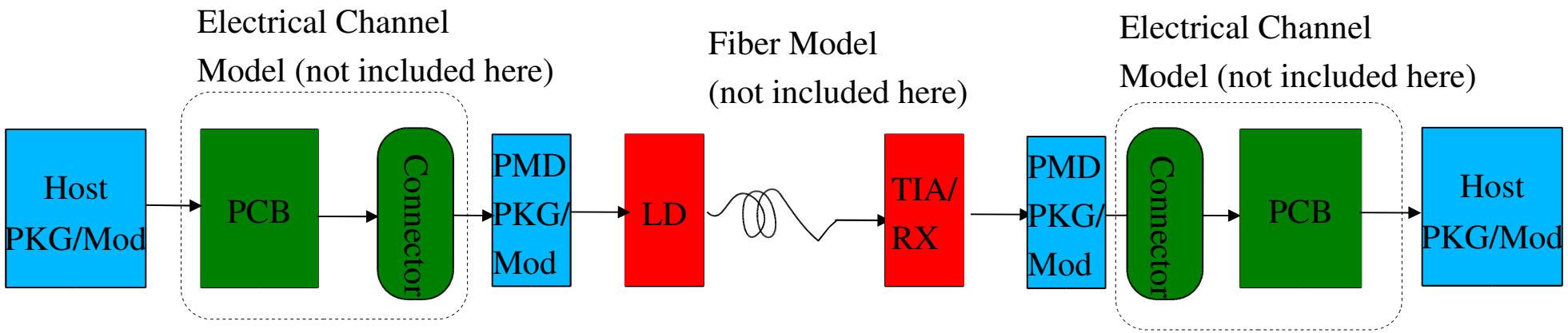
These models are provided as courtesy and as is.

Overview

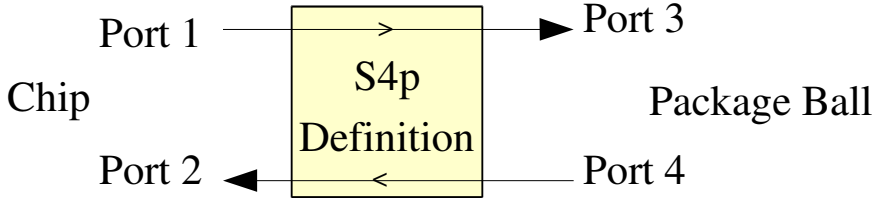
- **Provide host IC and PMD IC models for link simulation for up to 11 Gb/s.**
- **The s4p file include package model, chip parasitics, BGA balls, and BGA pads based on distributed models.**
  - ⇨BGA pads were 1 mm.
- **Package s4p model was extracted with 3D field solver.**
- **Package was based on a low cost plastic BGA.**
- **The host and PMD models have been used for SFP+ base line simulations.**
  - ⇨A version was also provided to T11 for 8.5 Gig FC with the same host return loss of -8 dB and PMD return loss of -10 dB but at 4.25 GHz instead of 5.5 GHz

Basic SFP+ Link Model

- **S4P files include package model and IC parasitics for typical 9.95-11.1 Gigabaud SerDes and PMD (Laser Driver and PostAMP/TIA) IC's.**
  - ⇨Host IC has 2 dB worse return loss than the PMD IC at 5.5 GHz



S4P File Definition for Host and Module S-parameters port definition



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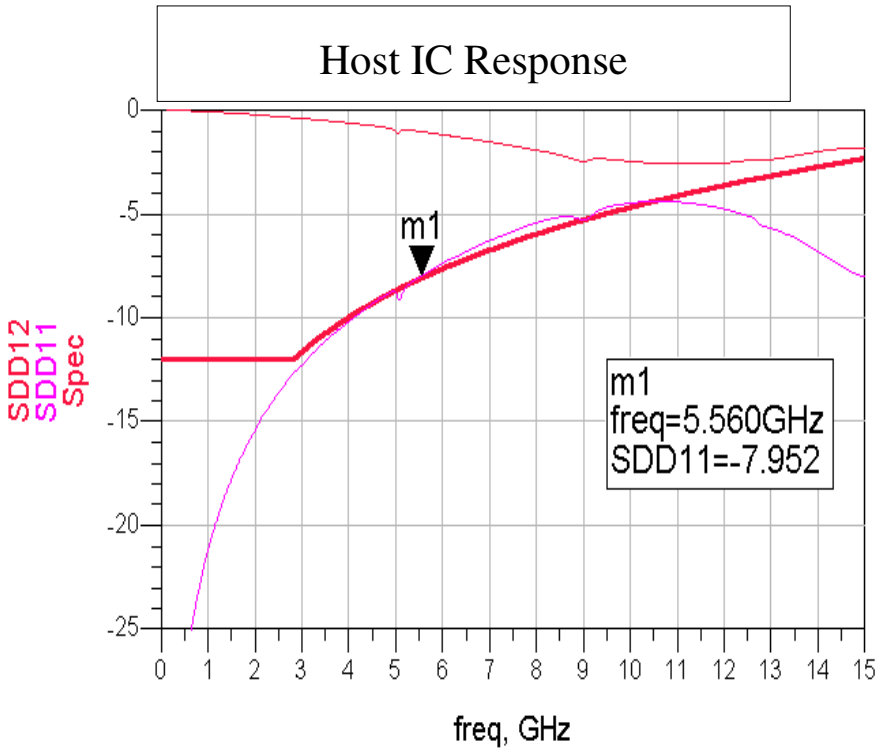
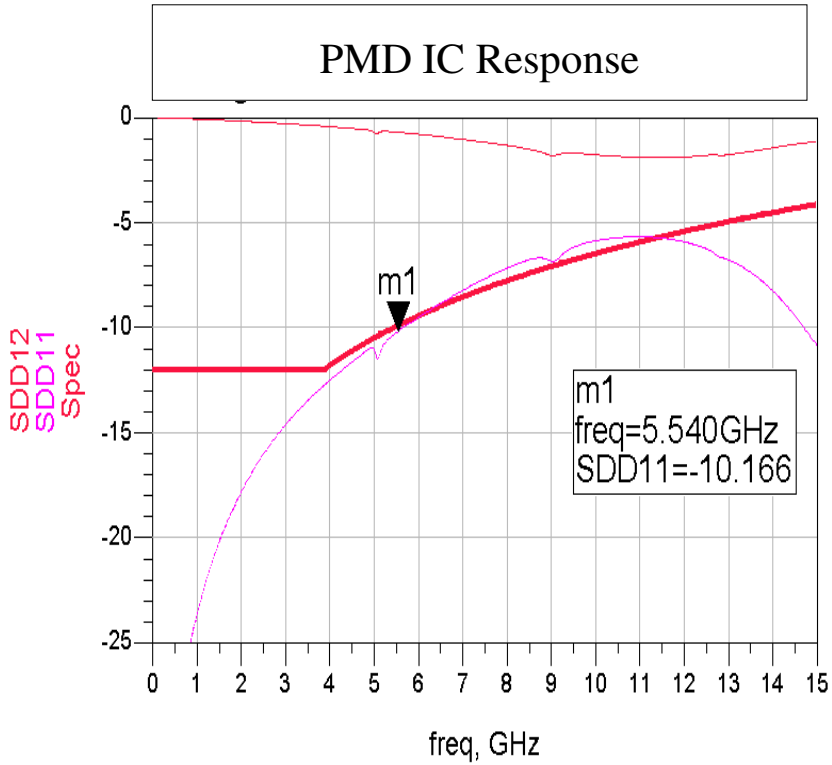
Host and PMD IC Response

- **More relaxed than XFP, similar to CEI, but tighter than 8Gig FC**



Eqn Spec=if(freq<2.8e9)then -12 else (-5.8 + 13.33*log10(freq/8.25e9



Eqn Spec=if(freq<3.9e9)then -12 else (-7.6 + 13.33*log10(freq/8.25e9))