Changes to ANSI/IEEE Std. IEEE 802.3-2008, Clause 45

45. Management Data Input/Output (MDIO) Interface

45.2.1 PMA/PMD registers

Modify Table 45–3 from the form modified by IEEE 802.3ba-D3.0.

Table 45–3—PMA/PMD PMA/PMD registers

Register address	Register name	Clause
~~1.1710 through 1.32767~~	~~Reserved~~	
1.1710 through 1.1799	Reserved	
1.1800	TimeSync capability	45.2.1.100
1.1801 through 1.1804	TimeSync PHY transmit latency	45.2.1.101
1.1805 through 1.1808	TimeSync PHY receive latency	45.2.1.102
1.1809 through 1.32767	Reserved	

Insert subclauses 45.2.1.100, 45.2.1.101, 45.2.1.102 immediately after the last subclause added in the IEEE P802.3ba draft D3.0:

45.2.1.100 TimeSync capability (Register 1.1800)

The TimeSync PHY capability register (see Table 45–65e) identifies the capability of the given PHY to provide the transmit and receive paths, as stored in registers 1.1801 through 1.1804 and 1.1805 through 1.1808, respectively.

Table 45–65e—TimeSync PHY capability

Bit(s)	Name	Description	R/W[a]
1.1800.15:2	Reserved	Value always zero, writes ignored	RO
1.1800.1	TimeSync PHY latency for transmit path	1 = PHY provides transmit path latency information in registers 1.1801 through 1.1804 0 = PHY does not provide transmit path latency information	
1.1800.0	TimeSync PHY latency for receive path	1 = PHY provides receive path latency information in registers 1.1805 through 1.1808 0 = PHY does not provide receive path latency information	

[a]RO = Read only, R/W = Read/Write

45.2.1.101 TimeSync PHY transmit latency (Register 1.1801, 1.1802, 1.1803, 1.1804)

The TimeSync PHY transmit latency register s s the maximum (Register 1.1801, 1.1802) and minimum (Register 1.1803, 1.1804) values of the PHY transmit latency, as defined in Table 45–65f. PHY transmit latency is expressed in units of ns.

Table 45–65f—TimeSync PHY transmit latency register

Bit(s)	Name	Description	R/W[a]
1.1801.15:0	Maximum PHY transmit latency, lower	PHY_latency_TX_max [15:0]	RO, NR
1.1802.15:0	Maximum PHY transmit latency, upper	PHY_latency_TX_max [31:16]	RO, MW, NR
1.1803.15:0	Minimum PHY transmit latency, lower	PHY_latency_TX_min [15:0]	RO, MW, NR
1.1804.15:0	Minimum PHY transmit latency, upper	PHY_latency_TX_min [31:16]	RO, MW, NR

[a]RO = Read only, MW = Multi-word, NR = Non Roll-over

45.2.1.102 TimeSync PHY receive latency (Register 1.1805, 1.1806, 1.1807, 1.1808)

The TimeSync PHY receive latency register s s the maximum (Register 1.1805, 1.1806) and minimum (Register 1.1807, 1.1808) values of the PHY receive latency, as defined in Table 45–65g. PHY receive latency is expressed in units of ns.

Table 45–65g—TimeSync PHY receive latency register

Bit(s)	Name	Description	R/W[a]
1.1805.15:0	Maximum PHY receive latency, lower	PHY_latency_RX_max [15:0]	RO, MW, NR
1.1806.15:0	Maximum PHY receive latency, upper	PHY_latency_RX_max [31:16]	RO, MW, NR
1.1807.15:0	Minimum PHY receive latency, lower	PHY_latency_RX_min [15:0]	RO, MW, NR
1.1808.15:0	Minimum PHY receive latency, upper	PHY_latency_RX_min [31:16]	RO, MW, NR

[a]RO = Read only, MW = Multi-word, NR = Non Roll-over