45. Management Data Input/Output (MDIO) Interface

45.2.1 PMA/PMD registers

Modify Table 45–3 from the form modified by IEEE Std 802.3ba:

Table 45–3—PMA/PMD registers

Register address	Register name	Clause
~~1.1710 through 1.32767~~	~~Reserved~~	
1.1710 through 1.1799	Reserved	
1.1800	TimeSync PMA/PMD capability	45.2.1.99a
1.1801 through 1.1804	TimeSync PMA/PMD transmit path data delay	45.2.1.99b
1.1805 through 1.1808	TimeSync PMA/PMD receive path data delay	45.2.1.99c
1.1809 through 1.32767	Reserved	

Insert subclauses 45.2.1.99a, 45.2.1.99b, 45.2.1.99c immediately after the last subclause added in IEEE Std 802.3ba, 45.2.1:

45.2.1.99a TimeSync PMA/PMD capability (Register 1.1800)

The TimeSync PMA/PMD capability register (see Table 45–65e) indicates the capability of the PMA/PMD to report the transmit and receive data delay, stored in registers 1.1801 through 1.1804 and 1.1805 through 1.1808, respectively.

Table 45–65e—TimeSync PMA/PMD capability

Bit(s)	Name	Description	R/W[a]
1.1800.15:2	Reserved	Value always zero, writes ignored	RO
1.1800.1	TimeSync transmit path data delay	1 = PMA/PMD provides information on transmit path data delay in registers 1.1801 through 1.1804 0 = PMA/PMD does not provide information on transmit path data delay	RO
1.1800.0	TimeSync receive path data delay	1 = PMA/PMD provides information on receive path data delay in registers 1.1801 through 1.1804 0 = PMA/PMD does not provide information on receive path data delay	RO

[a]RO = Read only

45.2.1.99b TimeSync PMA/PMD transmit path data delay (Registers 1.1801, 1.1802, 1.1803, 1.1804)

The TimeSync PMA/PMD transmit path data delay register contains the maximum (Registers 1.1801, 1.1802, see Table 45–65f) and minimum (Registers 1.1803, 1.1804, see Table 45–65f) values of the transmit

path data delay. The transmit path data delay is expressed in the units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in Register 1.1 (see 45.2.1.2.2).

Table 45–65f—TimeSync PMA/PMD transmit path data delay register

Bit(s)	Name	Description	R/W[a]
1.1801.15:0	Maximum PMA/PMD transmit path data delay, lower	PMA/PMD_delay_TX_max [15:0]	RO, MW
1.1802.15:0	Maximum PMA/PMD transmit path data delay, upper	PMA/PMD_delay_TX_max [31:16]	RO, MW
1.1803.15:0	Minimum PMA/PMD transmit path data delay, lower	PMA/PMD_delay_TX_min [15:0]	RO, MW
1.1804.15:0	Minimum PMA/PMD transmit path data delay, upper	PMA/PMD_delay_TX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.1.99c TimeSync PMA/PMD receive path data delay (Registers 1.1805, 1.1806, 1.1807, 1.1808)

The TimeSync PMA/PMD receive path data delay register contains the maximum (Registers 1.1805, 1.1806, see Table 45–65g) and minimum (Registers 1.1807, 1.1808, see Table 45–65g) values of the receive path data delay. The receive path data delay is expressed in the units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in Register 1.1 (see 45.2.1.2.2).

Table 45–65g—TimeSync PMA/PMD receive path data delay register

Bit(s)	Name	Description	R/W[a]
1.1805.15:0	Maximum PMA/PMD receive path data delay, lower	PMA/PMD_delay_RX_max [15:0]	RO, MW
1.1806.15:0	Maximum PMA/PMD receive path data delay, upper	PMA/PMD_delay_RX_max [31:16]	RO, MW
1.1807.15:0	Minimum PMA/PMD receive path data delay, lower	PMA/PMD_delay_RX_min [15:0]	RO, MW
1.1808.15:0	Minimum PMA/PMD receive path data delay, upper	PMA/PMD_delay_RX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.2 WIS registers

Modify Table 45–65 from the form included in IEEE Std 802.3-2008:

Insert subclauses 45.2.2.19a, 45.2.2.19b, 45.2.2.19c immediately after the last subclause in IEEE Std 802.3-2008, 45.2.2:

Table 45–65—WIS registers

Register address	Register name	Clause
~~2.80 through 2.32 767~~	~~Reserved~~	
2.80 through 2.1799	Reserved	
2.1800	TimeSync WIS capability	45.2.2.19a
2.1801 through 2.1804	TimeSync WIS transmit path data delay	45.2.2.19b
2.1805 through 2.1808	TimeSync WIS receive path data delay	45.2.2.19c
2.1809 through 2.32767	Reserved	

45.2.2.19aTimeSync WIS capability (Register 2.1800)

The TimeSync WIS capability register (see Table 45–81a) indicates the capability of the WIS to report the transmit and receive data delay, stored in registers 2.1801 through 2.1804 and 2.1805 through 2.1808, respectively.

Table 45–81a—TimeSync WIS capability

Bit(s)	Name	Description	R/W[a]
2.1800.15:2	Reserved	Value always zero, writes ignored	RO
2.1800.1	TimeSync transmit path data delay	1 = WIS provides information on transmit path data delay in registers 2.1801 through 2.1804 0 = WIS does not provide information on transmit path data delay	RO
2.1800.0	TimeSync receive path data delay	1 = WIS provides information on receive path data delay in registers 2.1801 through 2.1804 0 = WIS does not provide information on receive path data delay	RO

[a]RO = Read only

45.2.2.19bTimeSync WIS transmit path data delay (Registers 2.1801, 2.1802, 2.1803, 2.1804)

The TimeSync WIS transmit path data delay register contains the maximum (Registers 2.1801, 2.1802, see Table 45–81b) and minimum (Registers 2.1803, 2.1804, see Table 45–81b) values of the transmit path data

delay. The transmit path data delay is expressed in the units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in Register 1.1 (see 45.2.1.2.2).

Table 45–81b—TimeSync WIS transmit path data delay register

Bit(s)	Name	Description	R/W[a]
2.1801.15:0	Maximum WIS transmit path data delay, lower	WIS_delay_TX_max [15:0]	RO, MW
2.1802.15:0	Maximum WIS transmit path data delay, upper	WIS_delay_TX_max [31:16]	RO, MW
2.1803.15:0	Minimum WIS transmit path data delay, lower	WIS_delay_TX_min [15:0]	RO, MW
2.1804.15:0	Minimum WIS transmit path data delay, upper	WIS_delay_TX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.2.19cTimeSync WIS receive path data delay (Registers 2.1805, 2.1806, 2.1807, 2.1808)

The TimeSync WIS receive path data delay register contains the maximum (Registers 2.1805, 2.1806, see Table 45–81c) and minimum (Registers 2.1807, 2.1808, see Table 45–81c) values of the receive path data delay. The receive path data delay is expressed in the units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in Register 1.1 (see 45.2.1.2.2).

Table 45–81c—TimeSync WIS receive path data delay register

Bit(s)	Name	Description	R/W[a]
2.1805.15:0	Maximum WIS receive path data delay, lower	WIS_delay_RX_max [15:0]	RO, MW
2.1806.15:0	Maximum WIS receive path data delay, upper	WIS_delay_RX_max [31:16]	RO, MW
2.1807.15:0	Minimum WIS receive path data delay, lower	WIS_delay_RX_min [15:0]	RO, MW
2.1808.15:0	Minimum WIS receive path data delay, upper	WIS_delay_RX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.3 PCS registers

Modify Table 45–82 from the form modified by IEEE Std 802.3ba:

Insert subclauses 45.2.3.39a, 45.2.3.39b, 45.2.3.39c immediately after the last subclause added by IEEE Std 802.3ba, 45.2.3:

Table 45–82—PCS registers

Register address	Register name	Clause
~~3.420 through 3.32 767~~	~~Reserved~~	
3.420 through 3.1799	Reserved	
3.1800	TimeSync PCS capability	45.2.3.39a
3.1801 through 3.1804	TimeSync PCS transmit path data delay	45.2.3.39b
3.1805 through 3.1808	TimeSync PCS receive path data delay	45.2.3.39c
3.1809 through 3.32767	Reserved	

45.2.3.39aTimeSync PCS capability (Register 3.1800)

The TimeSync PCS capability register (see Table 45–115cc) indicates the capability of the PCS to report the transmit and receive data delay, stored in registers 3.1801 through 3.1804 and 3.1805 through 3.1808, respectively.

Table 45–115c—TimeSync PCS capability

Bit(s)	Name	Description	R/W[a]
3.1800.15:2	Reserved	Value always zero, writes ignored	RO
3.1800.1	TimeSync transmit path data delay	1 = PCS provides information on transmit path data delay in registers 3.1801 through 3.1804 0 = PCS does not provide information on transmit path data delay	RO
3.1800.0	TimeSync receive path data delay	1 = PCS provides information on receive path data delay in registers 3.1801 through 3.1804 0 = PCS does not provide information on receive path data delay	RO

[a]RO = Read only

45.2.3.39bTimeSync PCS transmit path data delay (Registers 3.1801, 3.1802, 3.1803, 3.1804)

The TimeSync PCS transmit path data delay register contains the maximum (Registers 3.1801, 3.1802, see Table 45–115d) and minimum (Registers 3.1803, 3.1804, see Table 45–115d) values of the transmit path

data delay. The transmit path data delay is expressed in the units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in Register 1.1 (see 45.2.1.2.2).

Table 45–115d—TimeSync PCS transmit path data delay register

Bit(s)	Name	Description	R/W[a]
3.1801.15:0	Maximum PCS transmit path data delay, lower	PCS_delay_TX_max [15:0]	RO, MW
3.1802.15:0	Maximum PCS transmit path data delay, upper	PCS_delay_TX_max [31:16]	RO, MW
3.1803.15:0	Minimum PCS transmit path data delay, lower	PCS_delay_TX_min [15:0]	RO, MW
3.1804.15:0	Minimum PCS transmit path data delay, upper	PCS_delay_TX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.3.39cTimeSync PCS receive path data delay (Registers 3.1805, 3.1806, 3.1807, 3.1808)

The TimeSync PCS receive path data delay register contains the maximum (Registers 3.1805, 3.1806, see Table 45–115e) and minimum (Registers 3.1807, 3.1808, see Table 45–115e) values of the receive path data delay. The receive path data delay is expressed in the units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in Register 1.1 (see 45.2.1.2.2).

Table 45–115e—TimeSync PCS receive path data delay register

Bit(s)	Name	Description	R/W[a]
3.1805.15:0	Maximum PCS receive path data delay, lower	PCS_delay_RX_max [15:0]	RO, MW
3.1806.15:0	Maximum PCS receive path data delay, upper	PCS_delay_RX_max [31:16]	RO, MW
3.1807.15:0	Minimum PCS receive path data delay, lower	PCS_delay_RX_min [15:0]	RO, MW
3.1808.15:0	Minimum PCS receive path data delay, upper	PCS_delay_RX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.4 PHY XS registers

Modify Table 45–108 from the form included in IEEE Std 802.3-2008:

Insert subclauses 45.2.4.9a, 45.2.4.9b, 45.2.4.9c immediately after the last subclause in IEEE Std 802.3-2008, 45.2.4:

Table 45–108—PCS registers

Register address	Register name	Clause
~~4.26 through 4.32 767~~	~~Reserved~~	
4.26 through 4.1799	Reserved	
4.1800	TimeSync PHY XS capability	45.2.4.9a
4.1801 through 4.1804	TimeSync PHY XS transmit path data delay	45.2.4.9b
4.1805 through 4.1808	TimeSync PHY XS receive path data delay	45.2.4.9c
4.1809 through 4.32767	Reserved	

45.2.4.9aTimeSync PHY XS capability (Register 4.1800)

The TimeSync PHY XS capability register (see Table 45–114a) indicates the capability of the PHY XS to report the transmit and receive data delay, stored in registers 4.1801 through 4.1804 and 4.1805 through 4.1808, respectively.

Table 45–114a—TimeSync PHY XS capability

Bit(s)	Name	Description	R/W[a]
4.1800.15:2	Reserved	Value always zero, writes ignored	RO
4.1800.1	TimeSync transmit path data delay	1 = PHY XS provides information on transmit path data delay in registers 4.1801 through 4.1804 0 = PHY XS does not provide information on transmit path data delay	RO
4.1800.0	TimeSync receive path data delay	1 = PHY XS provides information on receive path data delay in registers 4.1801 through 4.1804 0 = PHY XS does not provide information on receive path data delay	RO

[a]RO = Read only

45.2.4.9bTimeSync PHY XS transmit path data delay (Registers 4.1801, 4.1802, 4.1803, 4.1804)

The TimeSync PHY XS transmit path data delay register contains the maximum (Registers 4.1801, 4.1802, see Table 45–114b) and minimum (Registers 4.1803, 4.1804, see Table 45–114b) values of the transmit path

data delay. The transmit path data delay is expressed in the units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in Register 1.1 (see 45.2.1.2.2).

Table 45–114b—TimeSync PHY XS transmit path data delay register

Bit(s)	Name	Description	R/W[a]
4.1801.15:0	Maximum PHY XS transmit path data delay, lower	PHY_XS_delay_TX_max [15:0]	RO, MW
4.1802.15:0	Maximum PHY XS transmit path data delay, upper	PHY_XS_delay_TX_max [31:16]	RO, MW
4.1803.15:0	Minimum PHY XS transmit path data delay, lower	PHY_XS_delay_TX_min [15:0]	RO, MW
4.1804.15:0	Minimum PHY XS transmit path data delay, upper	PHY_XS_delay_TX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.4.9cTimeSync PHY XS receive path data delay (Registers 4.1805, 4.1806, 4.1807, 4.1808)

The TimeSync PHY XS receive path data delay register contains the maximum (Registers 4.1805, 4.1806, see Table 45–114c) and minimum (Registers 4.1807, 4.1808, see Table 45–114c) values of the receive path data delay. The receive path data delay is expressed in the units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in Register 1.1 (see 45.2.1.2.2).

Table 45–114c—TimeSync PHY XS receive path data delay register

Bit(s)	Name	Description	R/W[a]
4.1805.15:0	Maximum PHY XS receive path data delay, lower	PHY_XS_delay_RX_max [15:0]	RO, MW
4.1806.15:0	Maximum PHY XS receive path data delay, upper	PHY_XS_delay_RX_max [31:16]	RO, MW
4.1807.15:0	Minimum PHY XS receive path data delay, lower	PHY_XS_delay_RX_min [15:0]	RO, MW
4.1808.15:0	Minimum PHY XS receive path data delay, upper	PHY_XS_delay_RX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.5 DTE XS registers

Modify Table 45–115 from the form included in IEEE Std 802.3-2008:

Insert subclauses 45.2.5.9a, 45.2.5.9b, 45.2.5.9c immediately after the last subclause in IEEE Std 802.3-2008, 45.2.5:

Table 45–115—DTE XS registers

Register address	Register name	Clause
~~5.26 through 5.32 767~~	~~Reserved~~	
5.26 through 5.1799	Reserved	
5.1800	TimeSync DTE XS capability	45.2.5.9a
5.1801 through 5.1804	TimeSync DTE XS transmit path data delay	45.2.5.9b
5.1805 through 5.1808	TimeSync DTE XS receive path data delay	45.2.5.9c
5.1809 through 5.32767	Reserved	

45.2.5.9aTimeSync DTE XS capability (Register 5.1800)

The TimeSync DTE XS capability register (see Table 45–121a) indicates the capability of the DTE XS to report the transmit and receive data delay, stored in registers 5.1801 through 5.1804 and 5.1805 through 5.1808, respectively.

Table 45–121a—TimeSync DTE XS capability

Bit(s)	Name	Description	R/W[a]
5.1800.15:2	Reserved	Value always zero, writes ignored	RO
5.1800.1	TimeSync transmit path data delay	1 = DTE XS provides information on transmit path data delay in registers 5.1801 through 5.1804 0 = DTE XS does not provide information on transmit path data delay	RO
5.1800.0	TimeSync receive path data delay	1 = DTE XS provides information on receive path data delay in registers 5.1801 through 5.1804 0 = DTE XS does not provide information on receive path data delay	RO

[a]RO = Read only

45.2.5.9bTimeSync DTE XS transmit path data delay (Registers 5.1801, 5.1802, 5.1803, 5.1804)

The TimeSync DTE XS transmit path data delay register contains the maximum (Registers 5.1801, 5.1802, see Table 45–121b) and minimum (Registers 5.1803, 5.1804, see Table 45–121b) values of the transmit path

data delay. The transmit path data delay is expressed in the units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in Register 1.1 (see 45.2.1.2.2).

Table 45–121b—TimeSync DTE XS transmit path data delay register

Bit(s)	Name	Description	R/W[a]
5.1801.15:0	Maximum DTE XS transmit path data delay, lower	DTE_XS_delay_TX_max [15:0]	RO, MW
5.1802.15:0	Maximum DTE XS transmit path data delay, upper	DTE_XS_delay_TX_max [31:16]	RO, MW
5.1803.15:0	Minimum DTE XS transmit path data delay, lower	DTE_XS_delay_TX_min [15:0]	RO, MW
5.1804.15:0	Minimum DTE XS transmit path data delay, upper	DTE_XS_delay_TX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.5.9cTimeSync DTE XS receive path data delay (Registers 5.1805, 5.1806, 5.1807, 5.1808)

The TimeSync DTE XS receive path data delay register contains the maximum (Registers 5.1805, 5.1806, see Table 45–121c) and minimum (Registers 5.1807, 5.1808, see Table 45–121c) values of the receive path data delay. The receive path data delay is expressed in the units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in Register 1.1 (see 45.2.1.2.2).

Table 45–121c—TimeSync DTE XS receive path data delay register

Bit(s)	Name	Description	R/W[a]
5.1805.15:0	Maximum DTE XS receive path data delay, lower	DTE_XS_delay_RX_max [15:0]	RO, MW
5.1806.15:0	Maximum DTE XS receive path data delay, upper	DTE_XS_delay_RX_max [31:16]	RO, MW
5.1807.15:0	Minimum DTE XS receive path data delay, lower	DTE_XS_delay_RX_min [15:0]	RO, MW
5.1808.15:0	Minimum DTE XS receive path data delay, upper	DTE_XS_delay_RX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.6 TC registers

Modify Table 45–122 from the form included in IEEE Std 802.3-2008:

Insert subclauses 45.2.6.13a, 45.2.6.13b, 45.2.6.13c immediately after the last subclause in IEEE Std 802.3-2008, 45.2.6:

Table 45–122—TC registers

Register address	Register name	Clause
~~6.28 through 6.32 767~~	~~Reserved~~	
6.28 through 6.1799	Reserved	
6.1800	TimeSync TC capability	45.2.6.13a
6.1801 through 6.1804	TimeSync TC transmit path data delay	45.2.6.13b
6.1805 through 6.1808	TimeSync TC receive path data delay	45.2.6.13c
6.1809 through 6.32767	Reserved	

45.2.6.13aTimeSync TC capability (Register 6.1800)

The TimeSync TC capability register (see Table 45–132a) indicates the capability of the TC to report the transmit and receive data delay, stored in registers 6.1801 through 6.1804 and 6.1805 through 6.1808, respectively.

Table 45–132a—TimeSync TC capability

Bit(s)	Name	Description	R/W[a]
6.1800.15:2	Reserved	Value always zero, writes ignored	RO
6.1800.1	TimeSync transmit path data delay	1 = TC provides information on transmit path data delay in registers 6.1801 through 6.1804 0 = TC does not provide information on transmit path data delay	RO
6.1800.0	TimeSync receive path data delay	1 = TC provides information on receive path data delay in registers 6.1801 through 6.1804 0 = TC does not provide information on receive path data delay	RO

[a]RO = Read only

45.2.6.13bTimeSync TC transmit path data delay (Registers 6.1801, 6.1802, 6.1803, 6.1804)

The TimeSync TC transmit path data delay register contains the maximum (Registers 6.1801, 6.1802, see Table 45–132b) and minimum (Registers 6.1803, 6.1804, see Table 45–132b) values of the transmit path

data delay. The transmit path data delay is expressed in the units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in Register 1.1 (see 45.2.1.2.2).

Table 45–132b—TimeSync TC transmit path data delay register

Bit(s)	Name	Description	R/W[a]
6.1801.15:0	Maximum TC transmit path data delay, lower	TC_delay_TX_max [15:0]	RO, MW
6.1802.15:0	Maximum TC transmit path data delay, upper	TC_delay_TX_max [31:16]	RO, MW
6.1803.15:0	Minimum TC transmit path data delay, lower	TC_delay_TX_min [15:0]	RO, MW
6.1804.15:0	Minimum TC transmit path data delay, upper	TC_delay_TX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.6.13cTimeSync TC receive path data delay (Registers 6.1805, 6.1806, 6.1807, 6.1808)

The TimeSync TC receive path data delay register contains the maximum (Registers 6.1805, 6.1806, see Table 45–132c) and minimum (Registers 6.1807, 6.1808, see Table 45–132c) values of the receive path data delay. The receive path data delay is expressed in the units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in Register 1.1 (see 45.2.1.2.2).

Table 45–132c—TimeSync TC receive path data delay register

Bit(s)	Name	Description	R/W[a]
6.1805.15:0	Maximum TC receive path data delay, lower	TC_delay_RX_max [15:0]	RO, MW
6.1806.15:0	Maximum TC receive path data delay, upper	TC_delay_RX_max [31:16]	RO, MW
6.1807.15:0	Minimum TC receive path data delay, lower	TC_delay_RX_min [15:0]	RO, MW
6.1808.15:0	Minimum TC receive path data delay, upper	TC_delay_RX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word