30. Management

Add subclauses 30.12 as follows (marked in red)

30.12 Management for oTimeSync entity

If the optional TimeSync function is implemented, then the oTimeSync managed object class shall be implemented in its entirety. All attributes of this managed object class are mandatory. TimeSync management is optional with respect to all other CSMA/CD management.

30.12.1 TimeSync entity managed object class

This subclause formally defines the behaviours for the oTimeSync managed object class attributes.

30.12.1.1 aTimeSyncCapabilityTX

ATTRIBUTE APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

True if the optional TimeSync capability is supported in the transmit path and false otherwise. If a Clause 45 MDIO Interface to PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC is present, then the value stored in this attribute equals to the logical OR operation over the values stored in the following instantiated MDIO registers 1.1800.1, 2.1800.1, 3.1800.1, 4.1800.1, 5.1800.1, and 6.1800.1.

30.12.1.2 aTimeSyncCapabilityRX

ATTRIBUTE

APPROPRIATE SYNTAX: BOOLEAN

DUULEAN

BEHAVIOUR DEFINED AS:

True if the optional TimeSync capability is supported in the receive path and false otherwise. If a Clause 45 MDIO Interface to PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC is present, then the value stored in this attribute equals to the logical OR operation over the values stored in the following instantiated MDIO registers 1.1800.0, 2.1800.0, 3.1800.0, 4.1800.0, 5.1800.0, and 6.1800.0.

30.12.1.3 aTimeSyncDelayTXmax

ATTRIBUTE	42
ATTRIDUTE	43
APPROPRIATE SYNTAX:	44
INTEGER	45
BEHAVIOUR DEFINED AS:	46
The maximum data delay as specified in 90.7, expressed in the units of ns.	47
If a Clause 45 MDIO Interface to PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC is prese	ent, 48
then the value stored in this attribute accounts for maximum transmit path data delay values,	49
composed of the following instantiated MDIO registers (for each MMD, in case of multiple	50
instances):	51
— for PMA/PMD: 1.1801 and 1.1802,	52
	53
— for WIS: 2.1801 and 2.1802,	54

— for PCS: 3.1801 and 3.1802,	1
— for PHY XS: 4.1801 and 4.1802,	2
— for DTE XS: 5.1801 and 5.1802,	3
— for TC: 6.1801 and 6.1802.	4
— 101 T.C. 0.1001 and 0.1002.	5 6
30.12.1.4 aTimeSyncDelayTXmin	7 8
ATTRIBUTE	8
APPROPRIATE SYNTAX: INTEGER	10 11
BEHAVIOUR DEFINED AS:	12
The minimum data delay as specified in 90.7, expressed in the units of ns.	13
If a Clause 45 MDIO Interface to PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC is present,	14 15
then the value stored in this attribute accounts for minimum transmit path data delay values, composed of the following instantiated MDIO registers (for each MMD, in case of multiple	16
instances):	17
— for PMA/PMD: 1.1803 and 1.1804,	18
— for WIS: 2.1803 and 2.1804,	19 20
— for PCS: 3.1803 and 3.1804,	20 21
— for PHY XS: 4.1803 and 4.1804,	22
- for DTE XS: 5.1803 and 5.1804,	23
 for DTE X3: 5.1605 and 5.1604, for TC: 6.1803 and 6.1804. 	24
— 101 TC. 0.1803 and 0.1804.	25 26
30.12.1.5 aTimeSyncDelayRXmax	26 27
	28
ATTRIBUTE	29
APPROPRIATE SYNTAX:	30
INTEGER	31
BEHAVIOUR DEFINED AS:	32 33
The maximum data delay as specified in 90.7, expressed in the units of ns. If a Clause 45 MDIO Interface to PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC is present,	34
then the value stored in this attribute accounts for maximum receive path data delay values,	35
composed of the following instantiated MDIO registers (for each MMD, in case of multiple	36
instances):	37
— for PMA/PMD: 1.1805 and 1.1806,	38 39
— for WIS: 2.1805 and 2.1806,	40
— for PCS: 3.1805 and 3.1806,	41
— for PHY XS: 4.1805 and 4.1806,	42
— for DTE XS: 5.1805 and 5.1806,	43
— for TC: 6.1805 and 6.1806.	44 45
	46
30.12.1.6 aTimeSyncDelayRXmin	47
ATTRIBUTE	48
APPROPRIATE SYNTAX:	49 50
INTEGER	50 51
BEHAVIOUR DEFINED AS:	52
The minimum data delay as specified in 90.7, expressed in the units of ns.	53
	54

If a Clause 45 MDIO Interface to to PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC is present, then the value stored in this attribute accounts for minimum receive path data delay values, composed of the following instantiated MDIO registers (for each MMD, in case of multiple instances):	1 2 3 4
 for PMA/PMD: 1.1807 and 1.1808,	5
for WIS: 2.1807 and 2.1808,	6
for PCS: 3.1807 and 3.1808,	7
for PHY XS: 4.1807 and 4.1808,	8 9
for DTE XS: 5.1807 and 5.1808,	10
for TC: 6.1807 and 6.1808.	11
 101 TC: 0.1807 and 0.1808.	12
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