In Module Deskew Function and Budget

40Gb/s Ethernet Single-mode Fibre PMD Task Force
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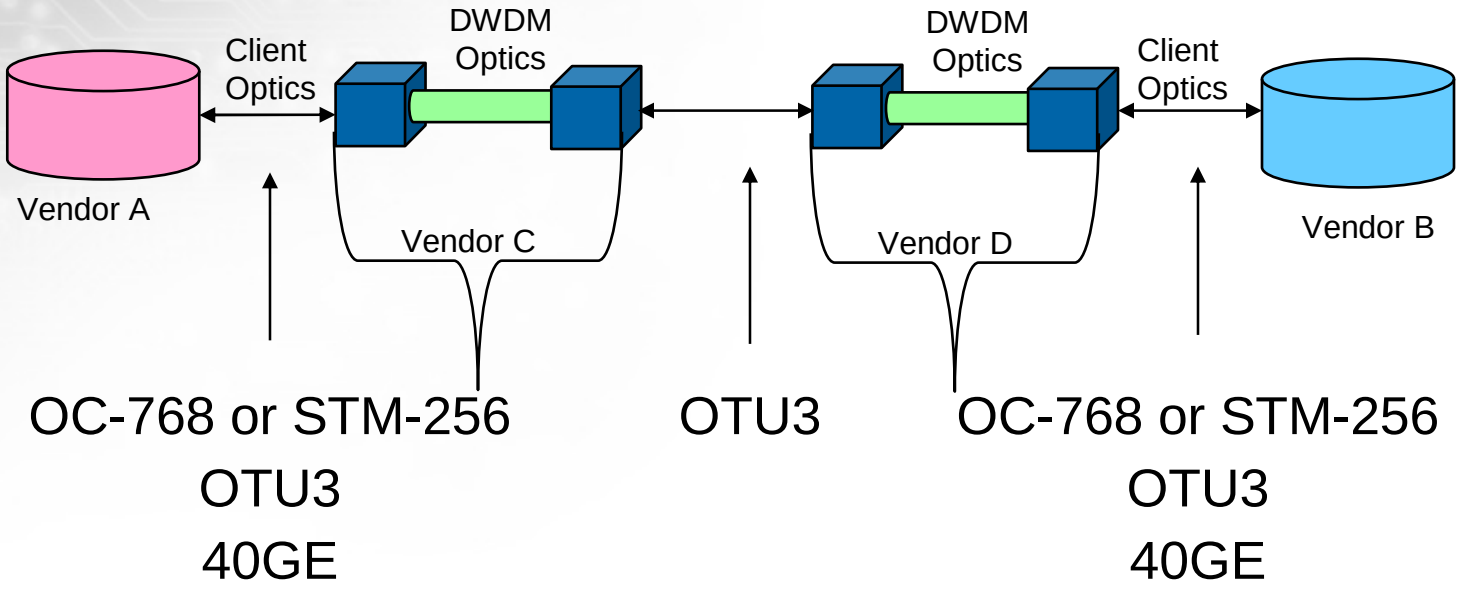
Song Shang

Carrier 40G Network Architecture



- **As currently defined in 802.3ba, 40GBASE-LR4 is optically incompatible with installed base preventing development of *a single multi-protocol 40G module (ex. CFP) that supports 40GE and the installed base of OC-768 or STM-256, and OTU3 services*.**
- **This has significant cost implications for carrier networks.**
- **A single multi-protocol 40G module optimized for central office reach* benefits carriers immensely and enables efficient increase in the global Ethernet footprint and penetration.**

* Common reach for client interfaces in carrier networks is 2km

From ATT presentation at 40GE SMF CFI material

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Requirements of In-Module Deskew

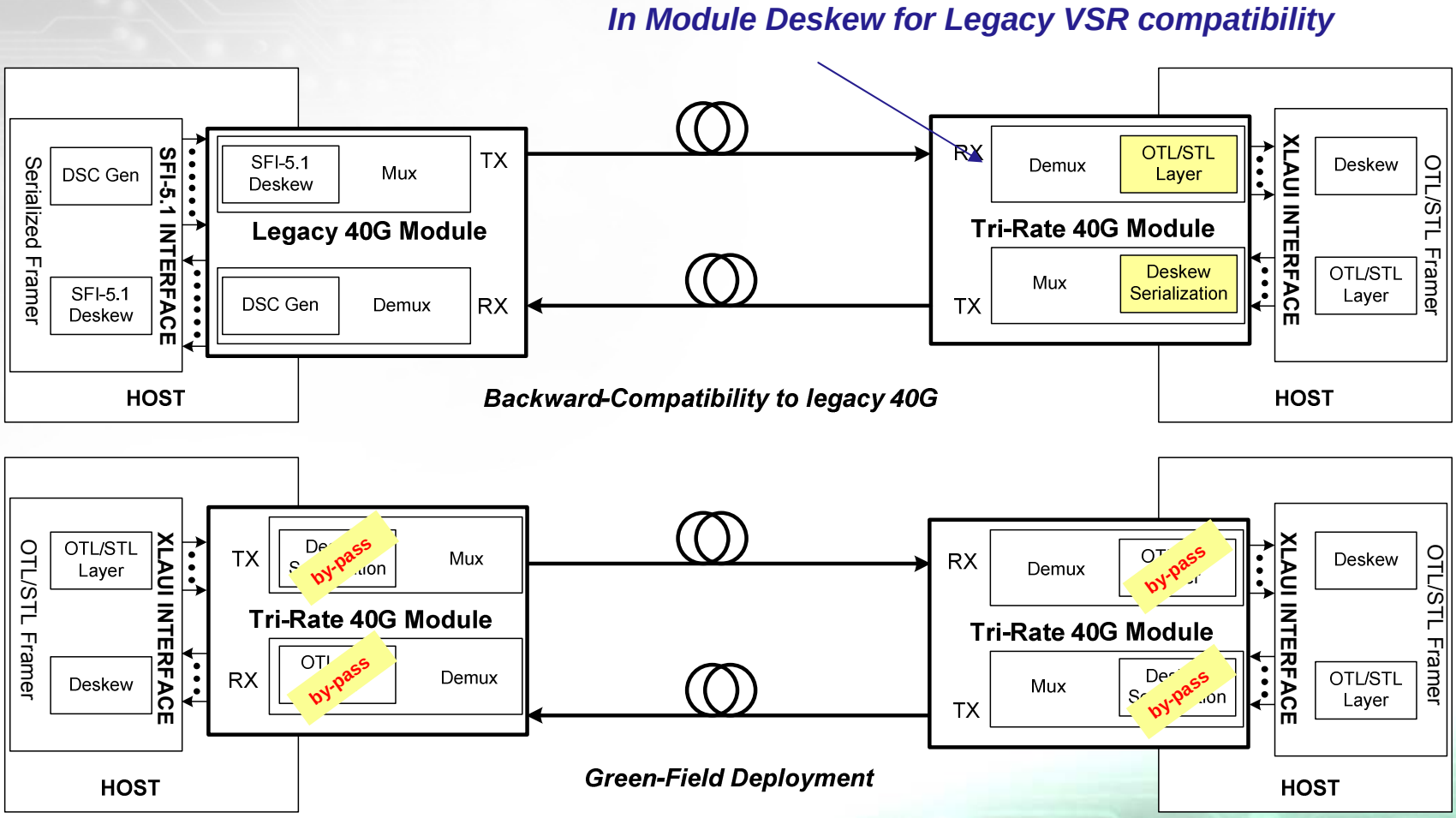
- Backward compatibility for installed VSR module (OC-768 and OTU-3)
- Future compatibility with existing IEEE802.3ba on 40GE MAC/PCS, PMA by using XLAUI interface (simple bit-Mux with deskew at far-end receiver)
- Future compatibility with OTL layer (ITU-T G.709/Y1331, Annex C) and STL layer (ITU-T G.707/Y1322, Annex I)

Optional in-module deskew based on STL256.4 and OTL3.4 can meet these requirements

- What is the required deskew budget?
  1. ASIC implementation for Framer/FEC
  2. FPGA implementation for Framer/FEC

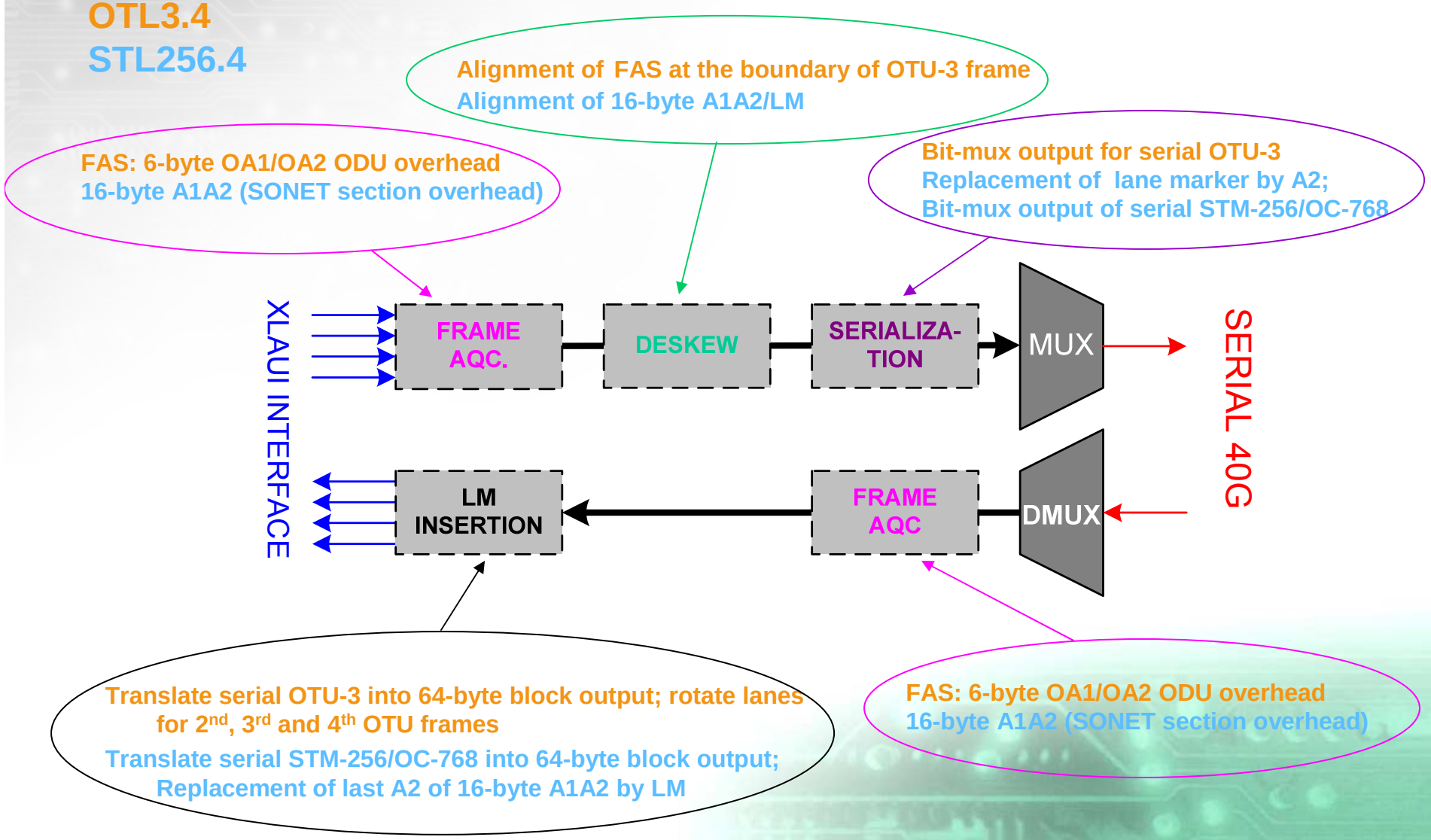
Even though deskew is out of the scope of 40Gb/s Ethernet Single-mode Fibre PMD technically, a consensus on deskw mechanism and budget is important for inter-operability for tri-rate module

Example of Tri-Rate Module Connections



Implementation of Optional In-Module deskew functions

OTL3.4
STL256.4



Skew Budget in OIF SFI-S IA

Interface skew budget from Tx direction:

Skew Contributor	Skew Budget @ 6.25 Gbps	Skew Budget @ 11.2 Gbps	Skew Budget [ps]
CEI TX Interface @ package pins (Te)	3.13 UI	5.50 UI	500
PCB and Connector	0.3 UI	0.6 UI	50
Subtotal @ package pins (Res)	3.43 UI	6.10 UI	550
Serdes Input	0.3 UI	0.6 UI	50
Total	3.75 UI	6.70 UI	600

Table 3: Channel to Channel Skew Budget for FEC processor/Framer to Serdes Link

Normative spec for deskew budget

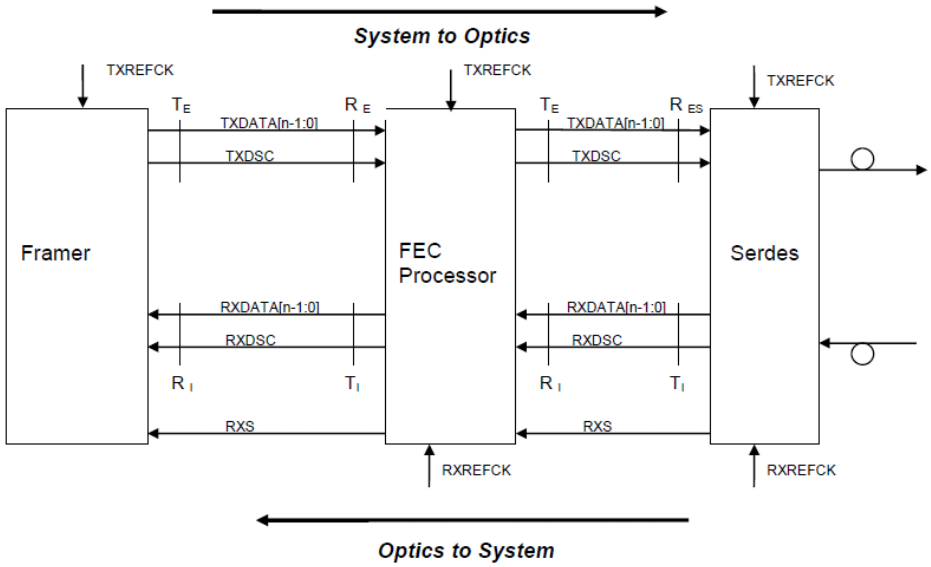


Figure 1: System Reference Model

Recommended deskew budget

13 **Appendix A: Recommended extended static Skew Compensation Capability**

It is recommended that SFI-S Receivers are designed to tolerate a minimum of 84 U.I. of static skew at test points RES, RI, and RE. This provides the same skew tolerance as in the informative recommendation for SFI-5.2 receivers.

Skew Budget derived from 802.3ba

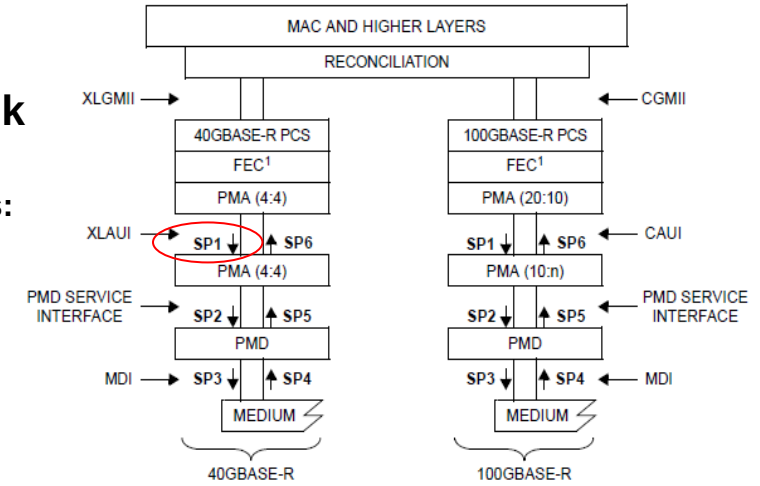
Table 80–4—Summary of Skew constraints

Skew Points	Maximum Skew (ns)[a]	Maximum Skew for 40GBASE-R PCS lane (UI)[b]	Maximum Skew for 100GBASE-R PCS lane (UI)[c]	Notes[d]
SP1	29	≈ 299	≈ 150	See 83.5.3.1.
SP2	43	≈ 443	≈ 222	See 83.5.3.3 or 84.5 or 85.5 or 86.3.2 or 87.3.2 or 88.3.2.
SP3	54	≈ 557	≈ 278	See 84.5 or 85.5 or 86.3.2 or 87.3.2 or 88.3.2
SP4	134	≈ 1382	≈ 691	See 84.5 or 85.5 or 86.3.2 or 87.3.2 or 88.3.2
SP5	145	≈ 1495	≈ 748	See 84.5 or 85.5 or 86.3.2 or 87.3.2 or 88.3.2
SP6	160	≈ 1649	≈ 824	See 83.5.3.5
At PCS receive	180	≈ 1856	≈ 928	See 82.2.12.

- Even though 802.3ba skew budget does not apply to interface skew between Framer/FEC to tri-rate module (802.3bg project), the analysis here is to show the deskew budget for a FPGA implementation for framer/FEC

- The detail skew budget for PCS with FPGA implementation has been analyzed by 802.3ba task force presentation(giannakopoulos_01_0508) :
  - ~299UI (255UI) was derived using 64-bit i/f to external 10G Serdes: 128UI (2x64) internal FPGA and the remaining 127UI from external Serdes

- New gen. FPGAs all have internal 10G Serdes, therefore the max skew budget will be 128UI for 64-bit wide and 80UI for 40-bit wide internal Serdes bus



Summary

- In-Module deskew function is not required to be specified for 40GE in 40Gb/s Ethernet Single-mode Fibre PMD specs
- For tri-rate module, deskew functions based on STL256.4 and OTL3.4 can meet the interoperability requirement to the legacy VSR modules
- Suggest to include two separate in-module deskew budgets as "informative" in 40Gb/s Ethernet Single-mode Fibre PMD document:
  1. Minimum deskew budget: 8UI
  2. Maximum deskew budget: 128UI

Q & A

SEMTECH

Thank You!

Supporting Material

OTL3.4 Structure

OTU-3 Frame

	1					4080
1	1:16 (FAS)	17:32	33:48	49:64	• • • •	4065:4080
2	4081:4096	4097:5012	5013:5028	5029:5044		9145:9160
3	9161:9176	9177:9192	9193:9208	9209:9224		12225:12240
4	12241:12256	12257:12272	12273:12288	12289:13304		16305:16320

64-byte block distribution over 4 lanes

	MFAS = xxxx xx00				Rotate	MFAS = xxxx xx01			Rotate	MFAS = xxxx xx10			Rotate	MFAS = xxxx xx11			Rotate	
	1	2		255	256		510	511		765	766		1020	1				
Lane 0	1:16 (FAS)	65:80	• • •	16247:16272	49:64	• • •	16305:16320	33:48	• • •	16289:16304	17:32	• • •	16263:16288	1:16 (FAS)				
Lane 1	17:32	81:96		16263:16288	1:16 (FAS)		16247:16272	49:64		16305:16320	33:48		16289:16304	17:32				
Lane 2	33:48	97:112		16289:16304	17:32		16263:16288	1:16 (FAS)		16247:16272	49:64		16305:16320	33:48				
Lane 3	49:64	113:128		16305:16320	33:48		16289:16304	17:32		16263:16288	1:16 (FAS)		16247:16272	49:64				

- *Each 16-byte increment of an OTU3 frame is distributed, round robin, to each of the four physical lanes. On each OTU3 frame boundary, the lane assignments are rotated.*

- *For OTU3, the lane rotation and assignment is determined by the two LSB of the MFAS, which indicates the starting group of bytes of the OTU3 frame that are sent on each lane.*

- *The pattern repeats over each 64 bytes until the end of the OTU3 frame.*

Table C.1/G.709/Y.1331 - Lane rotation assignments for OTU3

MFAS 7-8	Lane 0	Lane 1	Lane 2	Lane 3
*00	1:16	17:32	33:48	49:64
*01	49:64	1:16	17:32	33:48
*10	33:48	49:64	1:16	17:32
*11	17:32	33:48	49:64	1:16

From Annex C, ITU-T G.709

STL256.4 Structure

STM-256/
OC-768 Frame

	1					69120
1	1:16	17:32	33:48	49:64		69105:69120
2	69121:69136	69137:69152	69153:69168	69169:69184		138225:138240
3	138241:138256	138257:138272	138273:138288	138289:138304		207345:207360
4	207361:207376	207377:207392	207393:207408	207409:207424		276465:276480
5	276481:276496	276497:276512	276513:276528	276529:276544	• • •	345585:345600
6	345601:345616	345617:345632	345633:345648	345649:345664		414705:414720
7	414721:414736	414737:414752	414753:414768	414769:414784		483825:483840
8	483841:483856	483857:483872	483873:483888	483889:483904		552945:552960
9	552961:552976	552977:552992	552993:553008	553009:553024		622065:622080

64-byte block distribution over 4 lanes

								Next frame	
Lane 0	1:16	65:80	• • •	705:720 (A1)	769:784 (A2)	• • •	622017:622032	1:16	• • •
Lane 1	17:32	81:96		721:736 (A1)	785:800 (A2)		622033:622048	17:32	
Lane 2	33:48	97:112		737:752 (A1)	801:816 (A2)		622049:622064	33:48	
Lane 3	49:64	113:128		753:768 (A1)	817:832 (A2)		622065:622080	49:64	

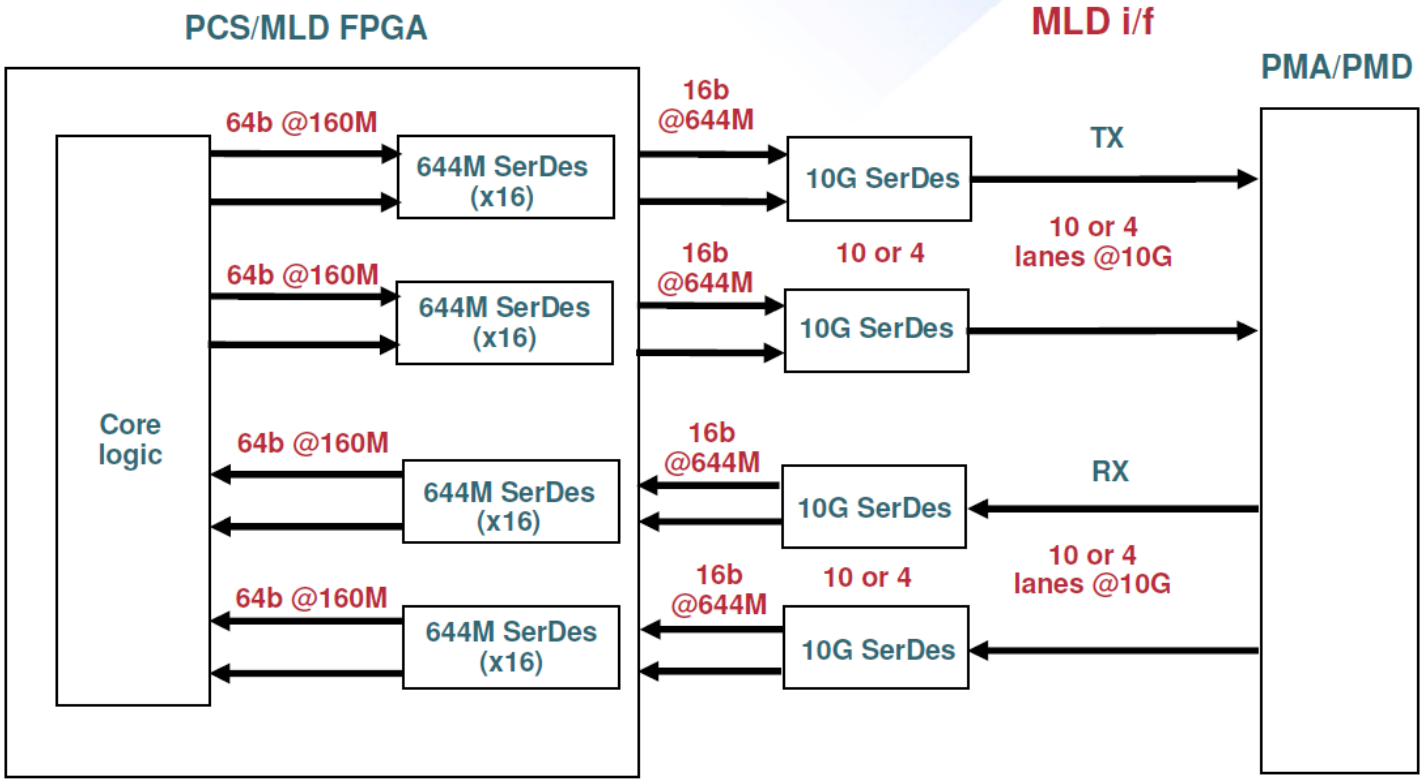
The last A2 of the 16-byte A1A2 is borrowed as lane marker:
Lane Marker Value:

Lane 0: 0, 4, …, 252
Lane 1: 1, 5, …, 253
Lane 2: 2, 6, …, 254
Lane 3: 3, 7, …, 255

The logic lane number can be recovered by a modulo-4 operation
When deskew is finished, Lane maker is replaced by A2 for serial STM-256/OC-768

From Annex I, ITU-T G.707

PCS/MLD skew – FPGA case



MLD i/f: 10 lanes for 100 GE or 4 lanes for 40GE @10G

Giannakopoulos_01_0508 (IEEE 802.3ba)