Rapid alignment marker performance

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Introduction

As part of the discussion on EEE support for 100GbE in the IEEE P802.3bj Task Force, it has been proposed to use Rapid Alignment Markers (RAM) to enable alignment of the PCS lanes to be achieved much more quickly than would otherwise be possible. See:

http://www.ieee802.org/3/bj/public/nov11/gustlin_02_1111.pdf

As discussed on slide 12 of gustlin_02_1111, as the RAM bits are not scrambled, care must be taken to ensure that the use of these markers does not compromise the clock content or baseline wander properties of the resulting signal.

This presentation is an initial look at this issue.

Assumptions

The assumptions used in the RAM analysis contained in this presentation were:

- Rapid alignment markers use the same codes as normal markers except for the BIP fields
- The CD (ex BIP_3) byte is the M_0 byte exclusive OR'd with a count down from 47 to 0 (5 us of RAM)
- The !CD (ex BIP_7) byte is the inverse of the CD byte
- There are 7 /LI/ 66B blocks between adjacent RAM markers. /LI/ is 0x1E then 8 times 0x06, scrambled

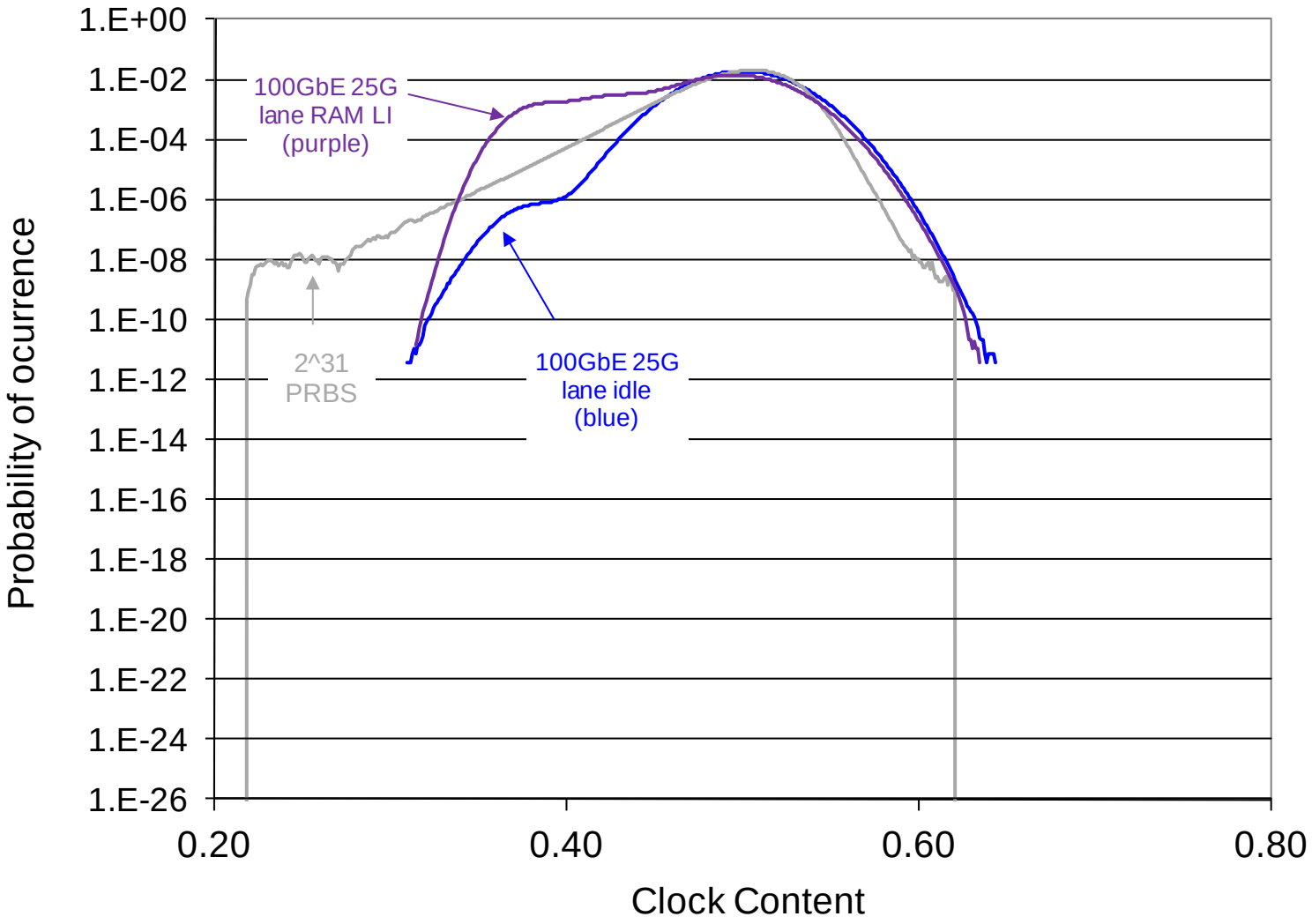
Analysis

Baseline wander for the RAM data isn't an issue because the alignment markers have been chosen to contain equal numbers of ones and zeros.

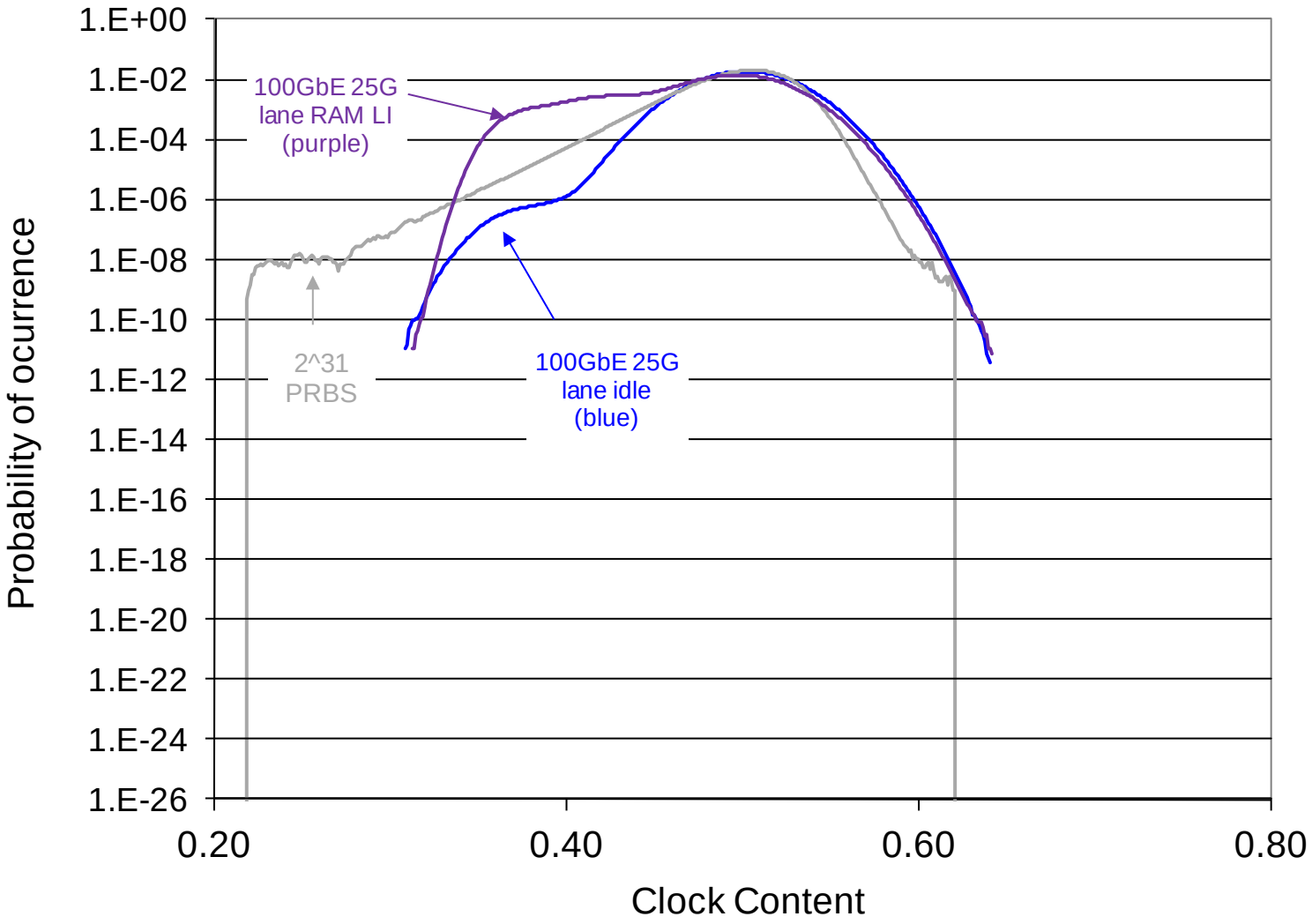
For clock content, the worst case for the choice of skew values and PCS lanes interleaved to form the 25G physical lane depends on the clock content of the data at the start of the interleaved markers. For the previous analysis on 100GbE, this was assumed to be 0.32 which is approximately the once in 10,000 year limit for 64B/66B encoded random binary.

The choice of this value for the RAM case where there are only 7 blocks of scrambled /LI/ between markers is not clear. This presentation therefore analyses the "book-end" cases of 0.32 and 0.5 in the next two slides.

Clock content – worst skew starting at CC=0.32



Clock content – worst skew starting at CC=0.5



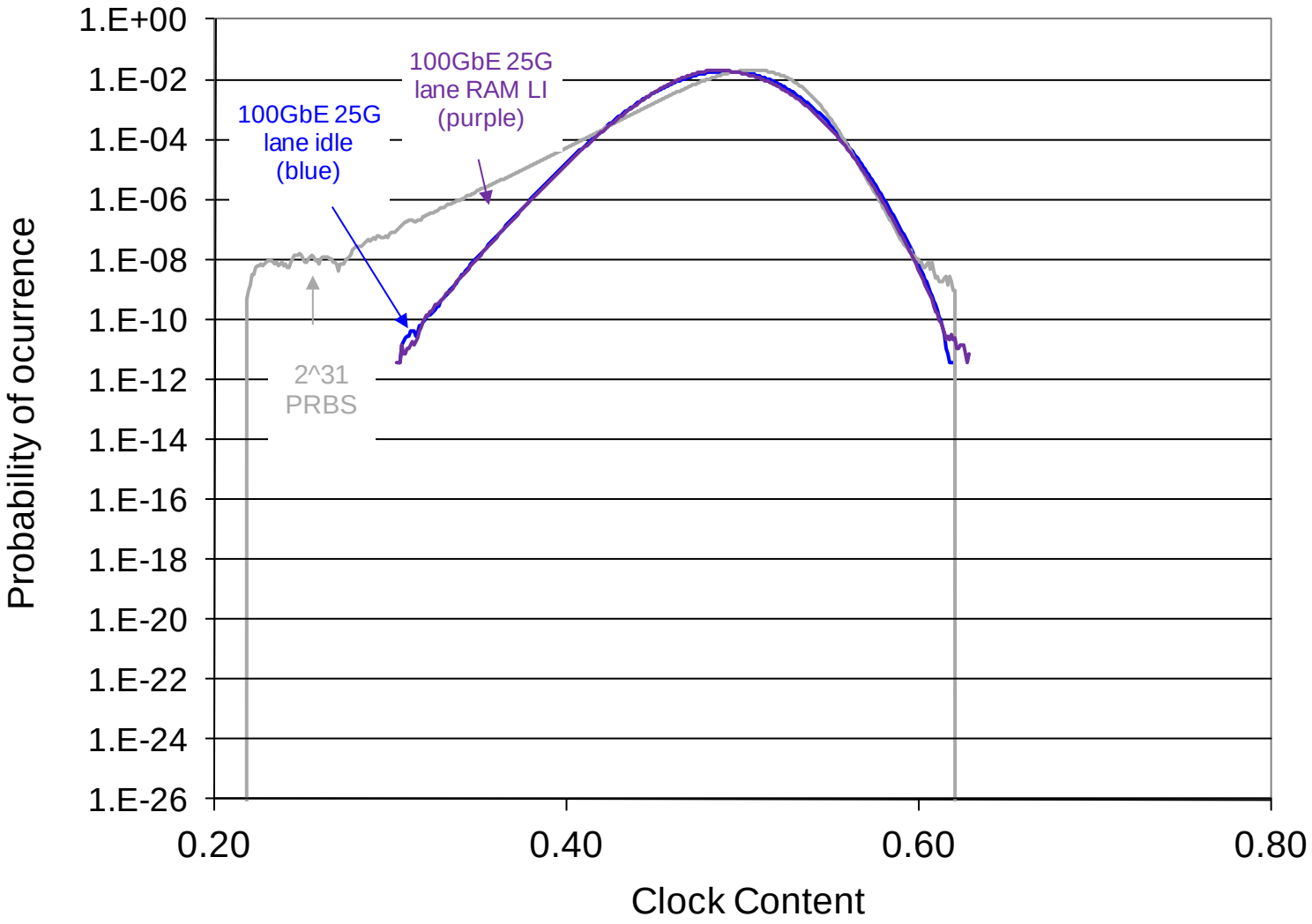
Results

As can be seen from the previous two slides, the worst case AM set assuming CC=0.32 before the markers (which is 1 3 12 18 4 with skew 0 -3 1 3 -3) gives CC PDFs for RAM and normal markers that have almost the same CC at the lowest probability simulated.

Likewise, the worst case AM set assuming CC=0.5 before the markers (which is 10 6 2 8 3 with skew 0 2 -3 -2 3) also gives CC PDFs for RAM and normal markers that have almost the same CC at the lowest probability simulated.

For reference, one further pair of simulations for PCS lanes 0 1 2 3 4 with skew 0 0 0 0 0 are given on the next slide.

Clock content – no skew



Conclusions

The clock content PDFs for RAM and normal markers have almost the same clock content at the lowest probability simulated for the cases of worst case skew with CC=0.5 before the markers, worst case skew with CC=0.32 before the markers and no skew lanes 0 to 4.

This suggests that the clock content during rapid alignment marker periods is no worse than that of idle 100 Gb Ethernet.

Thanks!