



MTTFPA Estimation for 100 Gb/s Backplane and Copper Cable

IEEE 802.3bj Task Force

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TC and FEC Options for NRZ Signaling

- Transcoding (TC) and FEC options for NRZ signaling considered in gustlin_01_0112

0% overclocking

- A1**: 512b/513b TC and RS(528,513), m=10
- A2**: 512b/514b TC and RS(528,514), m=10
- B1**: 512b/516b or 256b/258b TC and RS(528,516), m=10
- B2**: 512b/513b TC and RS(468,456), m=9

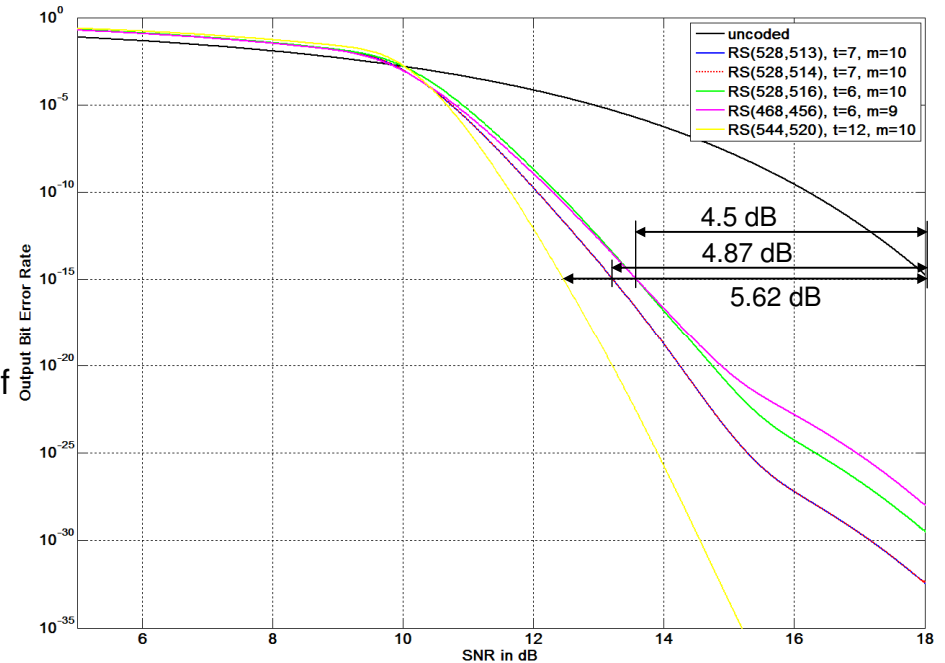
3% overclocking

- C**: 64b/65b TC and RS(544,520), m=10

- A1** and **A2** correct t=7 symbols in a FEC block consisting of 528 symbols and provide **4.87 dB** coding gain to achieve target BER 1e-15. Both options have same latency.
- B1** corrects t=6 symbols in 528 symbols and has **4.52 dB** coding gain. B1 has smaller latency than A1 and A2.
- B2** corrects t=6 symbols in 468 symbols and has **4.51 dB** coding gain. It has 20% smaller FEC block size and smaller symbol size than B1.

MTTFPA = average time between undetected MAC frame errors

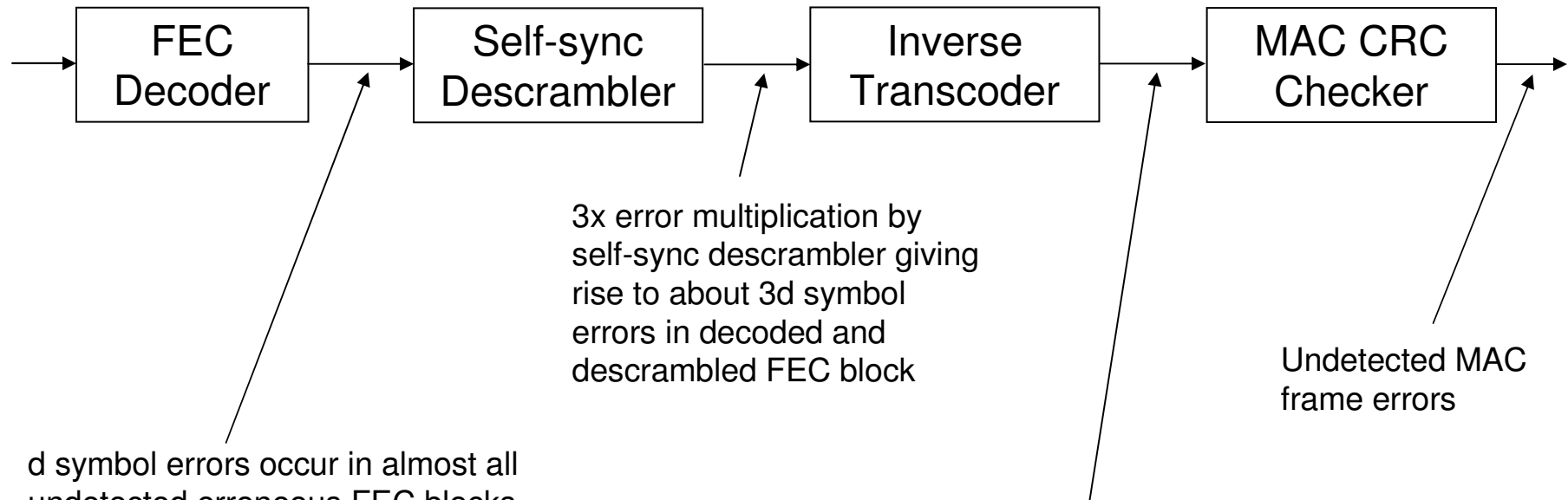
RS(n,k) codes with m-bit symbols correct t error symbols in n-symbol FEC block



Probability that next bit in a burst at DFE output is in error is b=0.5 for all computations in this presentation

How can we compute the Mean Time To False Packet Acceptance (MTTFPA)?

Undetected MAC Frame Errors



d symbol errors occur in almost all undetected erroneous FEC blocks where $d = n - k + 1$ is the minimum distance of the $RS(n,k,t,m)$ code

3x error multiplication by self-sync descrambler giving rise to about $3d$ symbol errors in decoded and descrambled FEC block

Undetected MAC frame errors

Each decoded and descrambled FEC block contains 8 or 10 transcoded 512b blocks. Undetected FEC block errors that are detected by inverse transcoder can be reported to PCS by changing the header of every 8th 66-bit block to “11” as described in section 74.7.4.5 of IEEE 802.3 standard.

Undetected MAC frame errors occur if undetected FEC block errors are not detected by inverse transcoder and MAC CRC checker.

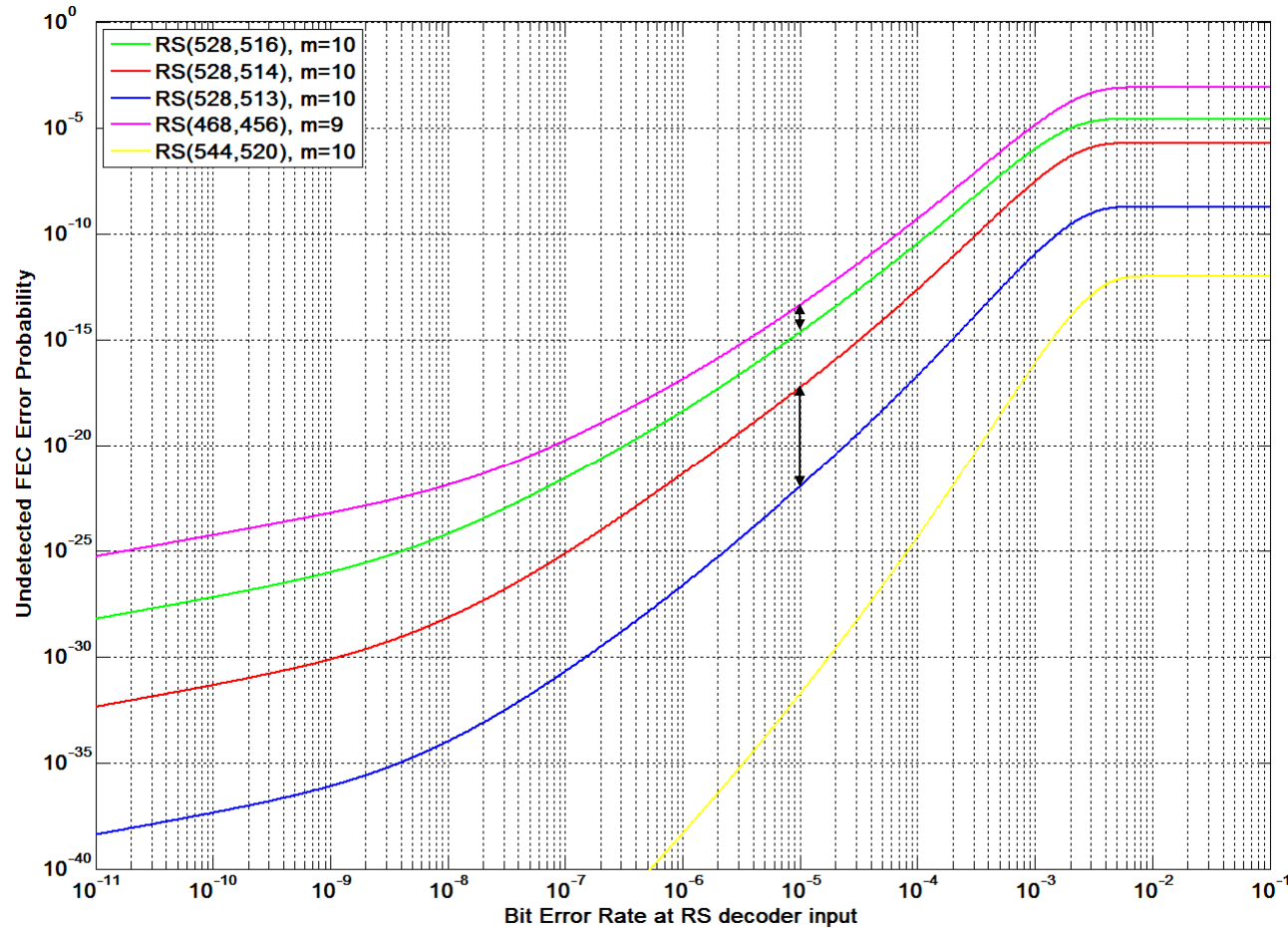
Undetected FEC Block Error Probability

- If there are $t = \text{floor}((n-k)/2)$ or less symbol errors in a FEC block, RS decoder corrects all errors in a FEC block.
- If more than t symbol errors in a FEC block occur, there are two possible cases:
 - 1) RS decoder fails to decode FEC block and reports to MAC layer that retransmission is required.
 - 2) RS decoder makes an undetected error because it finds a legal code word other than the transmitted code word. Most undetected FEC block errors are usually detected by inverse transcoder or CRC checker in MAC layer and therefore result in retransmission of an erroneous MAC frame.
- Dominant term in the probability of undetected FEC block errors P_{un}

$$P_{\text{un}} \approx (2^m - 1)^{-(d-t-1)} \binom{n-d+t}{t} \Pr\{d-t \text{ symbol errors}\}$$

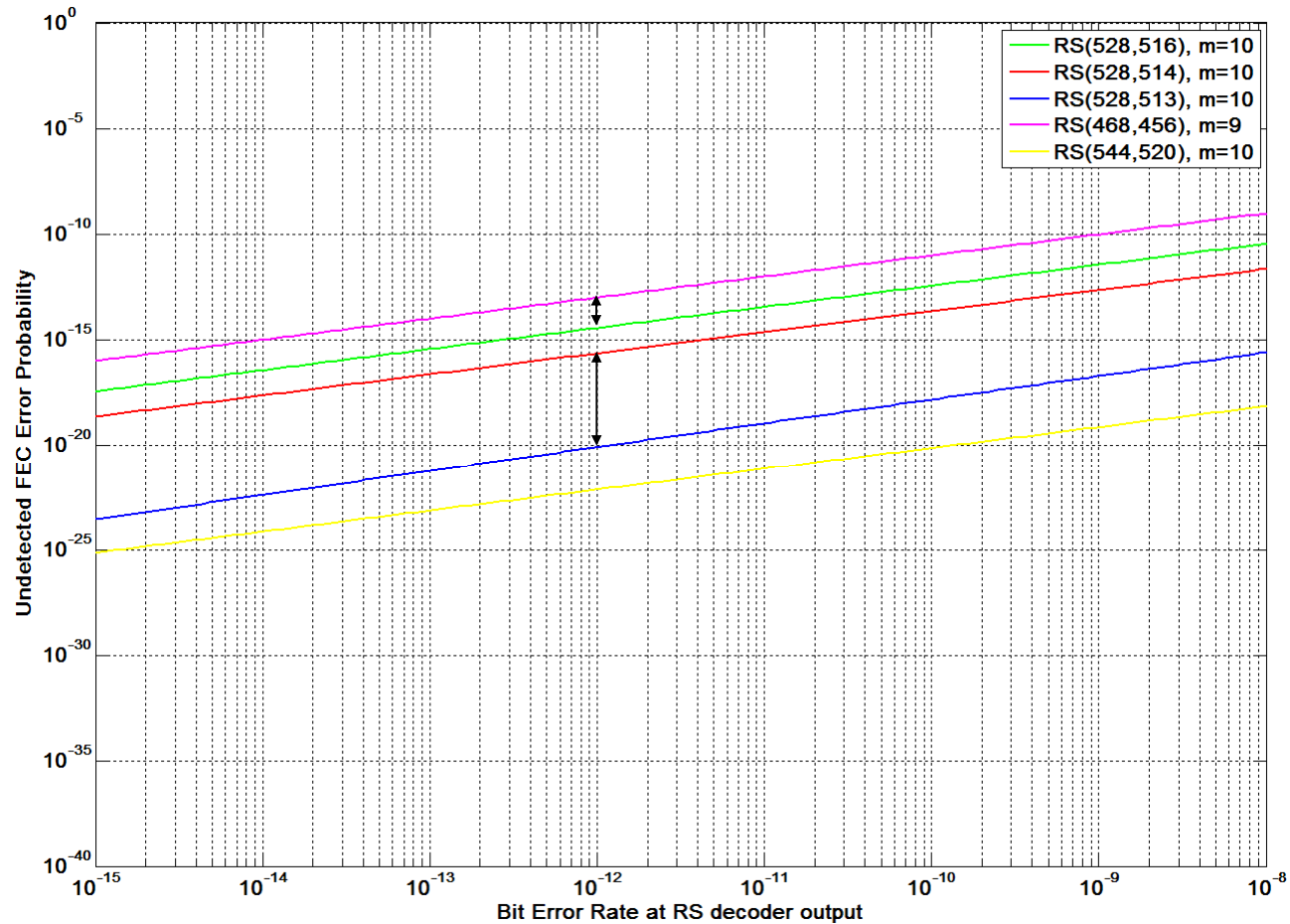
- For the RS(528,513) $m=10$ code: $P_{\text{un}} \approx 1.61 \times 10^{-9} \Pr\{9 \text{ symbol errors}\}$
- For the RS(528,514) $m=10$ code: $P_{\text{un}} \approx 1.67 \times 10^{-6} \Pr\{8 \text{ symbol errors}\}$

Undetected FEC Block Error Probability vs. DFE BER



RS(528,513) has 100,000x less undetected FEC errors than RS(528,514) at DFE BER=1e-5.
RS(528,516) has 10x less undetected FEC errors than RS(468,456) at DFE BER=1e-5.

Undetected FEC Block Error Probability vs. Target BER



RS(528,513) has 28,100x less undetected FEC errors than RS(528,514) at target BER=1e-12.
RS(528,516) has 27x less undetected FEC errors than RS(468,456) at target BER=1e-12.

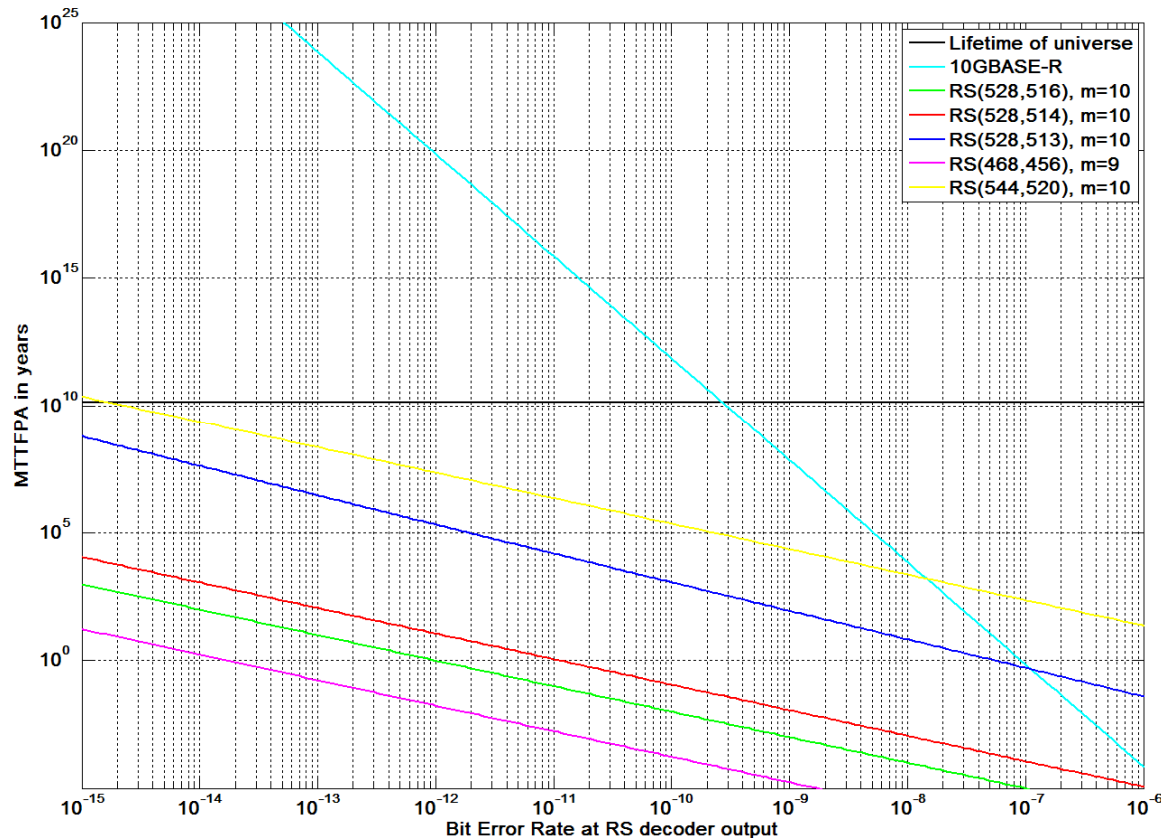
Descrambler and Inverse Transcoder

- Most undetected FEC block errors contain d symbol errors. For example, undetected FEC block errors at RS(528,513) decoder output usually contain $d=16$ erroneous symbols whereas undetected FEC block errors at RS(528,514) decoder output usually contain $d=15$ erroneous symbols. Similarly, undetected FEC block errors at RS(528,516) decoder output usually contain $d=13$ erroneous symbols.
- Due to 3x error multiplication at descrambler output there are usually about $3d$ undetected symbol errors per FEC block at descrambler output
- Percentage of error patterns in decoded FEC block not detected by inverse transcoder
 - 512b/514b TC and RS(528,514) code: $\sum_{i=0}^{10} \binom{10}{i} \left(\frac{3d}{n}\right)^i \left(\frac{511}{1023}\right)^i \left(1 - \frac{3d}{n}\right)^{10-i} = 65\%$
 - 512b/516b or 256b/258b TC and RS(528,516) code: $\sum_{i=0}^{20} \binom{20}{i} \left(\frac{3d}{n}\right)^i \left(\frac{511}{1023}\right)^i \left(1 - \frac{3d}{n}\right)^{20-i} = 47\%$
 - All 512b/513b TC options are assumed not to be able to detect errors

All transcoding options have very weak error detection capability

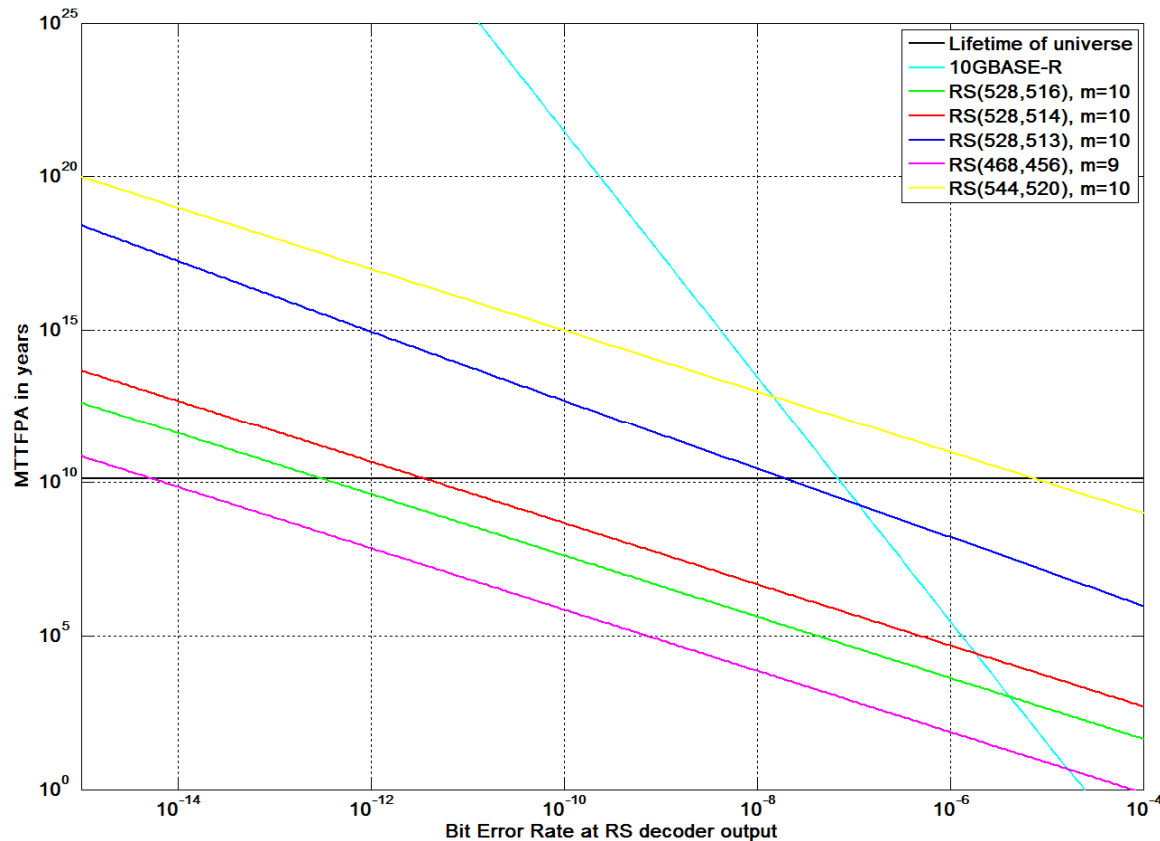
Conservative MTTFPA Estimate

- MAC Frame size = 1280 bytes = payload of 2 FEC blocks
- Conservative MTTFPA estimate computed similar to the approach taken by Rick Walker in walker_1_0300 for lower bounding MTTFPA of 10GBASE-R by not accounting for the CRC detection factor 2^{32}



MTTFPA Estimate including 2^{32} CRC Factor

- MAC Frame size = 1280 bytes = payload of 2 FEC Blocks
- MTTFPA estimate multiplied by CRC detection factor $2^{32} \approx 4 \cdot 10^9$
- Working assumption of 2^{32} CRC factor valid if the probability of undetected error patterns at the input of CRC checker that map into the zero syndrome is $1/2^{32}$ of the probability of all undetected error patterns at the input of CRC checker





Conclusion

- Analyzed MTTFPA for various TC and FEC options considered by the 802.3bj task force
- 0% overclocking: 512b/513b TC and RS(528,513) m=10 code provides the best error rate performance and MTTFPA
- 512b/513b TC and RS(528,513) m=10 code provides >10,000x improvement in MTTFPA when compared to 512b/514b TC and RS(528,514) m=10 code
- 512b/514b TC and RS(528,514) m=10 code has good MTTFPA if the CRC factor 2^{32} is included in the MTTFPA computation. However, there is no analysis supporting this.
- 512b/516b or 256b/258b TC and RS(528,516) m=10 code provides 80x improvement in MTTFPA when compared to 512b/513b TC and RS(468,456) m=9 code
- 3% overclocking: 64b/65b transcoding and RS(544,520) code provides better error rate performance and better MTTFPA than all 0% overclocking options



References

- [1] E. R. Berlekamp and J. L. Ramsey, “Readable erasures improve the performance of Reed-Solomon codes,” *IEEE Trans. Inform. Theory*, vol. 24, pp. 632-633, Sep. 1978.
- [2] R. J. McEliece and L. Swanson, “On the decoder error probability for Reed-Solomon codes,” *IEEE Trans. Inform. Theory*, vol. 32, pp. 701-703, Sep. 1986.
- [3] L. M. G. M. Tolhuizen, “A universal upper bound on the miscorrection probability with bounded distance decoding for a code used on an error-value symmetric channel,” *Eurocode 1992*, CISM Courses and Lectures no. 339, Springer Verlag, Wien-New York, pp. 313-320.