MLSD/DFE Based Transceivers with a Partially Terminated Trellis

for IEEE 802.3bj 100Gb/s Backplane and Copper Assemblies

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Agenda

- Introduction
- Construction for Low Overhead Termination Symbols
- Transmitter
- Precoder Implementation
- MLSD Implementation
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- DFE Error Detection Using Termination Symbols
- Combined MLSD/DFE Implementation
- RS Erasures Using Termination Symbols
- Conclusions

Introduction

- Termination symbols introduced in dabiri_01_0911 enabled independent detection of the segments of the trellis with no overlap.
- Goals for this presentation:
  - Introduce a new scheme that reduces the overhead of termination symbols for the same block length, and still enables no-overlap detection of trellis segments.
  - Show how termination symbols could be used for DFE error detection that allows for:
    - Selective enabling of the MLSD detectors in order to save power.
    - Intelligent erasure marking for the RS decoder.

Construction

- The terminated trellis of in dabiri_01_0911 was constructed by forcing the state of the trellis to be known for every M symbols.
  - Termination overheard is 1/M for blocks of size M.
- In the new construction the state of the trellis is <u>not fully</u> known for every M symbols.
- The state of the trellis is known to be either -3 or 3:
  - An information bit is used to select between the two levels:
    - Therefore the overhead is now 1/(2M).
  - An alternative method is described in the back up slides.
- It can be shown the minimum Euclidean distance of the paths on the finite trellis segment is: $2\sqrt{2}$
  - Therefore VA algorithm maintains the 3 dB asymptotic gain.
    - Termination bits have a *<u>pre-FEC</u>* error floor of 10^-19.

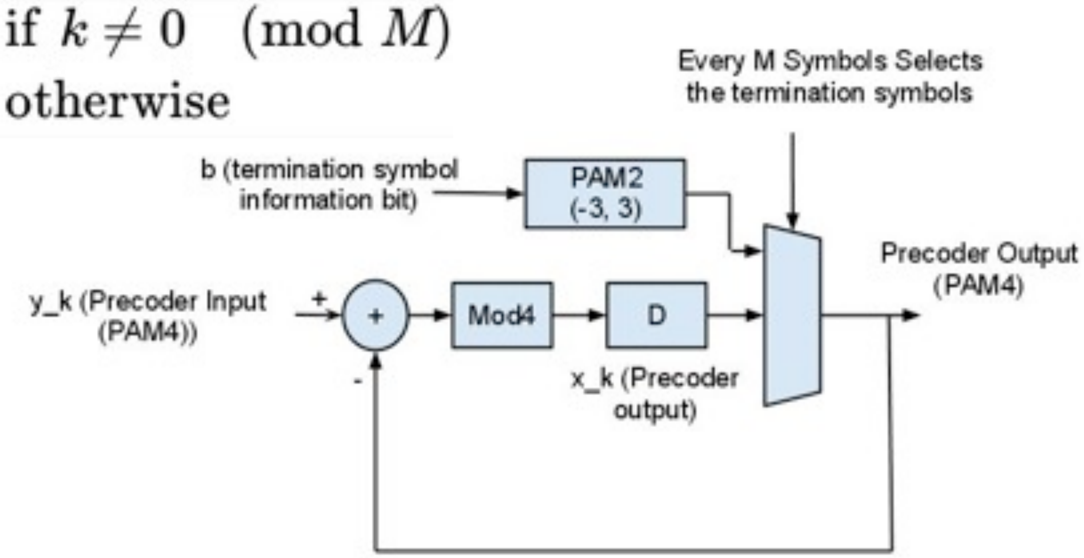
Transmitter

- In dabiri_01_0911 each termination symbol was determined by two bits generated from a PRBS sequence:
  - Therefore it carries no information bit.
- In the new scheme, the termination symbol is a PAM2 level and therefore it carries one information bit.
  - Block termination symbols are introduced every 32 symbols.
  - Details of the frame structure can be found in brown_01_0112.
- Information bit of the termination symbols enjoys more protection (extra 9dB) of PAM2 signaling: {-3, 3}:
- Slight power variation every M symbols: (no spectral line)
  - Alternative construction without power variation is doable.

Precoder Implementation

- Each termination symbol is used to reset the state of the precoder for every M symbols.
- The information bit of TS is encoded through FEC.
- The reseting scheme simplifies the precoder design by allowing overlapped operation between blocks.

$$x_k = \begin{cases} y_k - x_{k-1} \pmod{\text{PAM4}} & \text{if } k \neq 0 \pmod{M} \\ (-1)^b 3 & \text{otherwise} \end{cases}$$

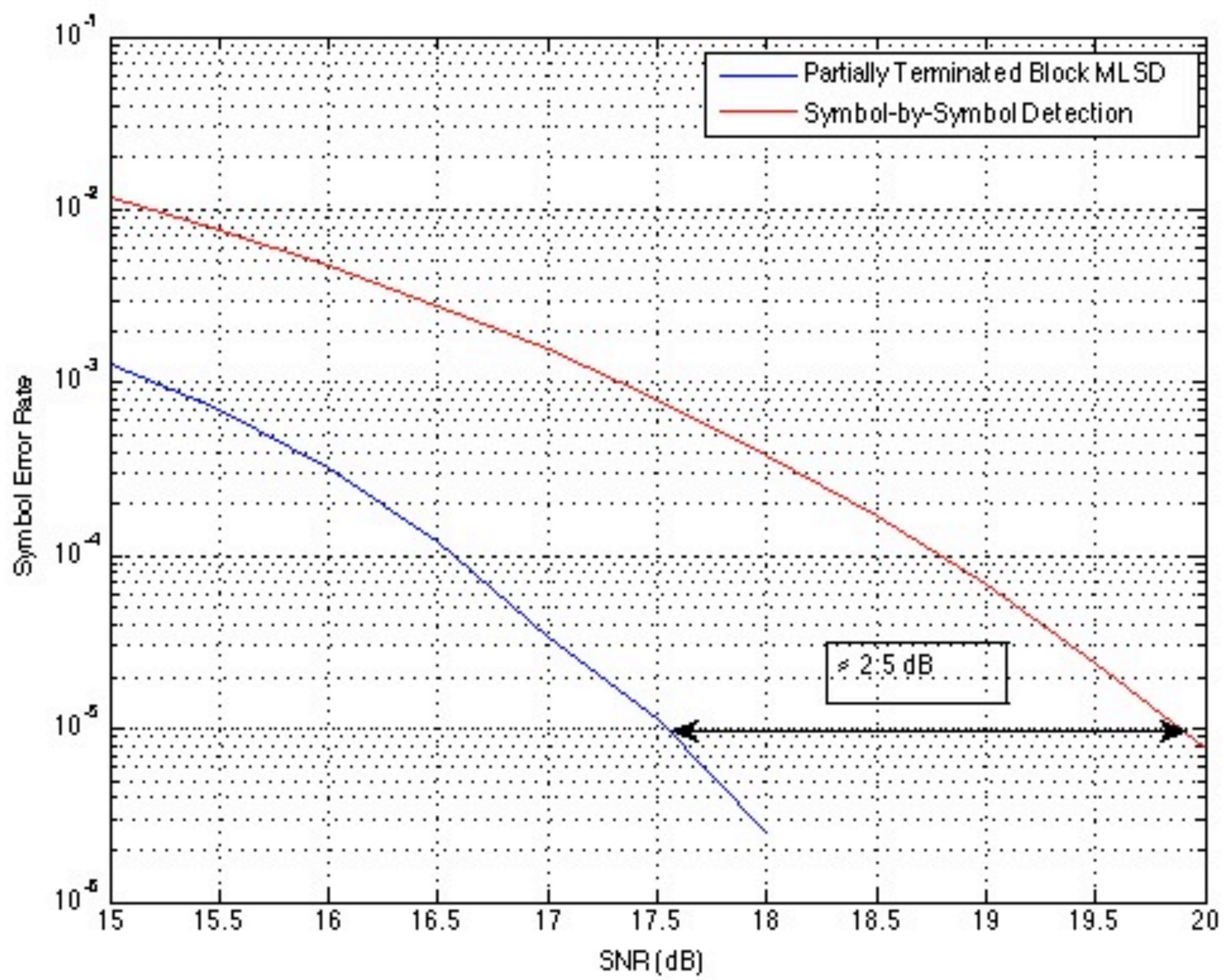


MLSD Implementation

- A 'text book' Viterbi Detector:
  - $P_k(s) = \min(P_{k-1}(t) + B_{k-1}(t \to s))$
  - for $k = 2, 3, \ldots, N$, we have $s, t \in \{-3, -1, 1, 3\}$
  - if k = 1, $t \in \{-3, 3\}$
  - if k = N+1, $s \in \{-3, 3\}$
- Traceback:
  - Starts at the state that minimizes $P_{N+1}(s)$
  - Ends at $k = 1$, i.e. no overlaps.

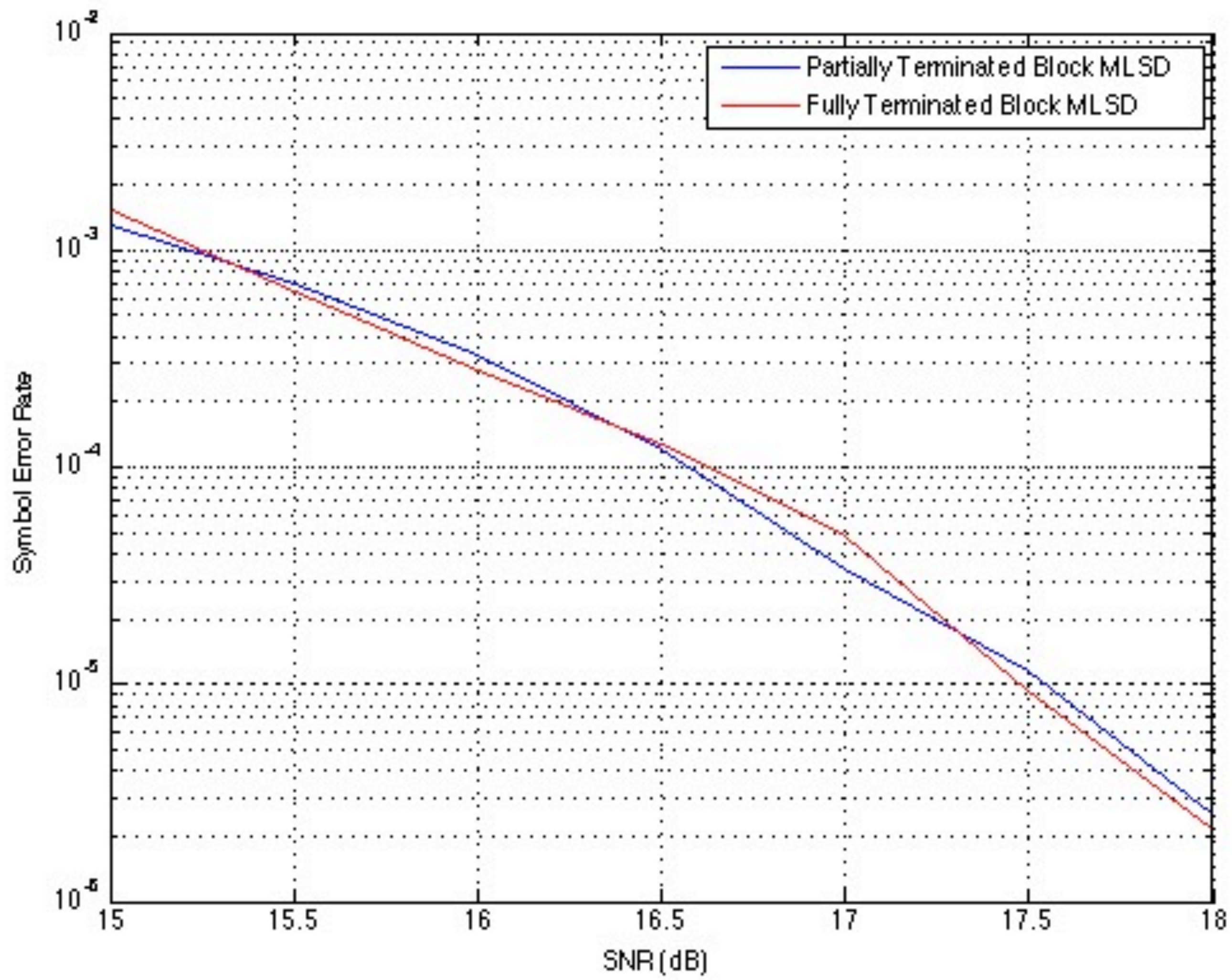
Simulation Results

- Results show the performance of the block by block detector compared to the symbol by symbol detector.



Simulation Results

- Results for full termination is almost identical with partial termination:

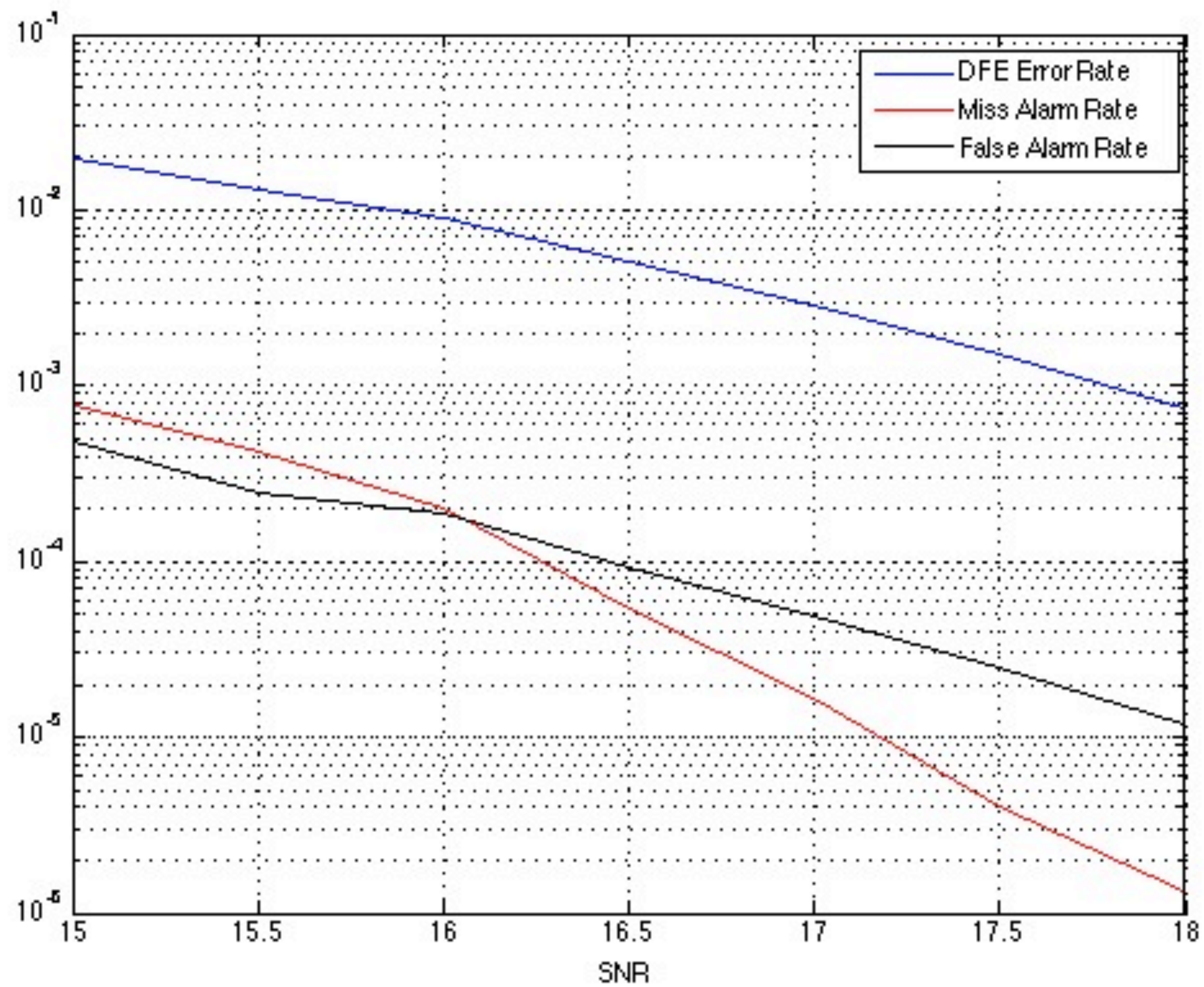


DFE Error Detection

- Error events for DFE with 1 + D (or close approximations) causes error patterns of the form +/-2 with alternating signs.
  - Error events typically end when the input to the channel is +/- 3.
  - 1+D post-processing filters most of the error patterns but the two symbols at the start and the end of the pattern.
- Main observation:
  - One can extend the error pattern if the DFE slicer is allowed to exceed the saturation levels of +/-3.
  - With a proper choice of block length, most of the error patterns can be extended to the termination symbols.
- Slicing at the termination symbols provides informations regarding to:
  - the existence of the error and the sign of the error pattern.

Simulation Results

- With a very high probability any error at the DFE can be detected at the termination symbols.



Applications to the MLSD Receiver

- MLSD arguably consumes more power than the DFE receiver.
- Using DFE error detection one can only enable MLSD only when DFE makes an error.
- Relatively short length of the termination blocks allows for low latency implementation.
- Low latency implementations of the Viterbi Algorithm are discussed in:
  - J. J. Kong and K. K. Parhi, 'Low-Latency Architectures for High-Throughput Rate Viterbi Decoders', IEEE Trans. VLSI Systems, Vol. 12, No. 6, June 2004.
  - R. Liu and K. K. Parhi, 'Low-Latency Low Complexity Architectures for Viterbi Decoders', IEEE Tans. CAS, Reg. Papers, Vol.56, No. 10, Oct. 2009.

Application to Erasure Decoding

- After 1 + D post processing typically two errors are created:
  - One at the beginning of the error pattern.
  - One at the end of the error pattern.
- One can rely on the error detection of the termination symbols to declare erasure for error/erasure RS decoding algorithms.
- Note that one can correct twice as many erasures with the same RS code compared to error only correction.

Sign of Error Detection

- Sign of the error of the pattern can be detected at the termination symbol.
- One can correct for the second error generated after 1+D post-processing.
- For the same SNR the number of errors that the RS decoder needs to correct can be reduced by as much as 1/2.

Conclusions

- Termination symbols provide opportunities for a variety of receiver implementations for both DFE and MLSD:
  - Low power combined DFE/MLSD implementation.
  - Performance improvements of the RS decoder by declaring erasures or pre-correction of the tail bit of the error pattern.
- Termination symbols allows for shorter latency and power by allowing independent detection of non-overlapping segments of the trellis.

Backups

Constant Power Termination Symbols

- Here the PAM2 levels are defined as {-3, 1}.
- No variation in power.
- Need sign randomization in order to avoid spectral lines.
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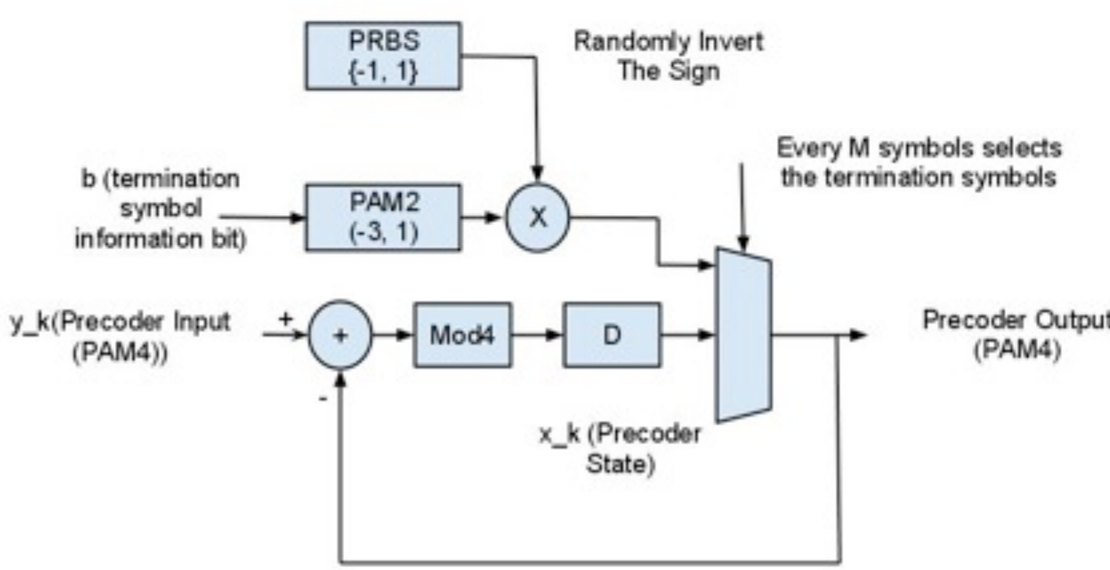

Proof:

- Definitions:
  - $X^{(l)} = \left\{ x_k^{(l)} \right\}$: Input vector of the channel
  - $Y^{(l)} = \left\{ y_k^{(l)} \right\}$: Output sequence of the channel
  - $y_k^{(l)} = x_k^{(l)} + x_{k-1}^{(l)}$
  - $\Lambda^{(l)} = x_M^{(l)} + (-1)^{M+1} x_0^{(l)} = \sum_{j=0}^{M-1} (-1)^j y_{M-j}^{(l)}$
  - $x_M^{(l)}, x_0^{(l)} \in \{-3, 3\} \Rightarrow \Lambda^{(l)} \in \{-6, 0, 6\}$
  - $\Delta = \Lambda^{(1)} - \Lambda^{(0)} \in \{-12, -6, 0, 6, 12\}$

  $x_M^{(l)}, x_0^{(l)} \in (-1)^\rho \{-3, 1\} \Rightarrow \Delta \in \{-8, -4, 0, 4, 8\}$

applied micro

Proof:

- If $d_E^2(Y^{(1)}, Y^{(0)}) < 8 \Rightarrow d_E^2(Y^{(1)}, Y^{(0)}) = 4$
- Since $d_E^2 \geq 4 d_H$, implies
  - $d_H = 1$
- It means: there is only one index k such that $y_k^{(1)} \neq y_k^{(0)}$.
- It's a contradiction since:
  - $d_E^2 = 4 \Rightarrow \left| y_k^{(1)} - y_k^{(0)} \right| = 2 \Rightarrow |\Delta| = 2$
- Finally one can easily show that $d_E^2 \leq 8$, therefore:
  - $d_E^2 = 8$

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