Design Process and Technical Thoughts on a Two Channel PHY Approach

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Supporters

- Howard Frazier – Broadcom
- Mark Nowell – Cisco
- Rich Mellitz – Intel

Summary
Technical View of Nowell_01_0112

- Discuss the Design process and technical details supporting a two channel definition from a system vendor and component vendor point of view.
- This presentation is not advocating one PHY proposal over another but is arguing that the industry will be well served by IEEE developing two PHYs specs.
- Both PHY proposals have merit and will have broad market potential.

System vendor backplane decision space Review from Nowell_01_0112

- Product breadth
  - Generally a system vendor has numerous product families across product portfolio
  - Switching – low-end access to high-end core
  - Routing – low end access to high-end core
  - Transport – low-end access to high-end core
  - Server – low-end server to high-end blade server
- Wide range of initial design dates
  - Platforms designed up to 10 years ago could still be being supported. Plus, backplanes are currently being designed or are in planning today. Once design is locked they are unable to be changed for the lifetime of platform.
- Backplane is unique
  - Once a platform ships, backplane performance is key factor in EOL decision. Only the backplane and power delivery system have this level of criticality.

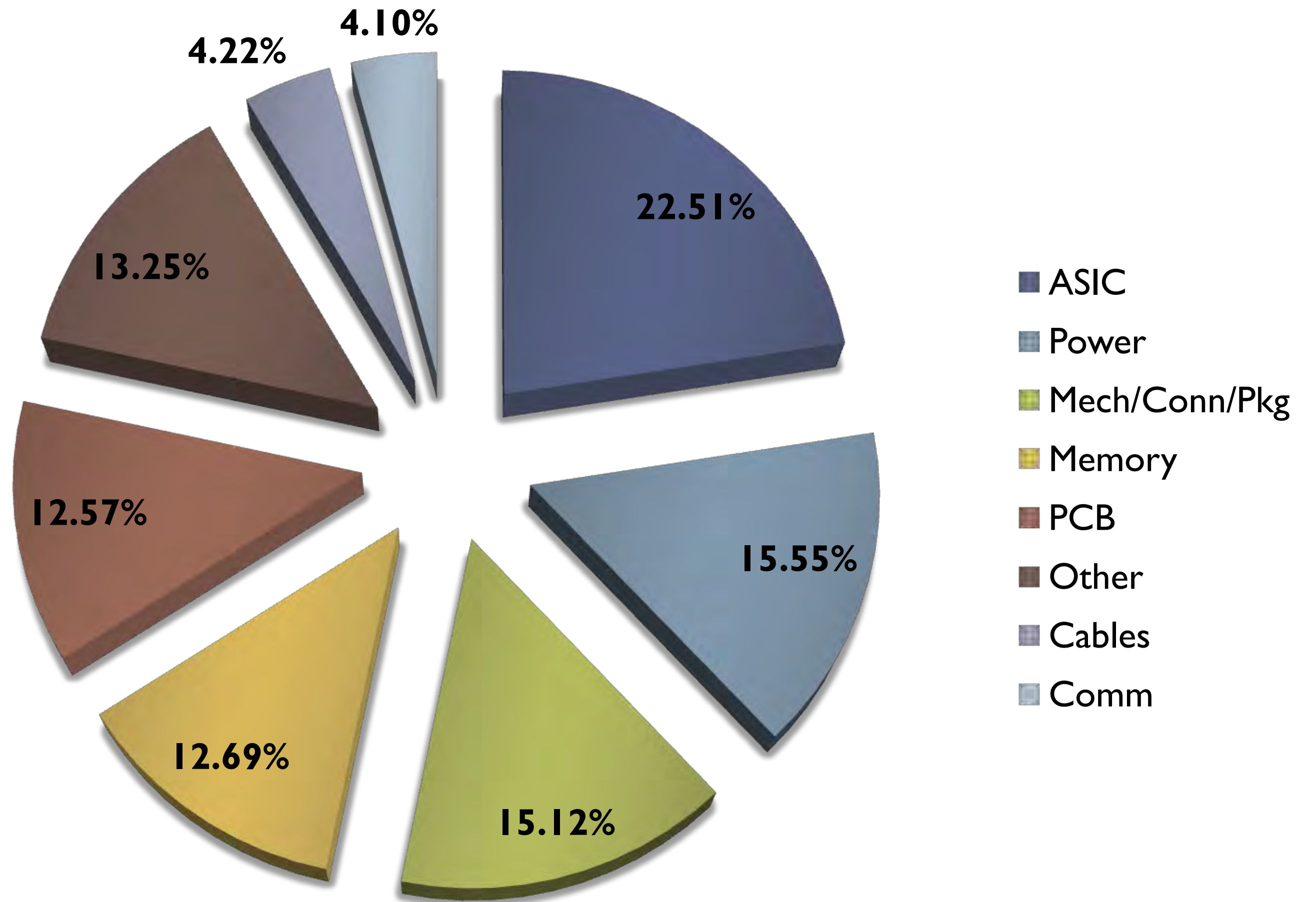
Application Debates
Deep Dive from Nowell_01_0112

- Design considerations
  - Trace length, width, thickness, surface roughness, geometries
  - Boards: board thickness, # of layers, PWB materials / glass / resin, use of counter boring
  - Cost, cost, cost….
  - etc…
- Let's Take a Deep Look at design considerations, or, more importantly, Technology Contribution …. Starting with technology trends and the Bill of Materials ….

Technology Trends of Circuit Boards Used in Switching, Routing, and Blade Servers – Low End or High End

	Board 1 18by24 Panel	**Board 2 18by24 Panel**
VIA Count	56,000 holes	52,600 holes
Etched Trace Length	31,000 inches	30,500 inches
Net Count	11,100	10,900
Placed Components	12,200	11,900

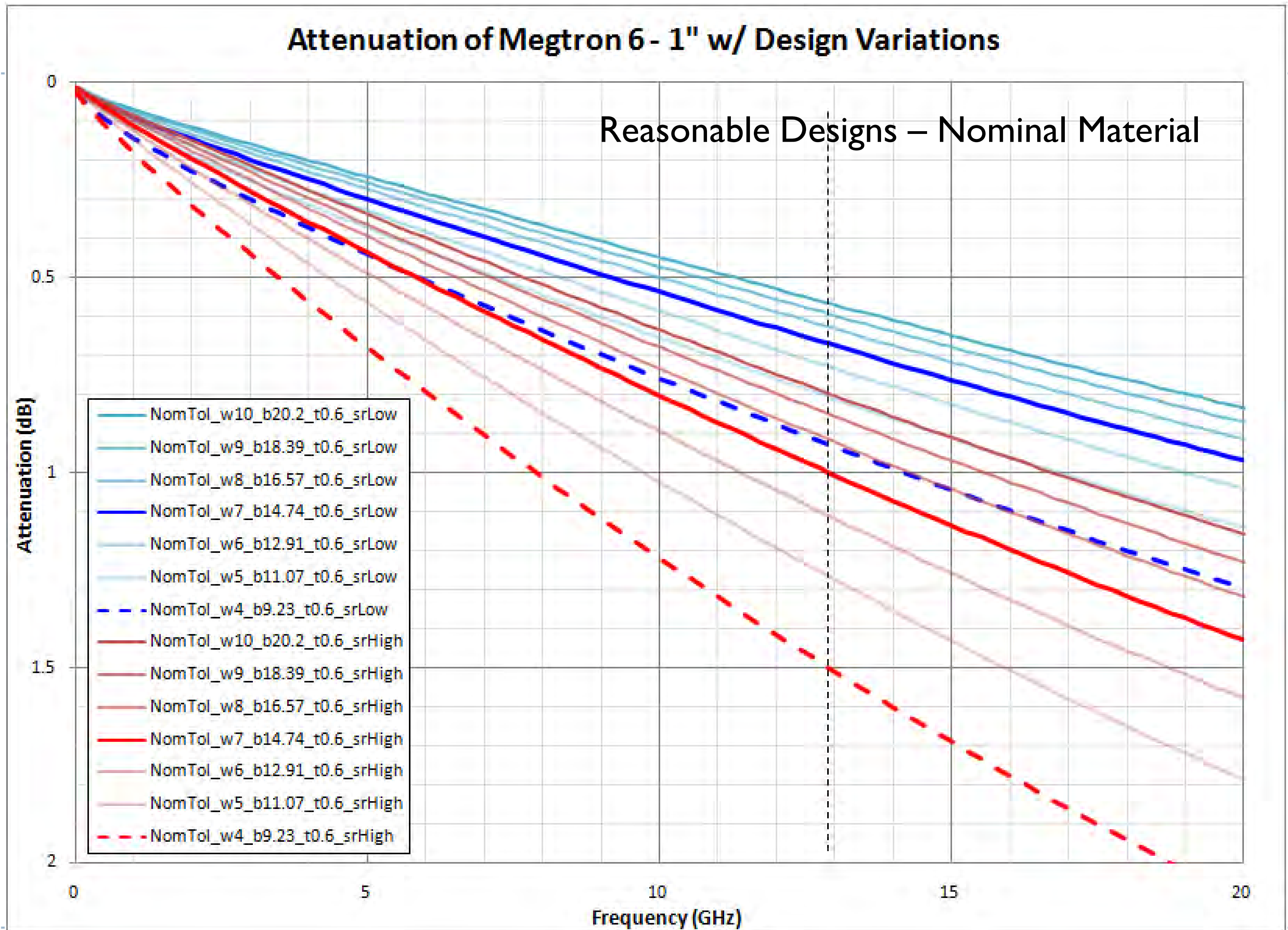
The Bill of Materials Breakdown: A Summary from Low End to High End



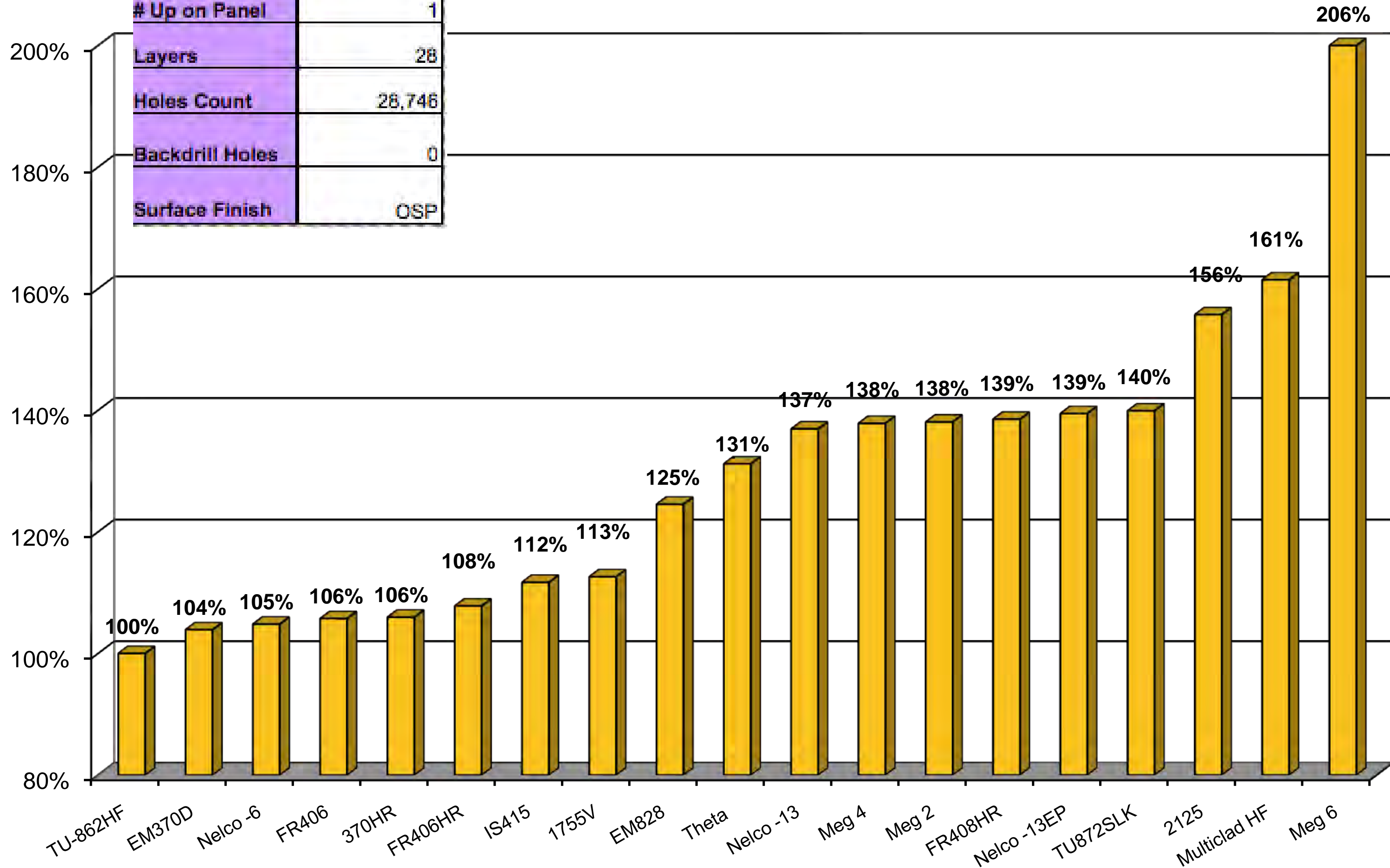
Now … Where to Focus …

- Let's analyze the technology contribution, and the cost of that contribution, specific to circuit boards.
- Low end designs may trade off technology costs for lower performance.
- High end designs may need the performance gains that value the technology costs.
- As you will see in this review … circuit board technology increases performance, and also cost ….

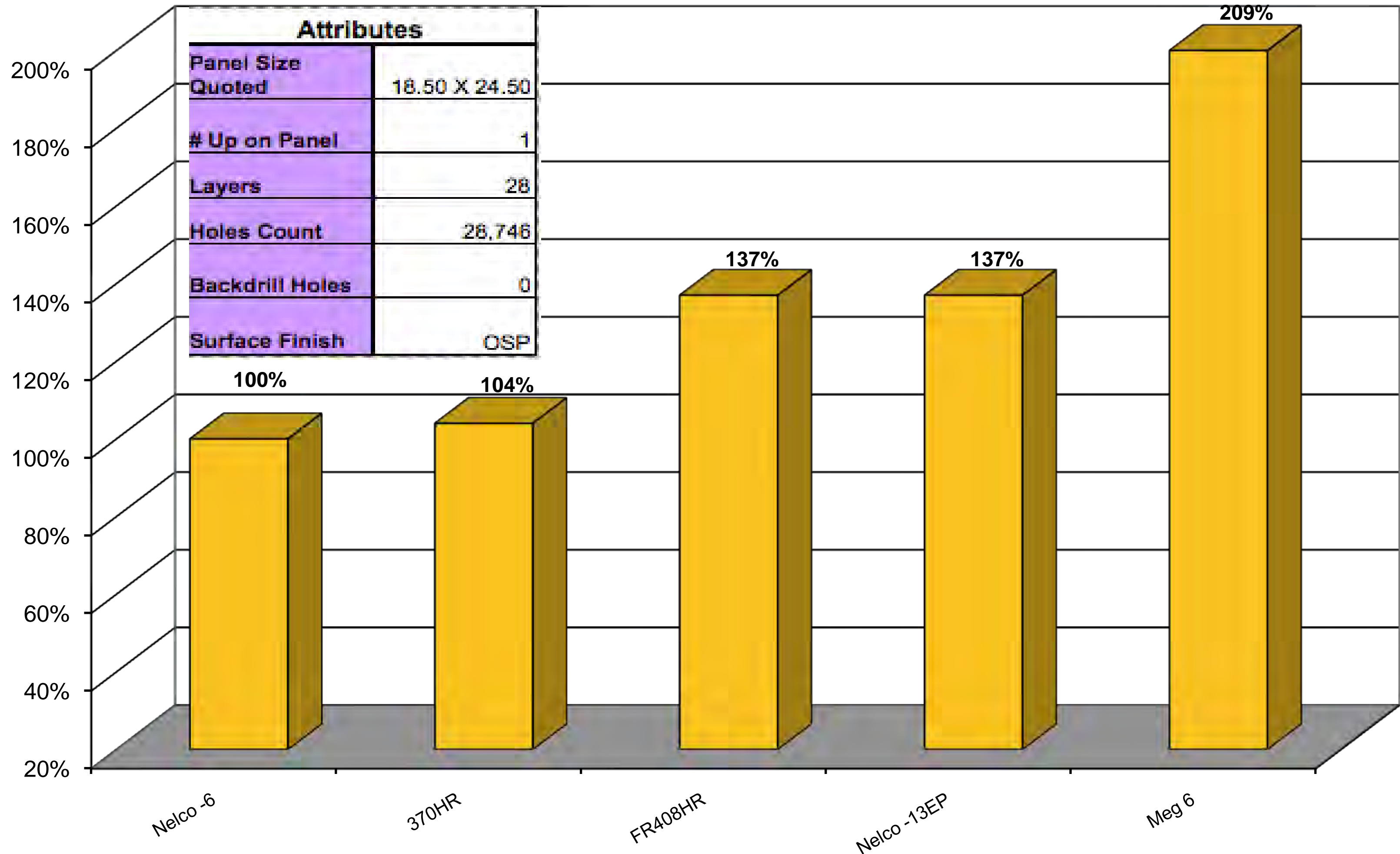
Technology Contribution: Trace Widths



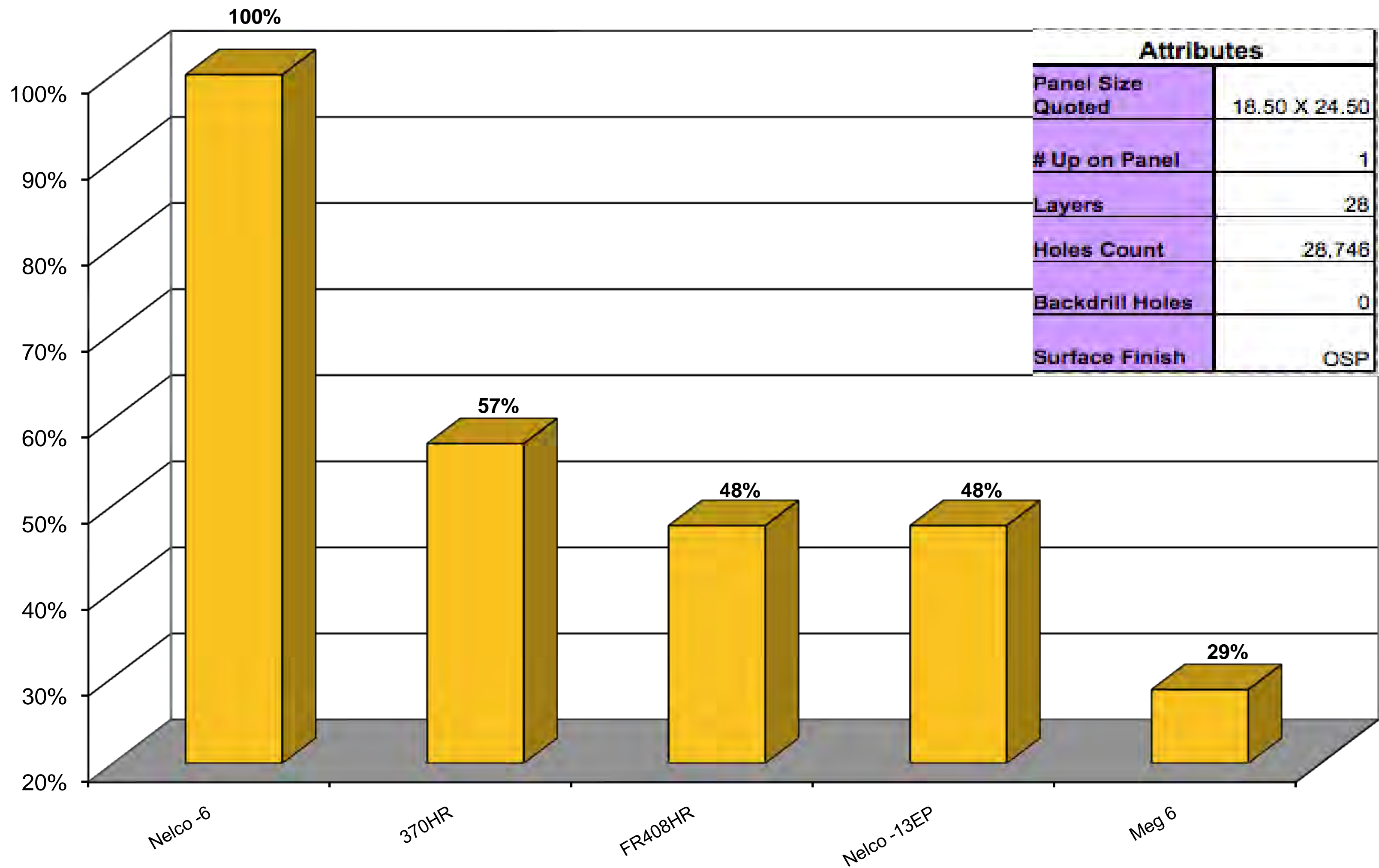
Technology Contribution: Material Cost



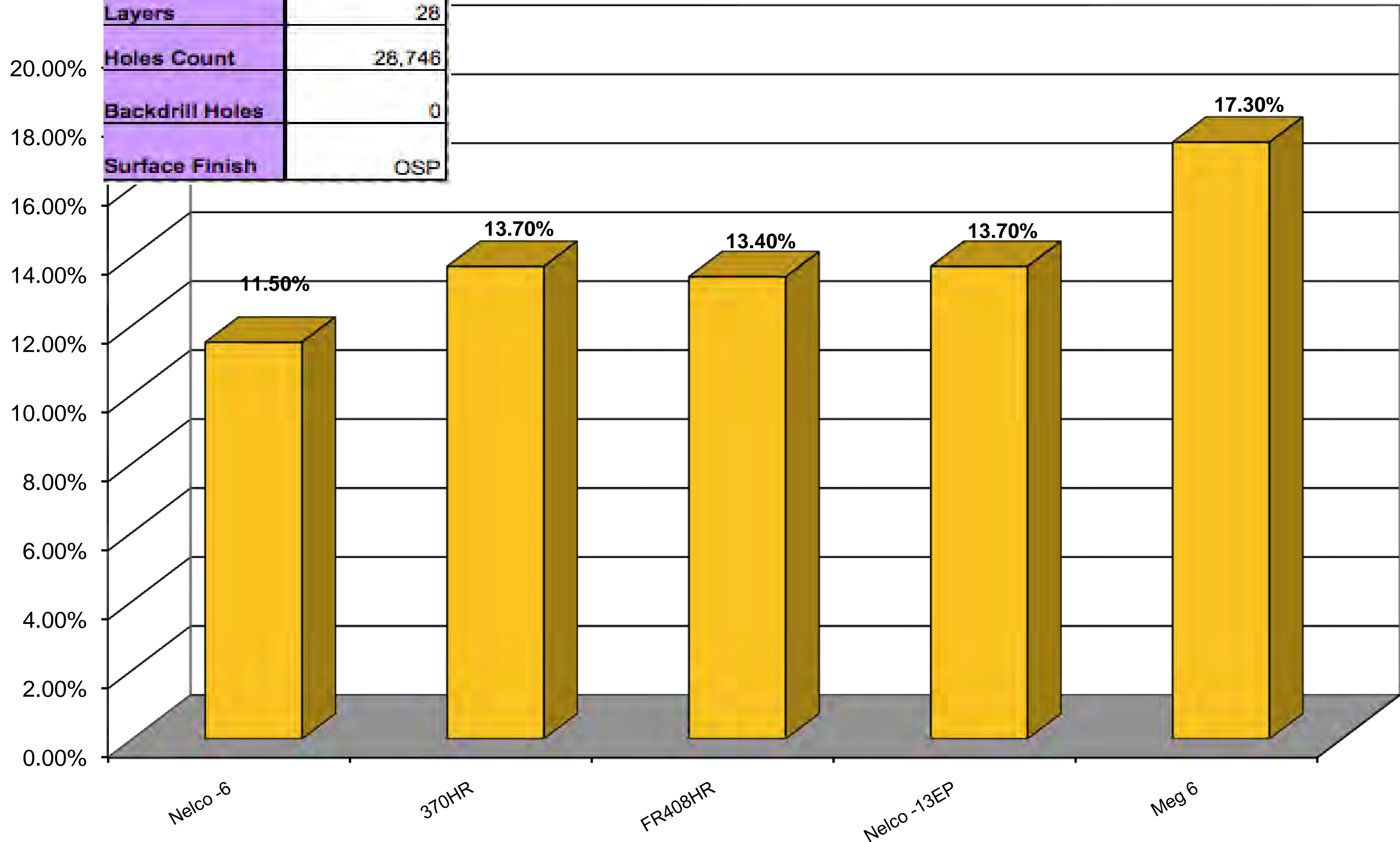
Focused Material Cost Relative to N4000-6



Technology Contribution: Drill Usage

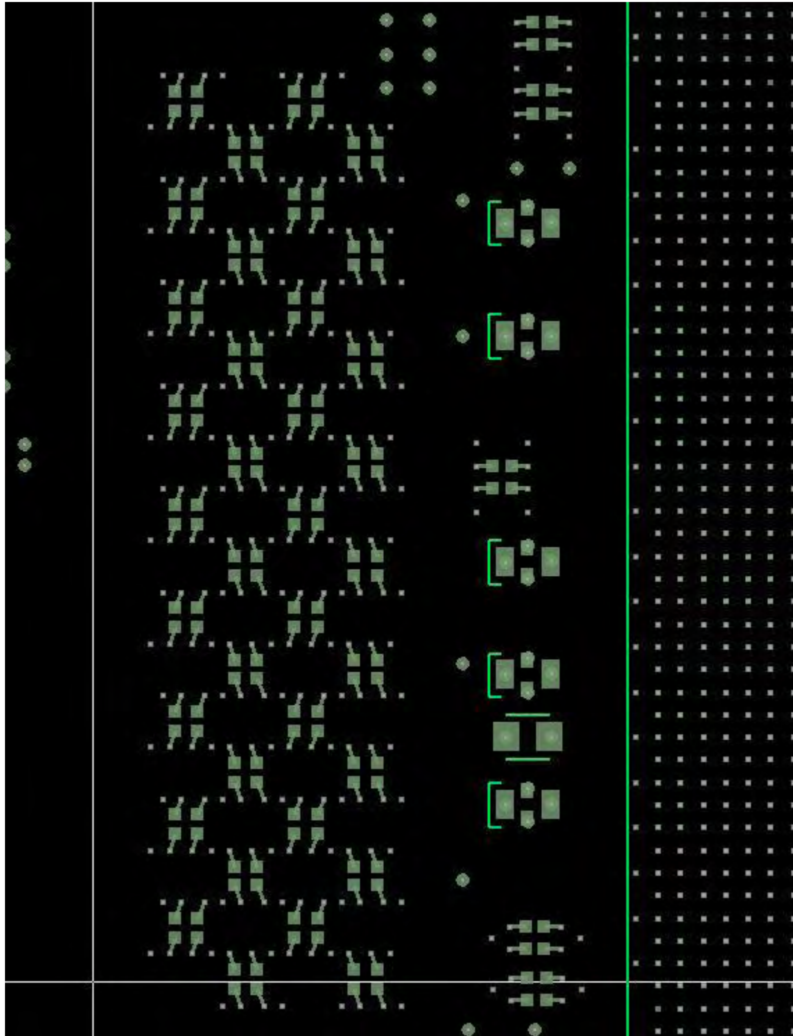


Technology Contribution: Drill Costs



Attributes	
Panel Size Quoted	18.50 X 24.50
# Up on Panel	1
Layers	28
Holes Count	28,746
Backdrill Holes	0
Surface Finish	OSP

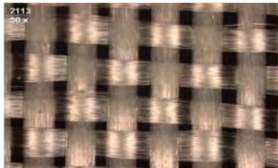
Technology Contribution: DC Blocking Capacitor Field



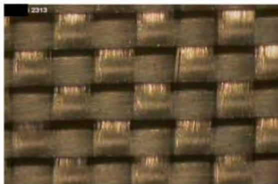
- Consumes a large area
- Requires considerable grounding to reduce common mode noise, control cross talk, and limit radiated emissions.

Technology Contribution: Glass Construction

Woven Glass Fabric isola



2113
Warp & Fill Count: 60 x 56 (ends/in)
Thickness: 0.0029" / 0.074 mm

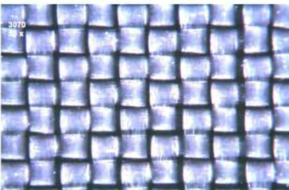


2313
Warp & Fill Count: 60 x 64 (ends/in)
Thickness: 0.0032" / 0.080 mm

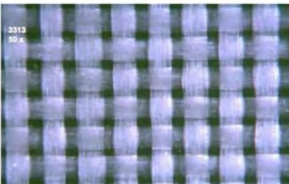
Photos courtesy of Isola R & D Laboratories

- This glass performs well for 10Gbps.

Woven Glass Fabric isola



3070
Warp & Fill Count: 70 x 70 (ends/in)
Thickness: 0.0034" / 0.086 mm



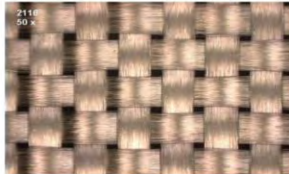
3313
Warp & Fill Count: 61 x 62 (ends/in)
Thickness: 0.0032" / 0.081 mm

Photos courtesy of Isola R & D Laboratories

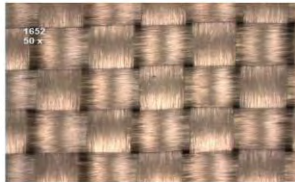
- This glass performs well for 10Gbps.

Technology Contribution: Glass Construction

Woven Glass Fabric isola



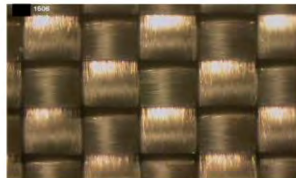
2116
Warp & Fill Count: 60 x 58 (ends/in)
Thickness: 0.0038” / 0.097 mm



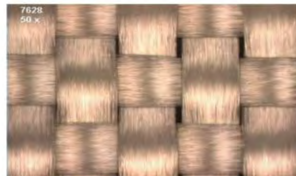
1652
Warp & Fill Count: 52 x 52 (ends/in)
Thickness: 0.0045” / 0.114 mm

Photos courtesy of Isola R & D Laboratories

Woven Glass Fabric isola



1506
Warp & Fill Count: 46 x 45 (ends/in)
Thickness: 0.0056” / 0.140 mm



7628
Warp & Fill Count: 44 x 32 (ends/in)
Thickness: 0.0068” / 0.173 mm

Photos courtesy of Isola R & D Laboratories

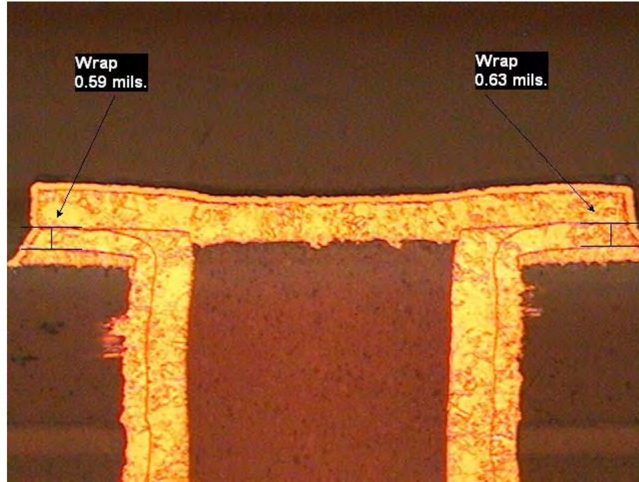
- Both Glass types behave well at 10Gbps and appear to work at speeds to 25Gbps.
- 7628 Does not perform well at high speeds in part to the Dielectric instability of the glass.

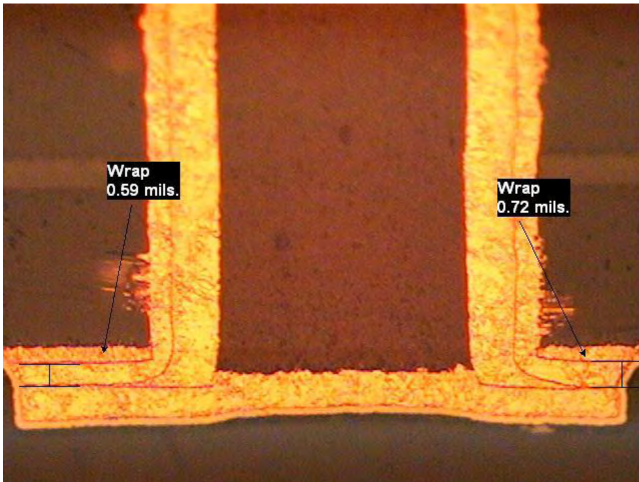
Glass Construction: Weave Position Does Make a Difference

- Figure 1. Cross sectional view of differential signal pair with very equal proximity and alignment to the fiberglass yarn bundle.

Technology Contribution: VIA in PAD Plated Over (VIPPO)

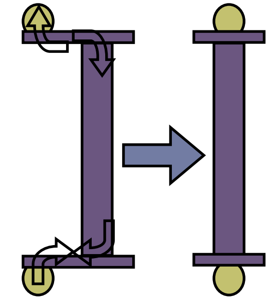
VIA in PAD

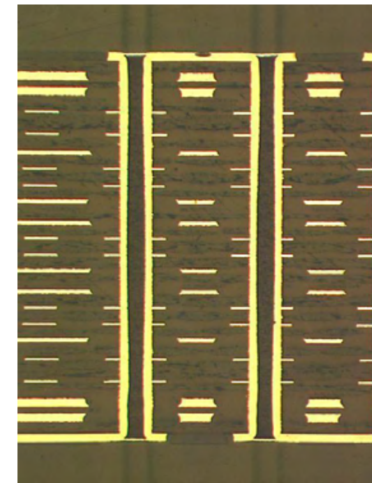




Technology Contribution: VIA in PAD Plated Over

Item	Comment
Signal Integrity	Eliminate dogbones
Routability	Very little – freed up outer layer area, but requires outer layer features and spaces
Reliability (SnPb)	Proven
Reliability (Pb-free)	No issues found yet
Supply Base	Large
Process Complexity	Moderate – additional plating, epoxy fill and planarization
Cost	~20% adder Adds processing up to 3 extra days dependant on tech level, layer count, etc
Hidden Cons	Restricted OL feature size Restricted OL spacing



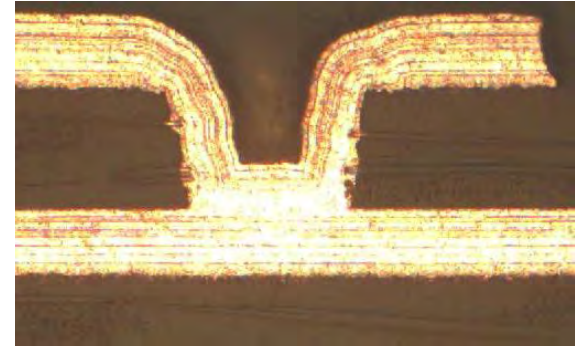


Technology Contribution: Micro VIA

- **What is it?**

  A standard through hole board with controlled depth vias (laser formed) which connect layer 1 to 2 and n to (n-1)

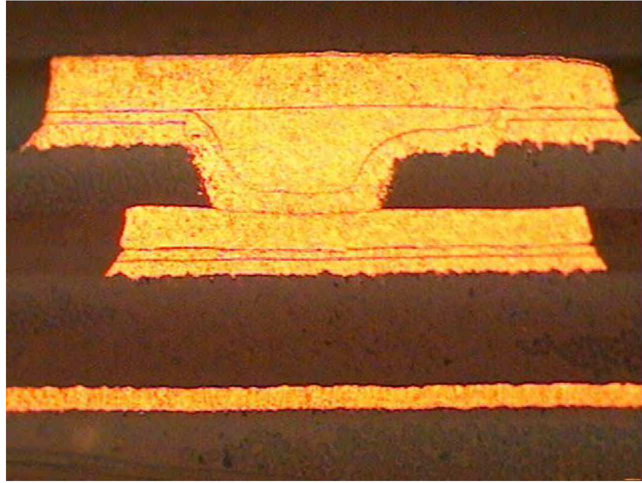
  Vias can be conformal plated or Cu fill plated

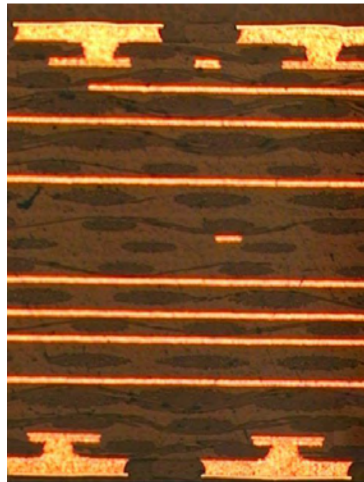


Conformal plated laser via

Fill plated laser via

Technology Contribution: Micro VIA





Technology Contribution: Micro VIA

Item	Comment
Signal Integrity	Small, stubless via
Routability	Freed up space on layer below via
Reliability (SnPb)	Proven – Passed L1 & L2 qualifications
Reliability (Pb-free)	Proven - Passed L1 & L2 qualifications
Supply Base	Large
Process Complexity	Minimal – laser drilling and microvia plating…pretty common technology for most suppliers
Cost	~5-15% (Conformal plated) ~15-40% (Cu fill plated)
Hidden Cons	Design tools not 100% optimized

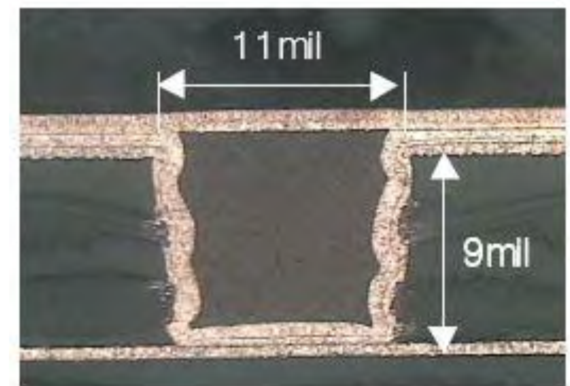
Technology Contribution: Skip VIA

- **What is it?**

  Laser vias which connect layer 1 to 3 and n to (n-2)

  Normally combined with the use of microvias

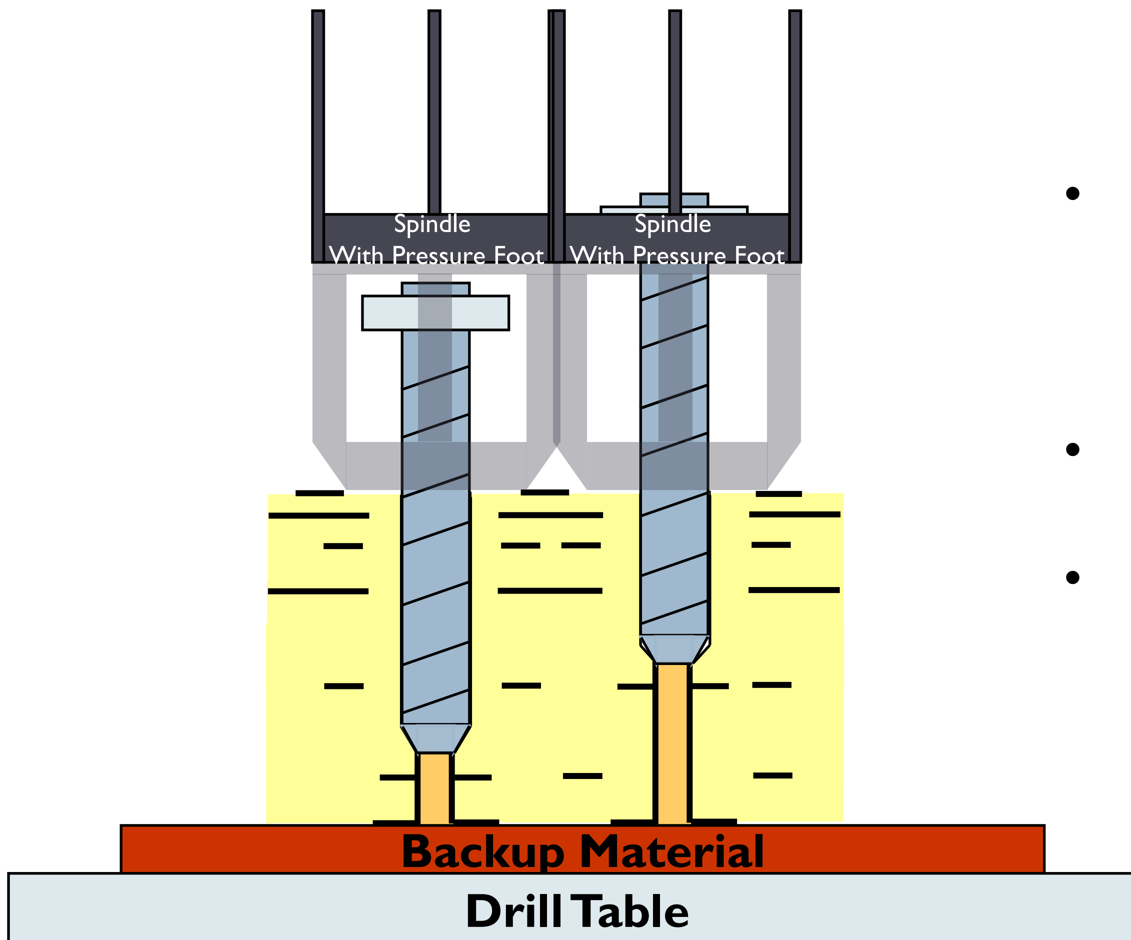
  Vias can be conformal plated or epoxy filled and plated over (SKIPPO)



Technology Contribution: Skip VIA

Item	Comment
Signal Integrity	Stubless via connection for high speed signals
Routability	Freed up space on layer below via
Reliability (SnPb)	Passed
Reliability (Pb-free)	Passed
Supply Base	Limited
Process Complexity	Moderate – complex laser drilling process
Cost	~15-20% (Conformal plated) ~30-40% (SKIPPO) Adds processing days! Up to 3 days.
Hidden Cons	Prone to laminate cracking below via

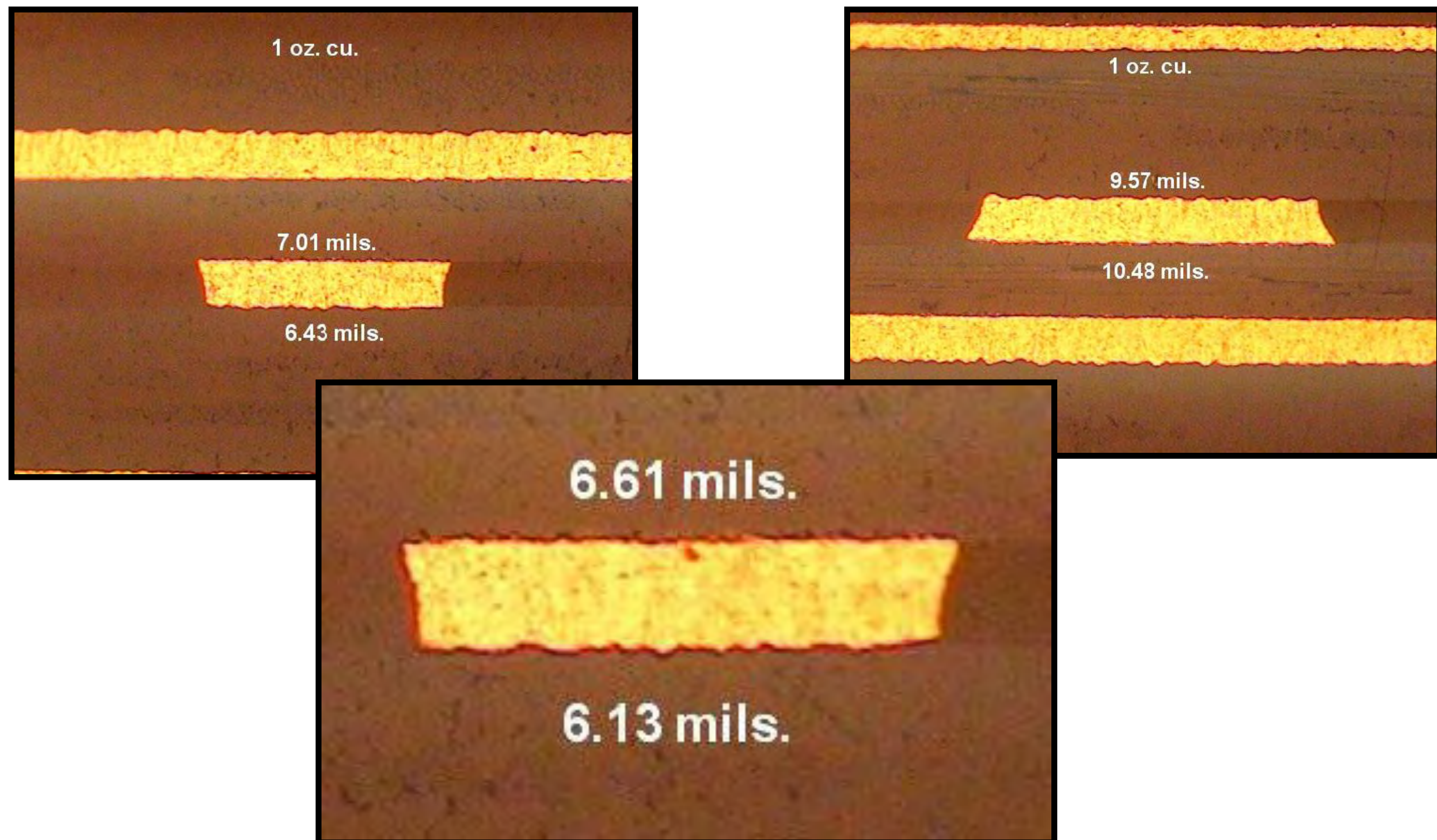
Technology Contribution: Back Drilling



- ***Back Drilling is a well defined process with < 4% cost impact on fr4 and < 8% on MEG6.***
- Stop depth tolerance can be as low as +/- 5 mils but often is in the range of +/- 10 mils.
- Removes a significant portion of the stub.
- Don't be afraid to deploy this fabrication technology. Seldom used in 2000, this technique is used today in almost all high speed designs.

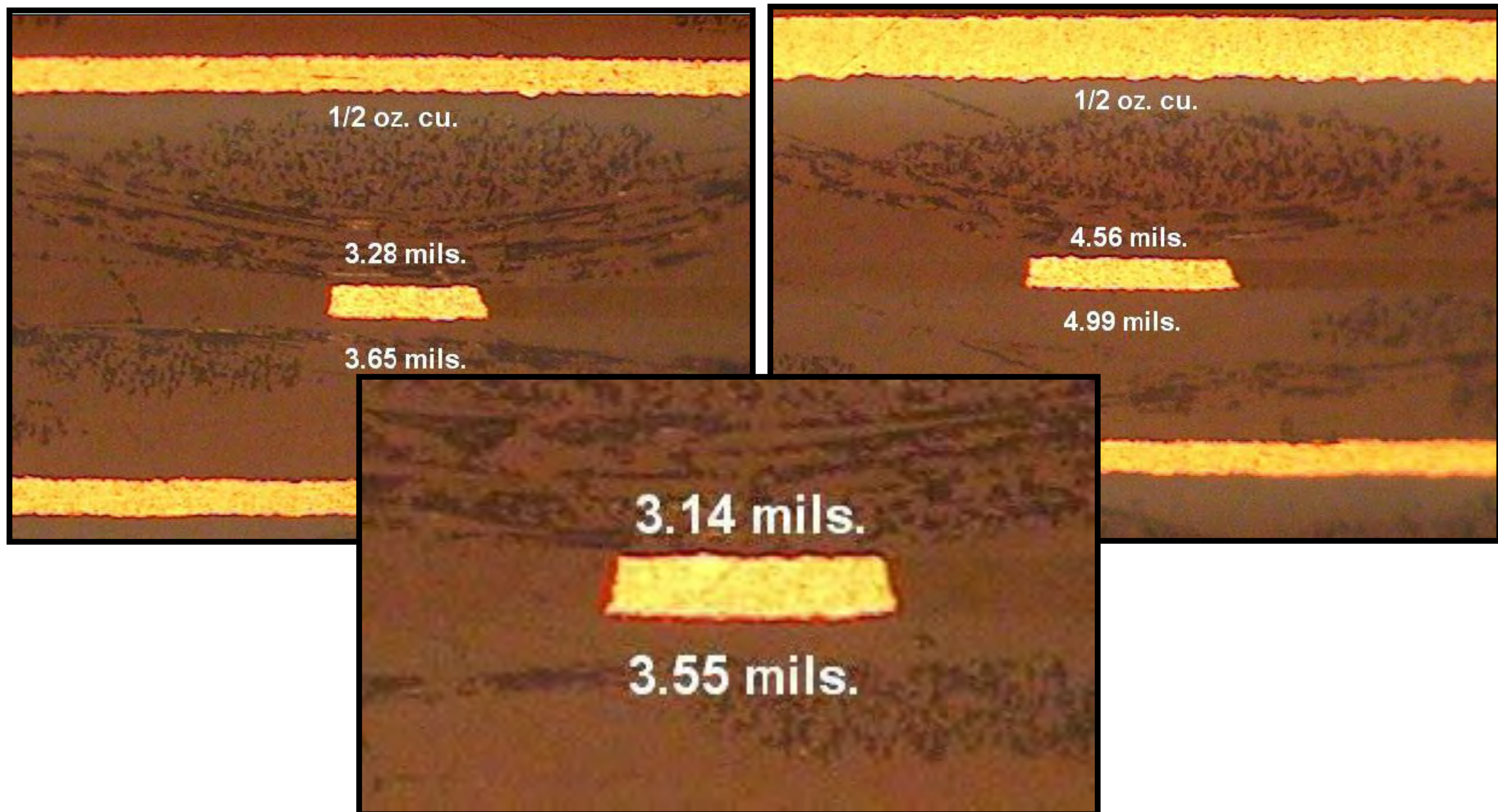
1 oz Copper Signal Characteristics Internal Layers

- 1 oz copper trapezoid shape ~ .50 -.90 mils total width reduction at top
- Copper thickness ~ 1.10-1.25 mils typically



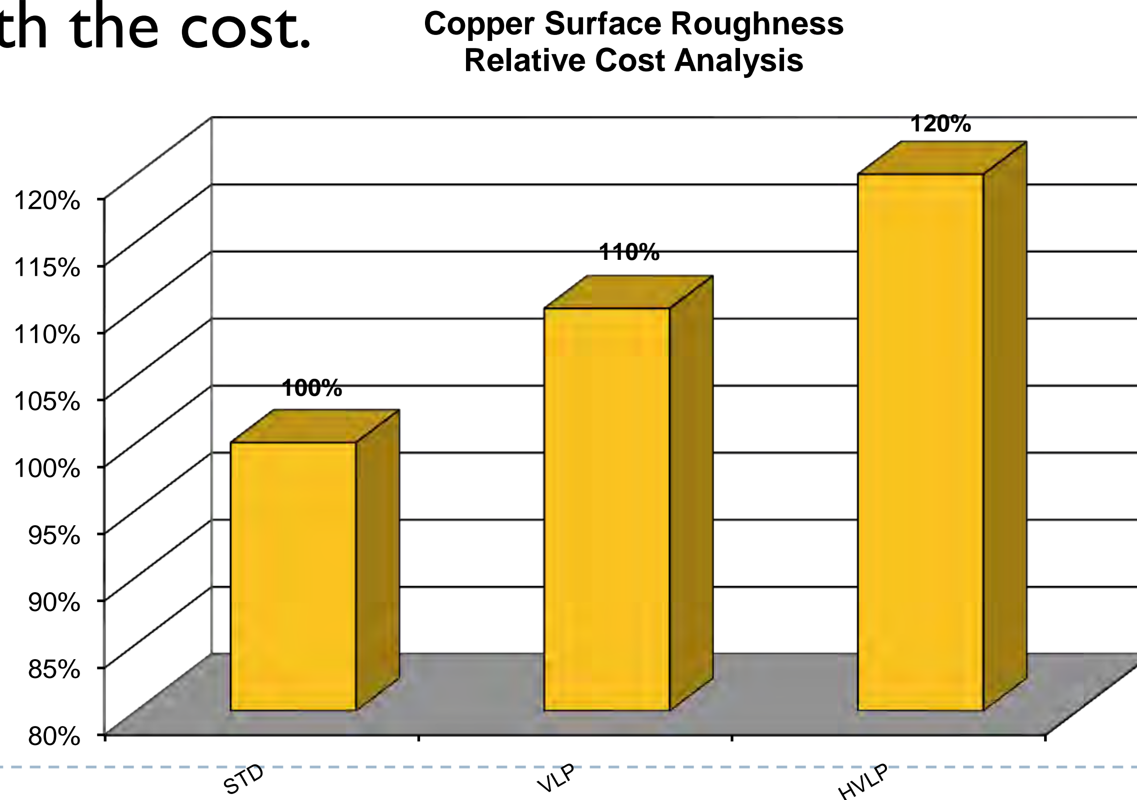
½ oz Copper Signal Characteristics Internal Layers

- ½ oz copper trapezoid shape ~ .40 -.50 mils total width reduction at top
- Copper thickness ~ .55 -.65 mils typically



Technology Contribution: Copper Surface Roughness

- Much work has been done here.
- Impact at 10Gbps is not worth the added costs.
- Impact at 25Gbps shows improvement but still might not be worth the cost.



Technology Contribution: Two Channel Definitions Provide Choices

Board Design Challenges

1. Total BOM costs are design specific
   - BOM cost tolerance is program related
   - FCS BOM cost is followed by engineering cost reductions
2. Technology choices can add risks and cost adders
3. Circuit boards are a fundamental component of BOM cost.

Improved FR-4

- ✓ Lower Cost of circuit board implementation and lower signal integrity performance.
- ✓ Limited design constraints .
- ✓ Minimal use of board technology components
- ✓ Usually a board yield in the high 90% range and buildable by a wide range of supplier base.

Super Improved FR-4

- ✓ Higher circuit board costs but much higher signal integrity performance.
- ✓ Can have harsh design constraints to support the performance targets.
- ✓ Utilizes a full set of board technology components in the fabrication.
- ✓ Usually a board yield in the high 60% range and limited in supplier base.

Summary

- We support and recommend the development of two PHYs targeting two classes of channels, based on two different classes of materials… Add an objective!

Thank You!