PKG RL Ad-Hoc Summary

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PKG Return Loss Ad-Hoc Group

- 5 Calls were conducted.
- 16 individuals Participated in the call(s): Thanks for the effort, participating and sharing thoughts and knowledge: Ali Ghiasi; Beth Kochuparambil; Richard Mellitz; Ckumar; Magesh; Mike Dudek; Mike Li; Rick Lutz; Rick Rabinovich; Adee Ran; Vasu; Piers; Galen Fromm; Charles Moore; Adam Healey; Matt Brown
- The group's main recommendations:
  - Supply updated return loss limits and equations for COM code and TP0a.
  - Add a Rx side package insertion loss model that follows Mellitz_3bj_01_0112.
- The suggested return loss and insertion loss model for COM based on Mellitz_3bj_01_0112 (and its correlated measured) provides a passing COM result with target interconnect.

Supporters

- Rabinovich, Rick - Alcatel-Lucent
- Adee Ran – Intel
- Galen Fromm - Cray Inc
- Charles Moore – Avago Technologies
- Beth Kochuparambil – Cisco Systems

Ad-Hoc Agreed Target

- Come up with a coherent proposal for return-loss for TP0, TP0a and TP2 as well as the symmetrical points on the Rx side.
- Come up with an agreed PKG return loss that will correspond to TP0a measured return loss and to TP2 return loss.
  - Update return loss definition according to agreement @:
    - TP0 (COM code)
    - KR4/KP4 TP0a (measured through fixture)
    - CR4 TP2
    - & the symmetrical @ the Rx side.

Submitted Comments

- #38: The return loss equation for TP0/TP5 as described in Eq: 93a-3,4,5 and table 93a-2 is not coherent (consistent) with the measured return loss at TP0a/TP5a as described in equations 93-2, 93-7, 94-5, 94-15 as well as with cable return loss as described at equations: 92-1 and 92-5.
- The Conclusions Also Address:
  - Comment 129 and 132 : Transmitter return loss mask
  - Comment 132: Receiver return loss mask

as submitted by Ali Ghiasi.

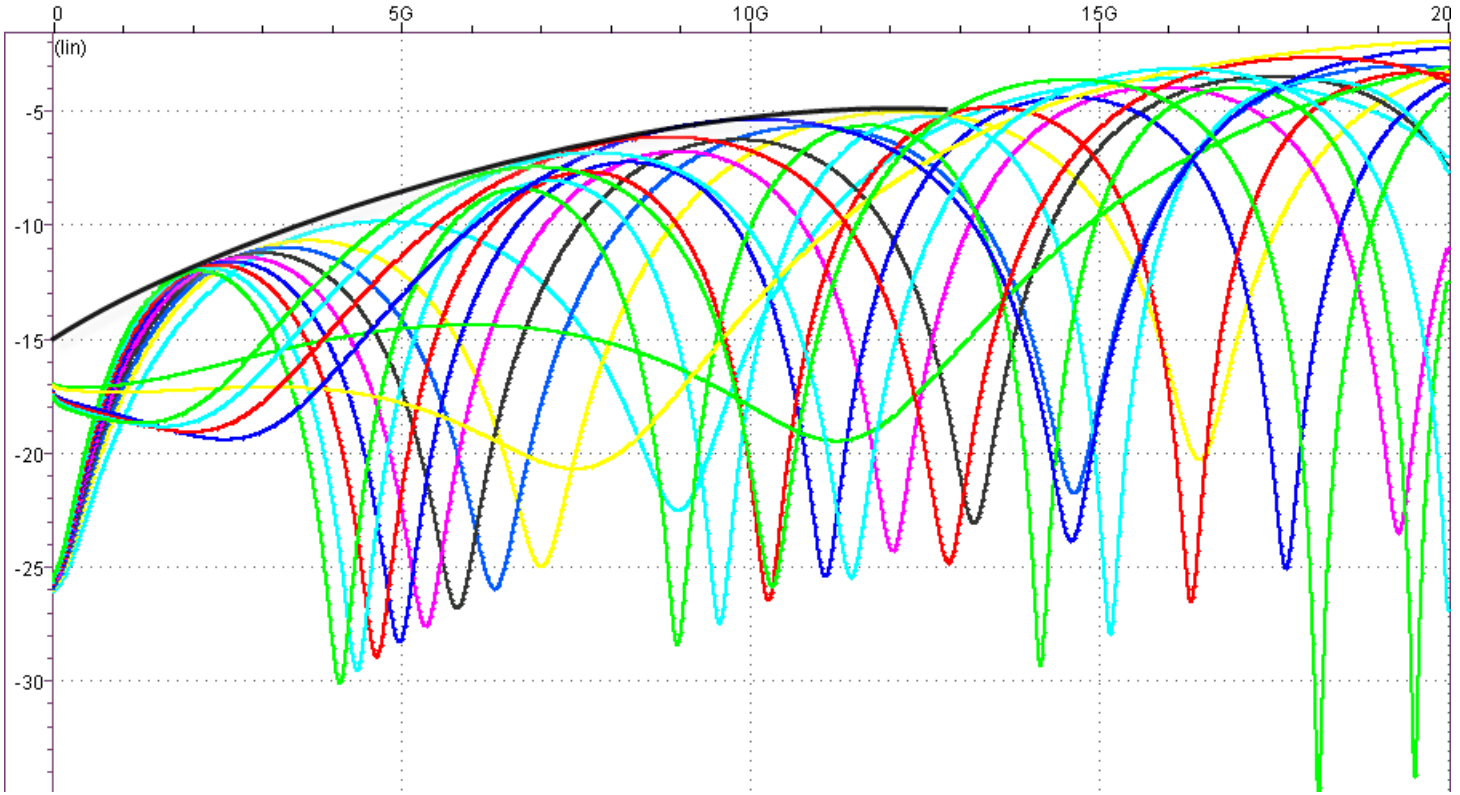
  - Comment #29: Return loss equation by Charles Moore
  - Comment #104: Return loss frequency range by Piers Dawe

Inputs, Collected Thoughts and Recommendations

- PKG TP0/TP5 return loss of ~12dB @ 2GHz and ~5dB @12.89GHz is considered a realistic achievable curve (slightly tightening the limit relative to formerly presented according to inputs from the group). – Thanks for sharing your thoughts!
- It is required to allow Tx DC impedance to go to lower values in order not to limit driver implementation.
  - The TP0a definition of measured RL should have a value lower than 15dB near DC to cover possible driver implementations.
  - A 30Ω odd mode(60Ω differential) driver was examined in COM and resulted in similar to better com value ➔ it is not the worst COM case Tx.
  - A low impedance Tx is therefore not needed to be included in the COM code.

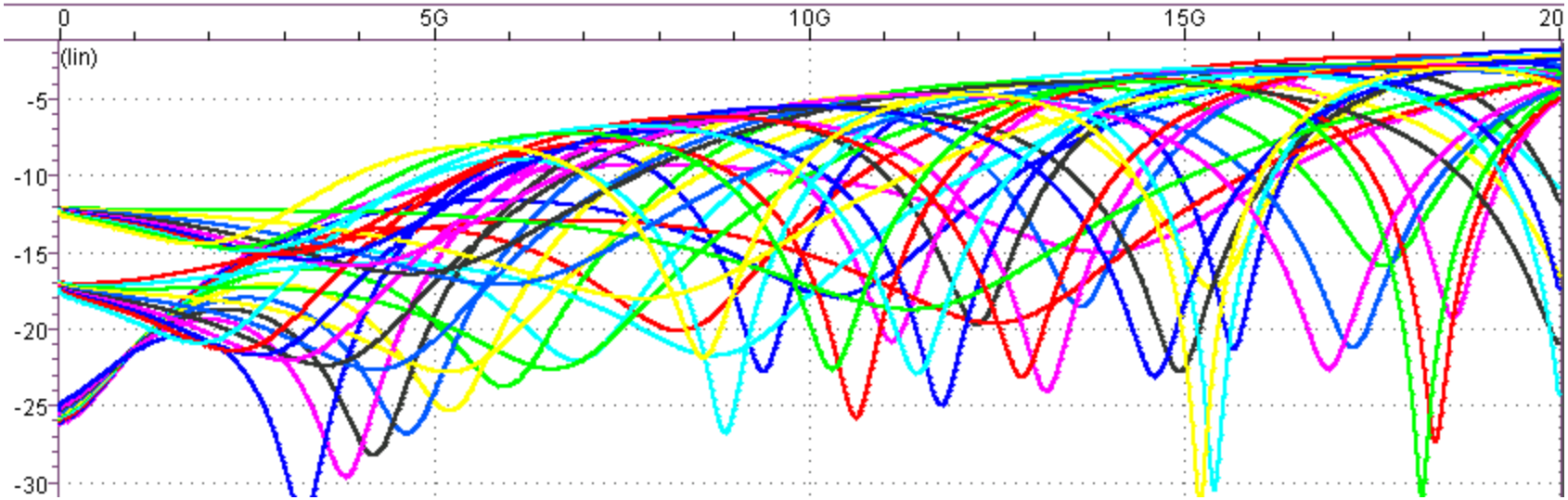
Simulated Return Losses

- PKG length swapping + two die impedances that meets the ad-hoc group consensus.
- A corresponding package was ran in COM – Encouraging results!



PKG Alteration Runs

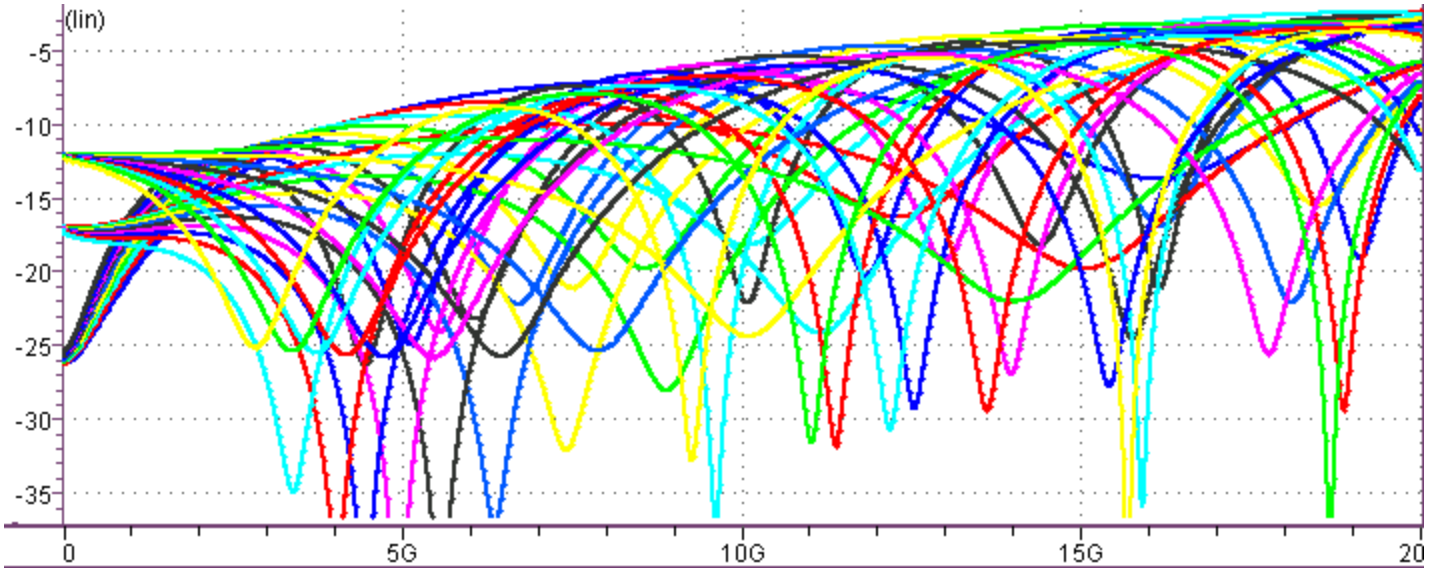
- 100ohm PKG



- Main issues are:
  - high frequency Ret-loss of ~4.3
  - Insertion loss of 3.3dB

PKG Alteration Runs

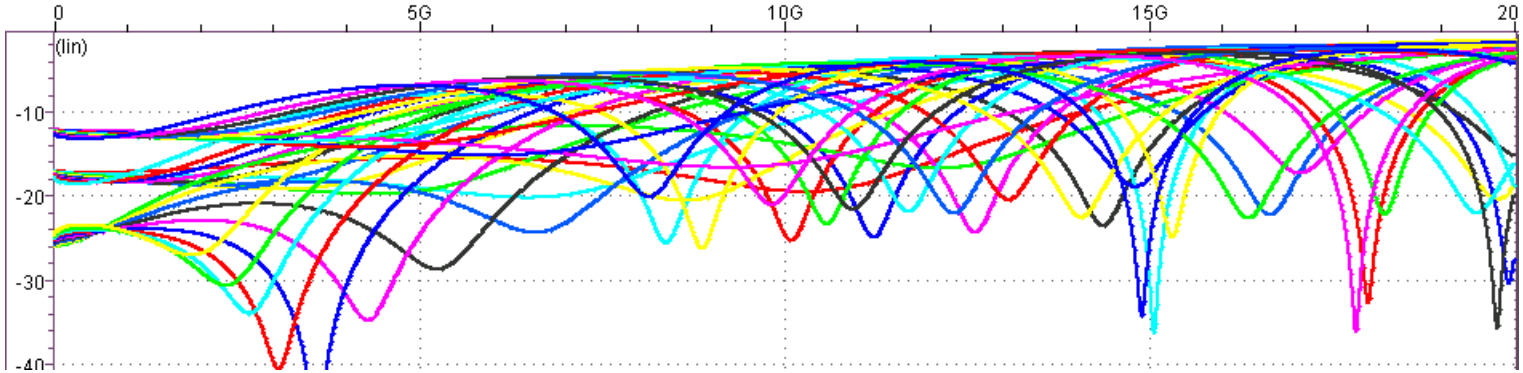
- 83ohm PKG



- Main issues are:
  - high frequency Ret-loss of ~4.6
  - Low freq (2GHz) ret-loss of 11.5dB
  - Insertion loss of ~3.1dB

PKG Alteration Runs

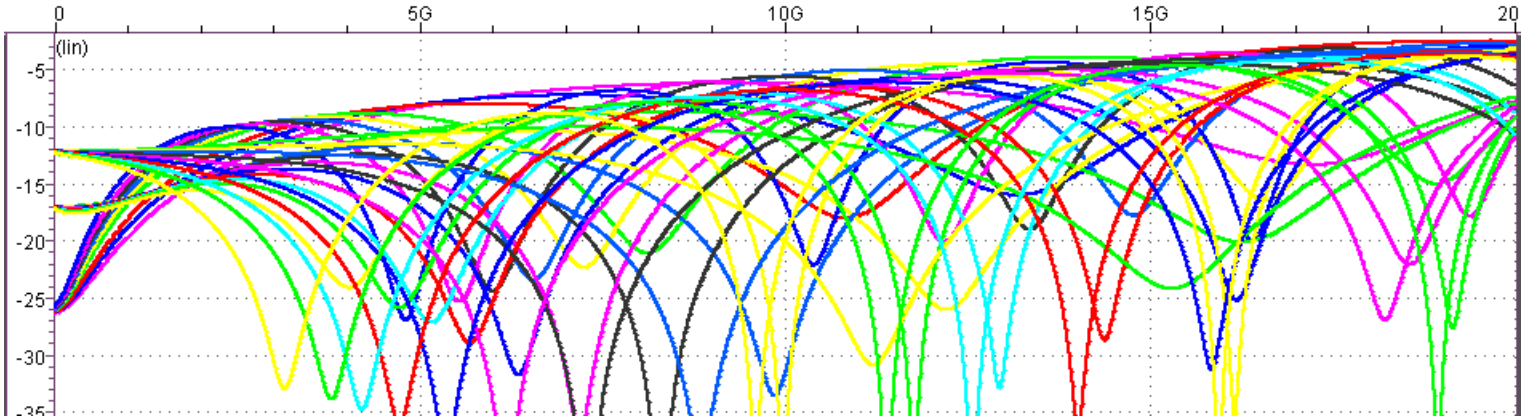
- 115ohm PKG



- Main issues are:
  - high frequency Ret-loss of ~4
  - Low freq (2GHz) ret-loss of 10.9dB
  - Insertion loss of ~3.7dB

PKG Alteration Runs

- 75ohm PKG (for the case of tuning PKG impedance lower for lower Tx impedances.)



- Main issues are:
  - high frequency Ret-loss of ~4.7
  - Low freq (2GHz) ret-loss of ~10.5dB
  - Insertion loss of ~3dB

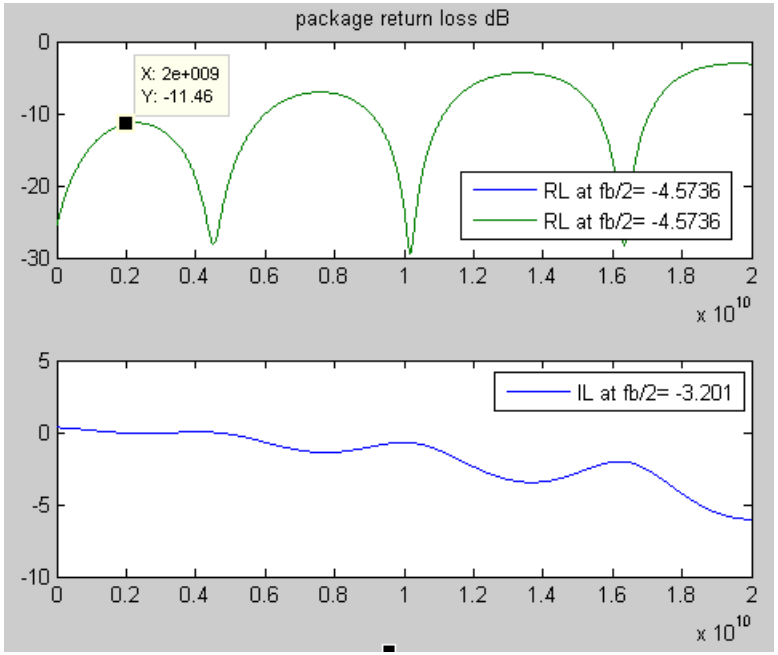
PKG Alteration Runs Conclusion

- The worst case is the 115ohm PKG impedance resulting in extra PKG insertion loss, 4dB return loss @ 13GHz as well as 10.9dB return loss @ 2GHz.
- Recommend tuning the COM return loss to ~11.5dB @2GHz and ~4.5dB @ 13GHz and PKG insertion loss to ~3.2dB.
- The above recommendation is not the worst case observed…

Recommended PKG Model Related Values

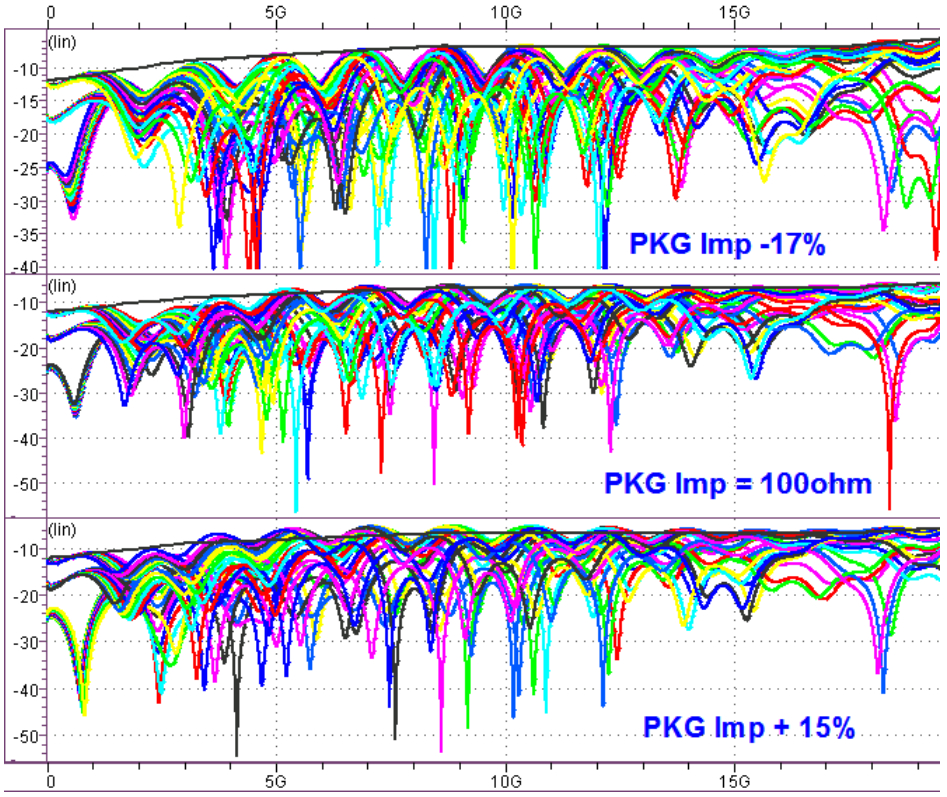
- The values below are recommended for use in correlation to the methodology described in in Mellitz_3bj_01_0113:

a_il_0	-4.453e-4 + 4.467e-05i	
a_il_1	-1.049e-08 - 4.568e-08i	
a_il_2	-6.409e-13-3.914e-11i	
a_il_3	-1.669e-23 + 3.134e-23i	
a_rl_0	-6.473 - 1.51i	
a_rl_1	6.451e-05 + 3.351e-07i	
a_rl_2	-2.712e-10 - 4.903e-11i	
a_rl_3	2.167e-21 + 2.765e-22i	
C_diepad	250	ff
R_diepad	55	
C_pkg_board	180	ff
Pkg_len	12	mm



Measured RL @ TP0a with PKG Impedance Tolerance

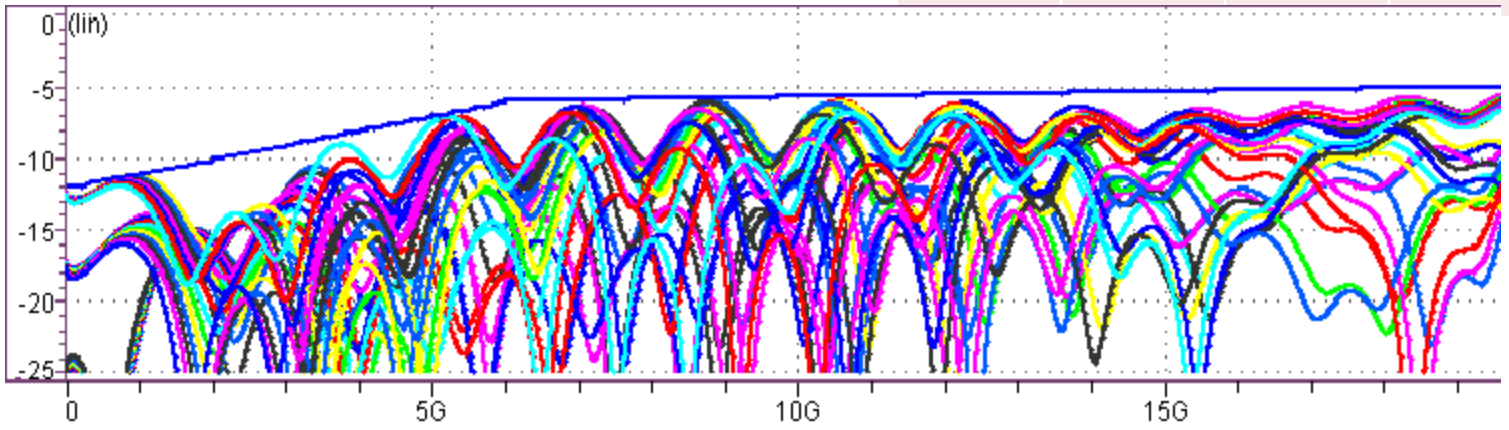
- The measured return loss (TP0a/TP5a) was simulated taking into account PKG manufacturing tolerance and worst case fixture.
- A suggested remedy on next slide



TP0a Suggested RL Limit

- Suggest that the measured return loss @TP0a/TP5a be higher than:
  RL@TP>aF+b (F in GHz) between F1 and F2
- Excluding the combination of high impedance PKGs + low impedance driver one can get: (Still allowing a low impedance driver)

F1	F2	a	b
0.05	6	-1	12.05
6	19	-0.075	6.45



The correlation between RL @ TP0a/TP5a and RL @ TP2/3

- TP0 to TP2 (TP5 to TP3) IL :

$$Insertion\_loss(f) \le \begin{cases} 0.084 + 0.599\sqrt{f} + 0.631f & 0.01 \le f < 14 \\ -20.07 + 2.23f & 14 \le f \le 19 \end{cases} \quad \text{(dB)}$$

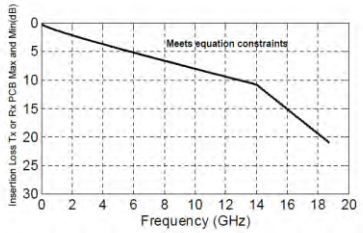


Figure 92–6—Maximum insertion loss TP0 to TP2 or TP3 to TP5

- The problem with the suggested return loss is the ability to achieve TP2 return loss with low loss TP0 to TP2 interconnect.
- Should we limit the min TP0-TP5 IL / change TP2 RL?
  - Not at this point, because:
    - one would <u>not</u> expect to achieve lower Insertion loss TP0-TP2 relative to the mated test fixture.
    - HCB is expected to provide as transparent as possible connection.
    - TP2 may change according to later simulation.
    - COM cable runs results with margin.

The mated test fixtures insertion loss limits are illustrated in Figure 92–17

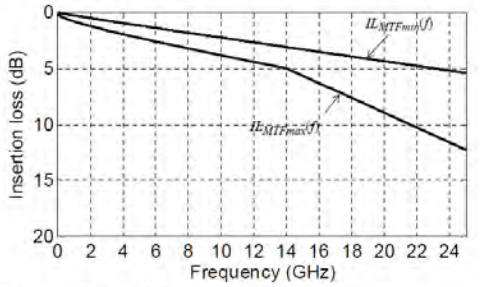
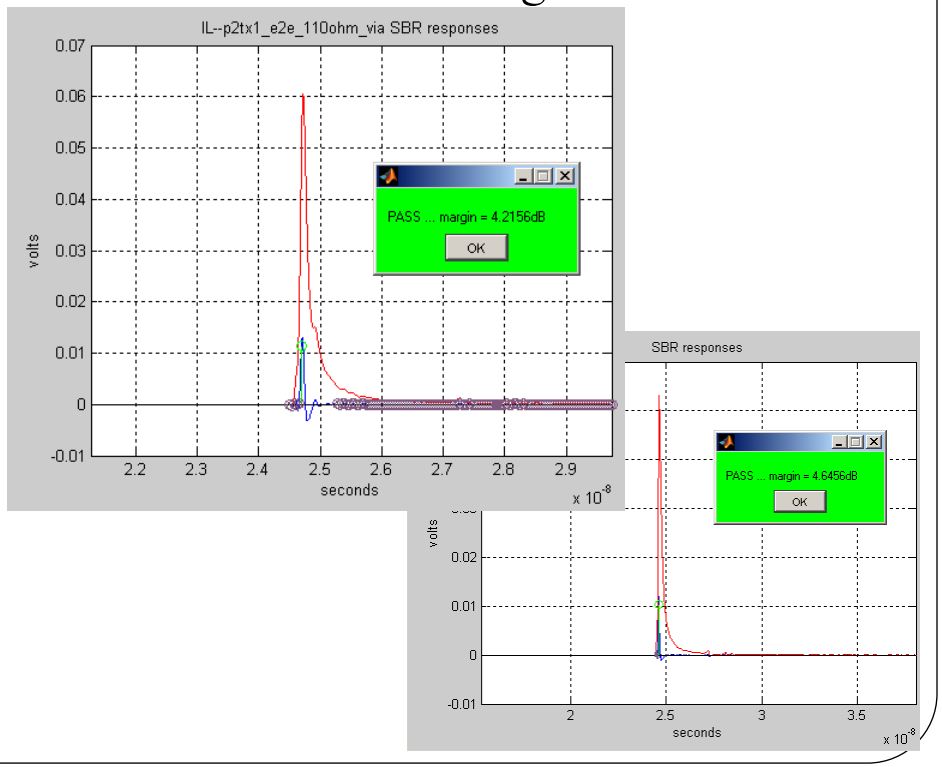


Figure 92–17—Mated test fixtures Insertion loss

Molex Cable End-to-End COM results

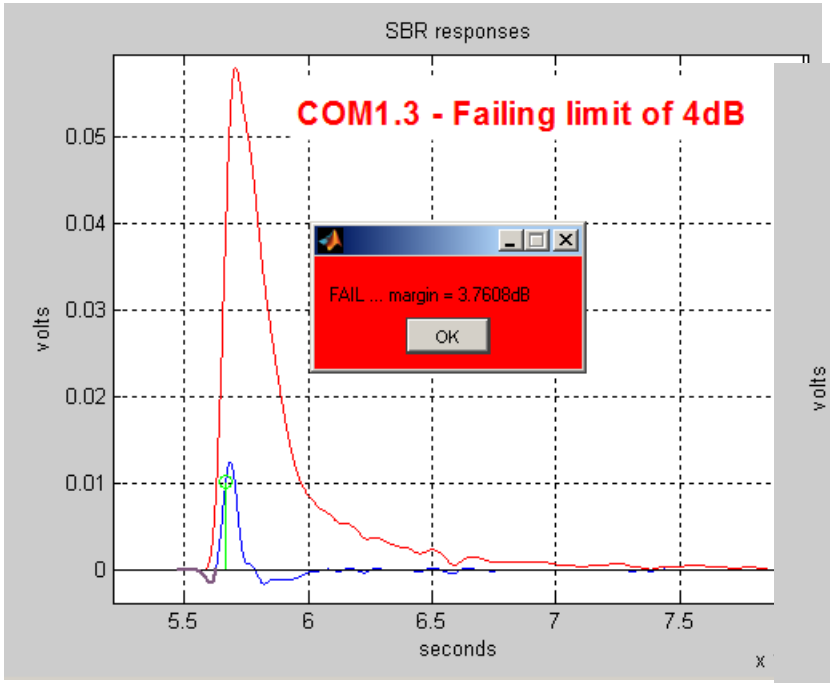
- Molex Cable_a was ran in COM with suggested RL and resulted in passing COM margin.
- (110Ω host board model + two vias)*2 were added to the bare cable model to get it close to 35dB @ 12.89GHz.
  - The via models represent the device break-out vias + cable connection vias. The trace was taken to the manufacturing tolerance of +10%.
- Model lacked host board Xtalk, but resulted in high margin after board concatenation.
- COM1.3 resulted in 0.64dB margin. ➔ Current suggestion margin = 1.21dB.

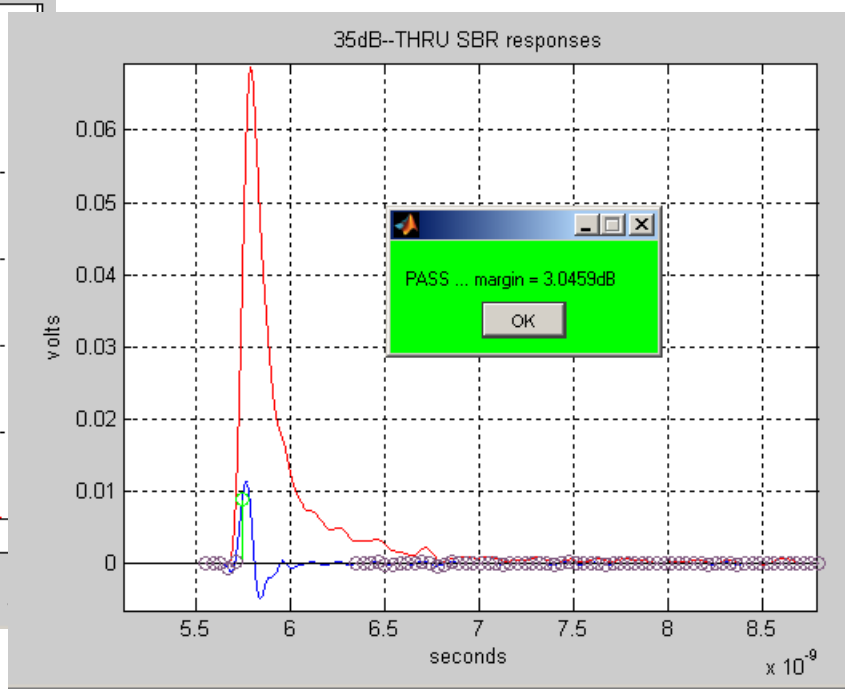


IBM35dB channel COM results

- Checking the 35dB IBM channel: COM result=~3. 05dB with Suggested alphas (~11.5dB @2GHz ; 4.6dB @ 13GHz) – Marginal results.

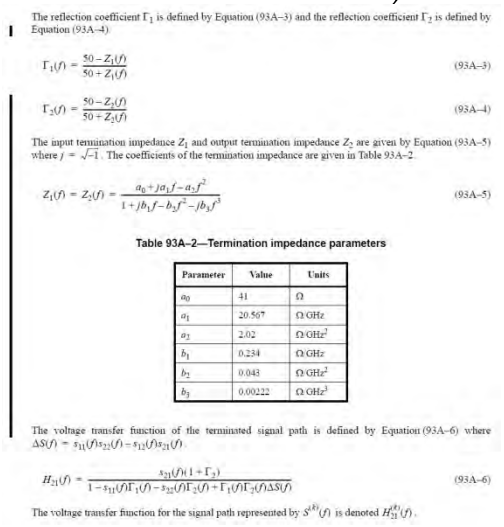
Note: The interconnect does not meet the return loss specification.





Comments Suggested Resolution

- Replace equations 93-2, 93-7, 94-5, 94-15 with the described @ slide #15. Limit the frequency range for clause 94 to 10GHz.
- Remove equations 93A-3 through 93A-6.
- Remove table 93A-2
- Add a PKG model section with the phases:
  - Estimate differential s-parameters for a small segment of uniform lossy transmission line (Mellitz_3bj_01_0113 slide#5)
  - Create s parameters for pad and ball (Mellitz_3bj_01_0113 slide#7)
  - Combining Parameters to create PKG and End2End model (Mellitz_3bj_01_0113 slides#8-9)
  - Add a table of PKG model values per slide 13 (in current presentation).



The reflection coefficient Γ_1 is defined by Equation (93A–3) and the reflection coefficient Γ_2 is defined by Equation (93A–4).

$$\Gamma_1(f) = \frac{50 - Z_1(f)}{50 + Z_1(f)} \quad (93A\text{–}3)$$

$$\Gamma_2(f) = \frac{50 - Z_2(f)}{50 + Z_2(f)} \quad (93A\text{–}4)$$

The input termination impedance Z_1 and output termination impedance Z_2 are given by Equation (93A–5) where $j = \sqrt{-1}$. The coefficients of the termination impedance are given in Table 93A–2.

$$Z_1(f) = Z_2(f) = \frac{a_0 + ja_1 f - a_2 f^2}{1 + jb_1 f - b_2 f^2 - jb_3 f^3} \quad (93A\text{–}5)$$

Table 93A–2—Termination impedance parameters

Parameter	Value	Units
a_0	41	Ω
a_1	20.567	Ω/GHz
a_2	2.02	Ω/GHz^2
b_1	0.234	Ω/GHz
b_2	0.043	Ω/GHz^2
b_3	0.00222	Ω/GHz^3

The voltage transfer function of the terminated signal path is defined by Equation (93A–6) where $\Delta S(f) = s_{11}(f)s_{22}(f) - s_{12}(f)s_{21}(f)$.

$$H_{21}(f) = \frac{s_{21}(f)(1 + \Gamma_2)}{1 - s_{11}(f)\Gamma_1(f) - s_{22}(f)\Gamma_2(f) + \Gamma_1(f)\Gamma_2(f)\Delta S(f)} \quad (93A\text{–}6)$$

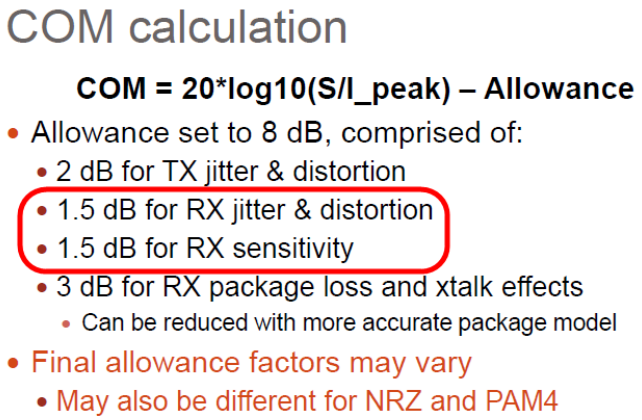
The voltage transfer function for the signal path represented by $S^{(k)}(f)$ is denoted $H_{21}^{(k)}(f)$.

Recommended Comment Resolution – Cont.

- Since a Rx side PKG insertion loss model is added, change the required COM Value from 4 to 3 (derived from Ran01_0712.pdf – page 8) at:
- CC1 @ 93.11.4.4 Channel characteristics
- 93.9.1 - Channel operating margin
- 94.4.1 - Channel operating margin
- CC1 @ 94.6.4.5 Channel characteristics

Notes:

- Different interconnects have different COM values according to different PKG RL/IL parameters with Pk-Pk variance of ~0.5dB.
- PKG crosstalk was not budgeted.



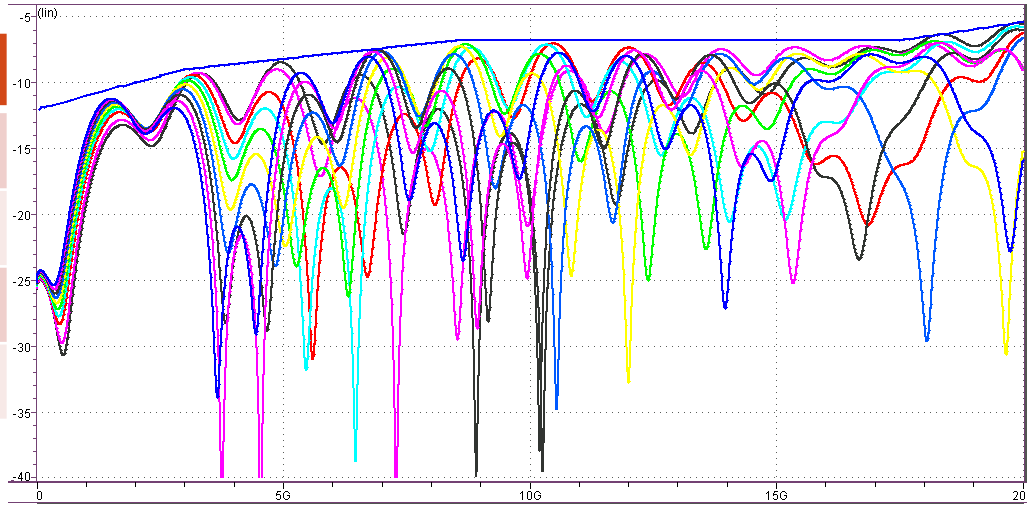
Thank you

Backup slides / Ad-hoc meetings slides

Suggested Measured RL @ TP0a/TP5a - Forth ad-hoc meeting – absolete

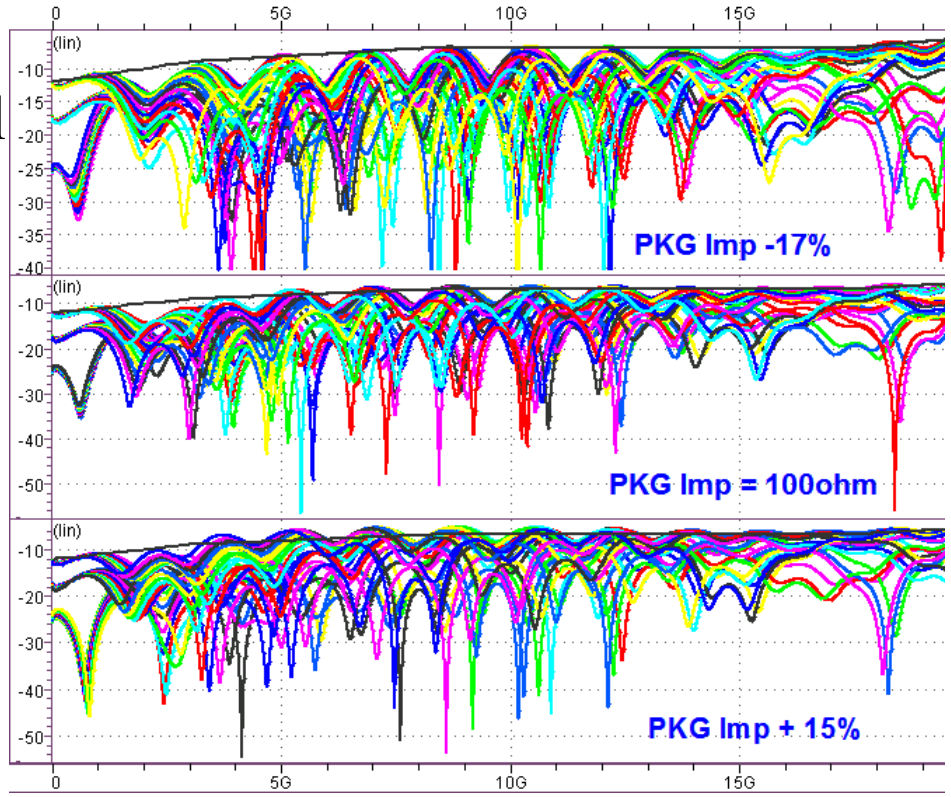
- Suggestion was changed according to PKG manufacturing tolerance runs…
- Simulated the PKG return loss as measured through the worst case allowed test fixture (inc. SMA launch)
- Suggest that the measured return loss @TP0a/TP5a be higher than:
  RL@TP>aF+b (F in GHz) between F1 and F2

F1	F2	a	b
0.05	3	-1.025	12.05
3	8.5	-0.4	10.2
8.5	17.5	0	6.8
17.5	19	-0.56	16.6



Measured RL @ TP0a with PKG Impedance Tolerance

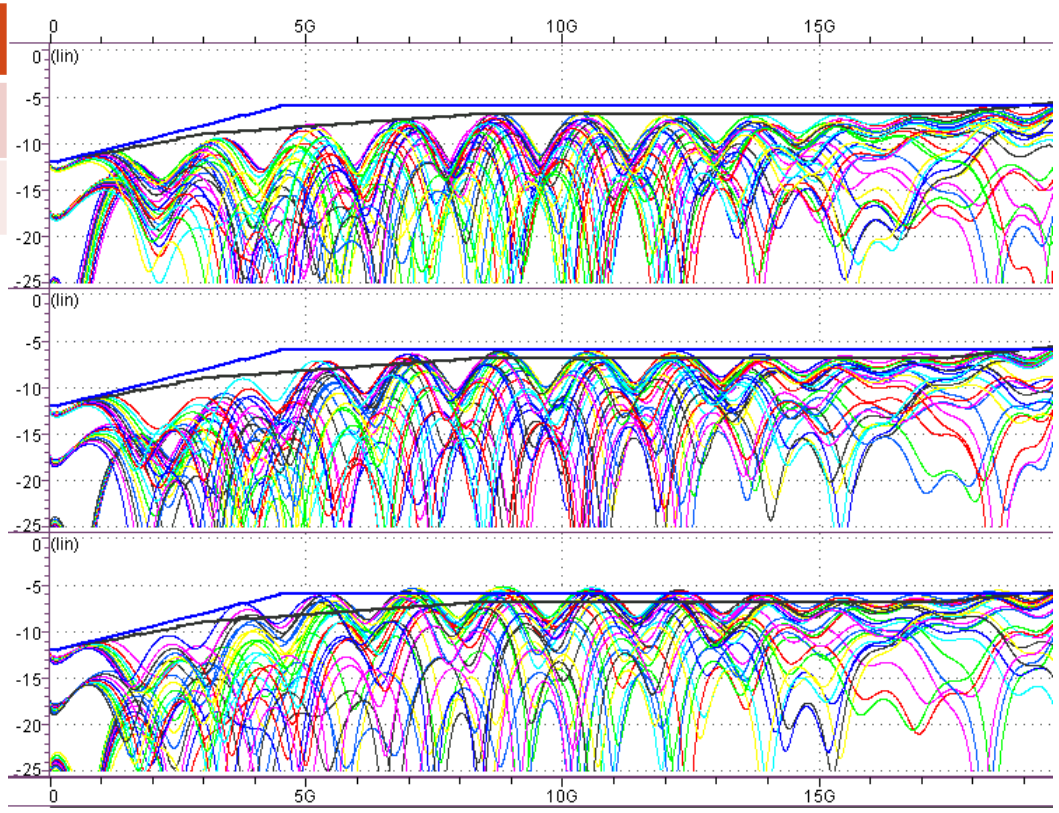
- The measured return loss (TP0a/TP5a) was simulated taking into account PKG manufacturing tolerance and worst case fixture.
- Specific frequency violations can be observed mainly with 60Ω driver and high impedance fixture.
- Possible solutions on next slide.



Possible TP0a solution for tolerance cases

- One possible solution is to use the following limit which meets most of the manufacturing tolerance cases.

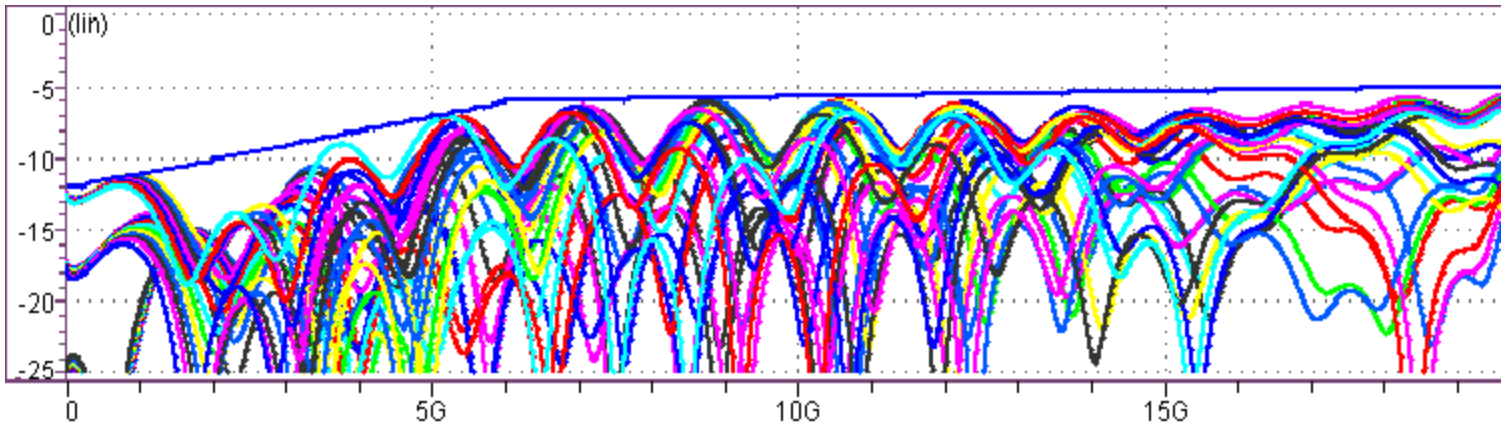
F1	F2	a	b
0.05	4.5	-1.35	12.06
4.5	19	0	6



TP0a Suggested RL Limit

- Suggest that the measured return loss @TP0a/TP5a be higher than:
  RL@TP>aF+b (F in GHz) between F1 and F2
- Excluding the combination of high impedance PKGs + low impedance driver one can get: (Still allowing a low impedance driver)

F1	F2	a	b
0.05	6	-1	12.05
6	19	-0.075	6.45



First meeting A.Rs

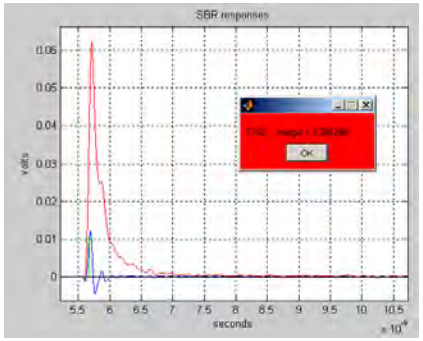
- Supply package trace simulation results without taking into account discontinuities.
- Remove non relevant (short) traces from PKG simulation and define “achievable” RL (see slide 8)
- Run IEEE target interconnects and come-up with the desired TP0/TP5 RL (using COM)
- Further PKG simulations from other people would be welcome.

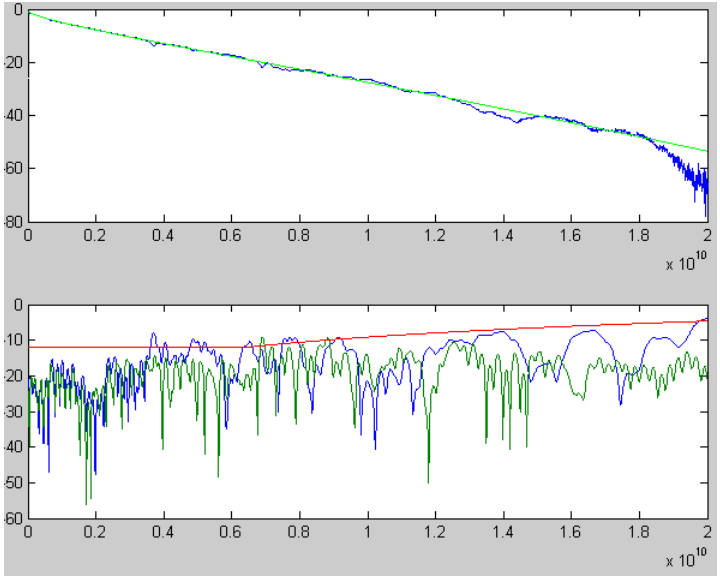
Required Return Loss to Meet 35dB Target

- The ~35dB IBM interconnect was used as a reference target interconnect.
- To represent the PKG return loss a trace representation was used (+ Parasitic capacitance of the Die and Ball) instead of the RL mathematical equation from the spec.
  The representation was swept with:
  - 45Ω/55Ω driver (odd mode)
  - Different package length.
  - PKG impedance was changed to achieve desired COM
  - Various combinations of driver/receiver to find worst combination.

The IBM ~35dB Interconnect

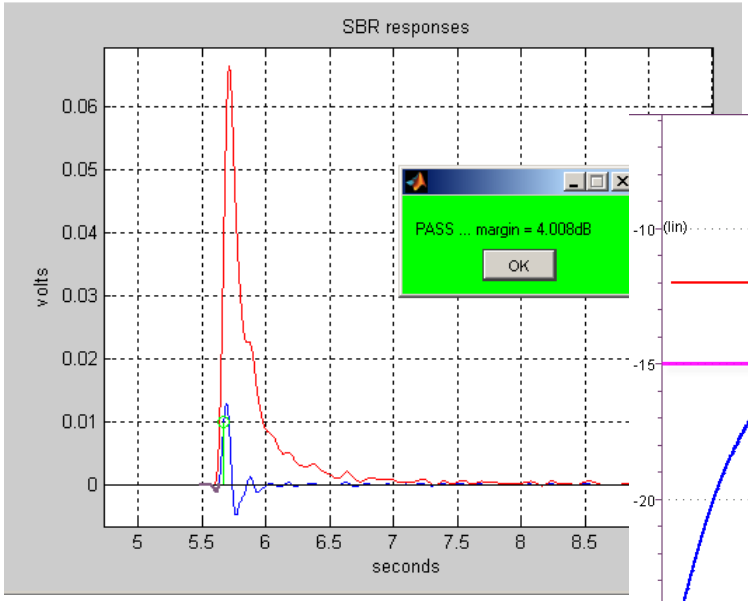
- Loss @ Fb/2 = 35.7dB
- Return loss (slightly) violates the informative definition (by fixing the RL an extra ~0.2dB of COM margin can be gained).
- ~3dB of COM result when combined with an "achievable" package return loss (according to the described at the former ad-hoc meeting)
  (one example below):

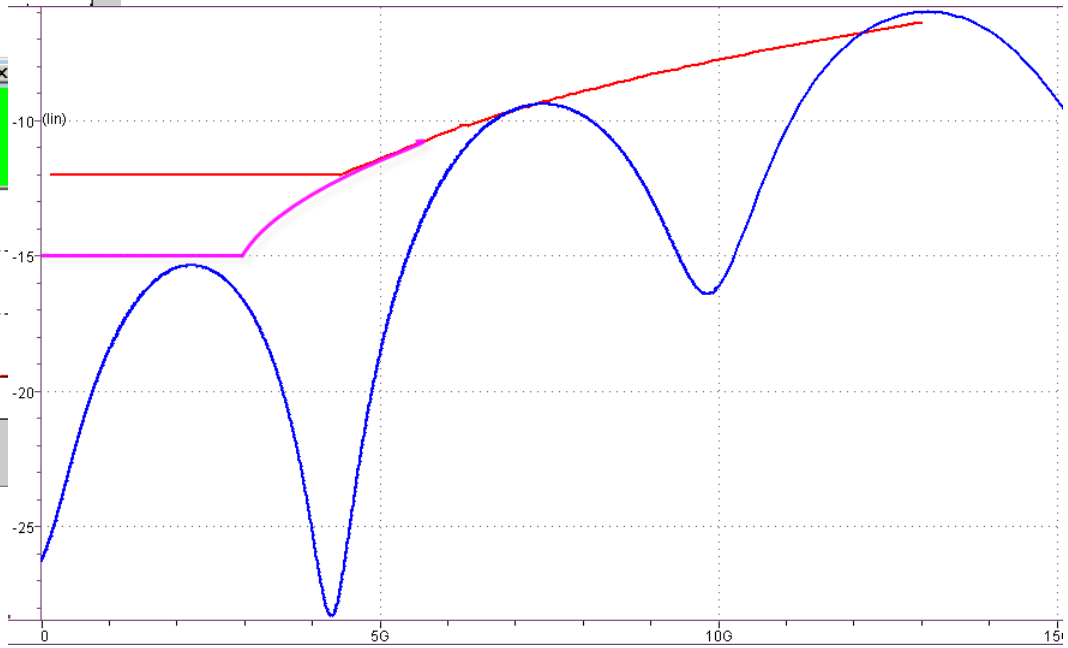




The Required PKG RL to Meet the Target

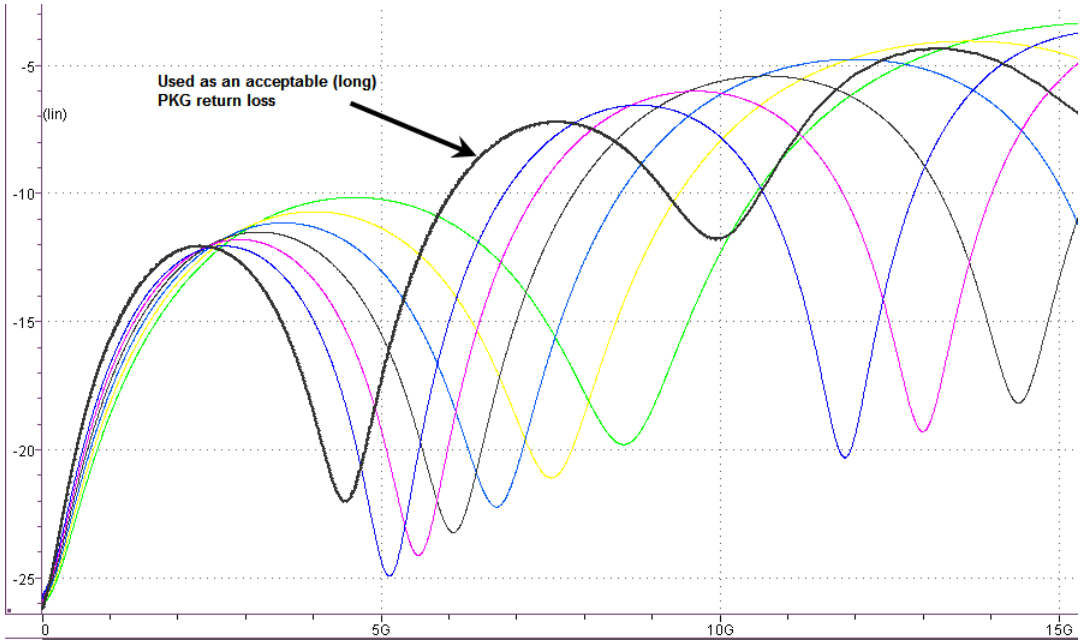
- With assumed combination of interconnect parameters the following is an example of the most strict PKG return loss needed to meet the target.





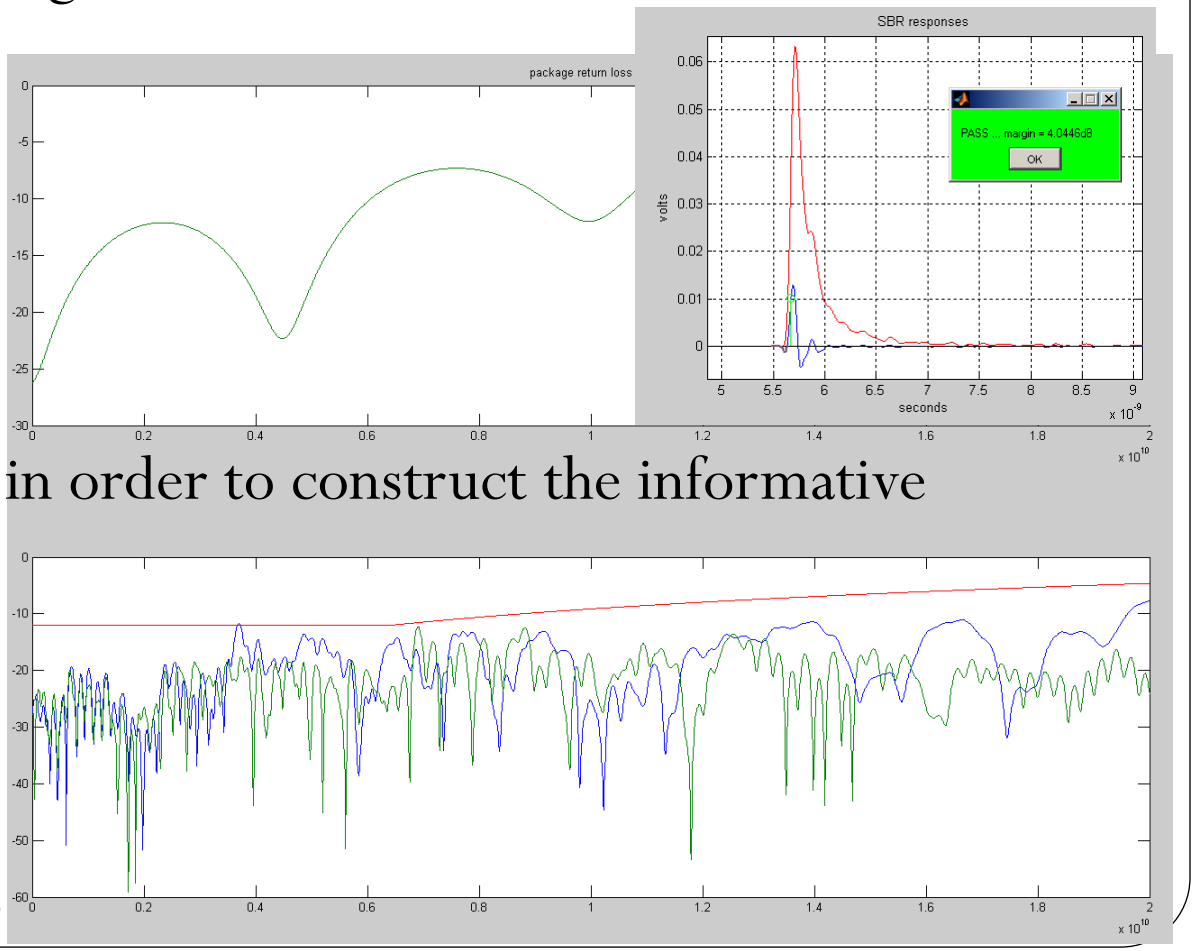
The Required Interconnect RL to Meet the Target
(given an "acceptable" PKG return loss)

- Assuming a specific PKG RL, examine the required interconnect RL in order to meet the target interconnect loss.
- An acceptable PKG RL was created (based on assumptions presented during the last meeting – assumptions can be seen on slide #21).



The Required Interconnect RL to Meet the Target (given an "acceptable" PKG return loss) – Cont.

- The Interconnect return loss required to meet the target, assuming the following PKG return loss was:
- Further tuning may be done to better distribute the RL between Sdd11 and Sdd22.
  - Will be important in order to construct the informative interconnect RL.
- Actual required RL Is closer to ~20dB @ low Frequencies



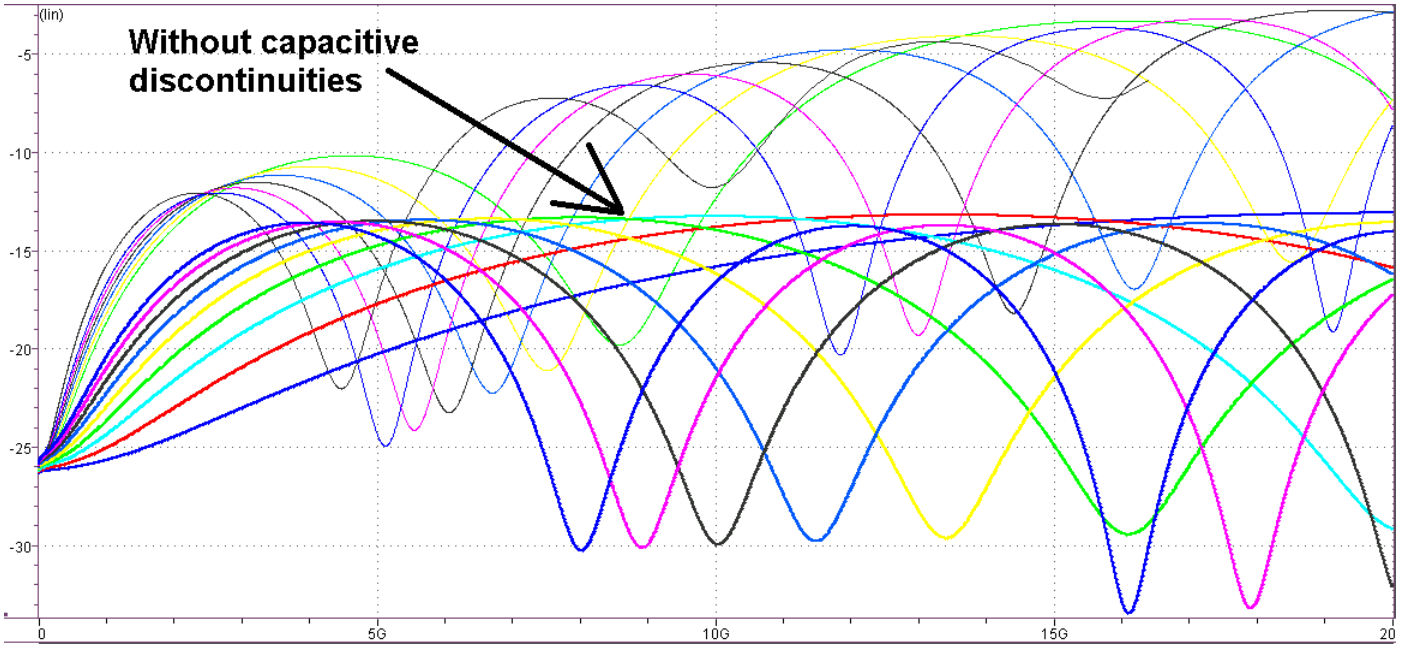
Status Summary

- It was demonstrated/claimed that:
  - OIF/CEI PKG return loss + OIF/CEI interconnect return loss are not enough to meet the target interconnect.
  - OIF PKG return loss does not line-up with simulated PKG RL (former meeting – slide #21).

Suggested Way to Proceed

- Agree on PKG parameters (die capacitance, trace manufacturing tolerance, etc.) and derive an acceptable PKG return loss based on the agreed parameters variance.
- Find the interconnect insertion loss border-line that can be achieved with current interconnect RL. Suggest a tighter interconnect RL for higher loss interconnects.
- Construct a PKG RL equation for COM that follows the same COM result as different PKG length.
- Define the measured PKG RL after fixture based on worst case fixture definition.
- Define the measured RL @ TP2 / TP3 for 100GBase-CR4 based on PKG RL + TP0 to TP2 interconnect.
- Use updated RL in COM to run TP0-TP5 (cable + board) interconnects and make sure to meet target.

PKG interconnect excluding Die and ball discontinuities



D1.3 RL Status description

- 802.3bj uses a time domain statistical based simulation methodology for qualifying channels. A channel actual transfer can only be examined when taking into account the effect of multiple reflections between the channel and the connecting items' return loss.
- 802.3bj incorporates two different package return loss definitions.
  - Return loss physical equation @TP0/TP5 to be used within the COM code in the context of channel qualification.
  - A measured return loss @TP0a/TP5a, as measured through a test fixture for KR4/KP4 Tx/Rx characteristics qualification.
    The test fixture definition has a return loss better then 15dB up to 13GHz…

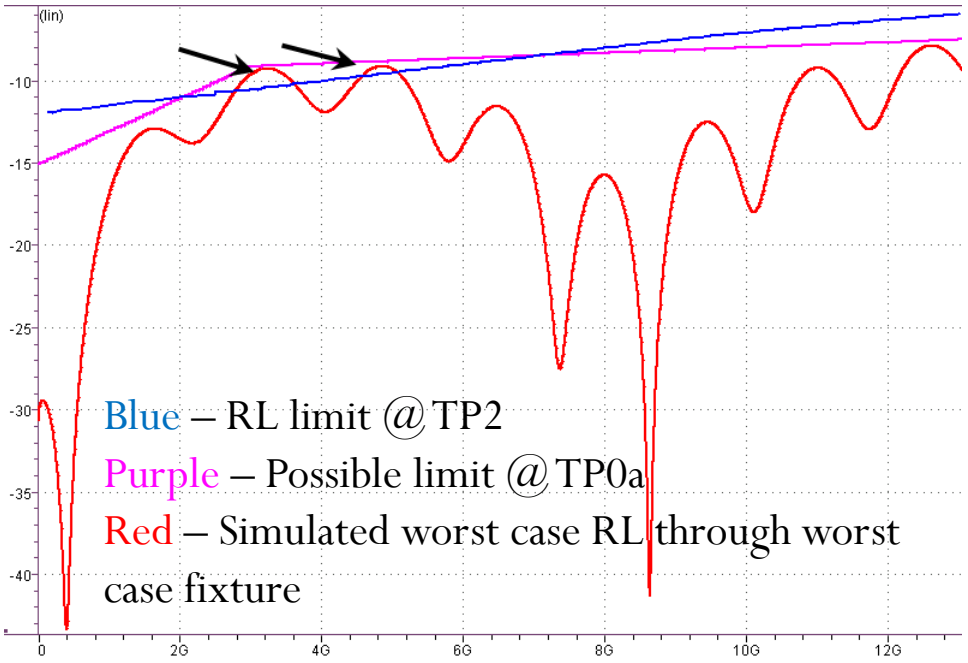
D1.3 RL Status description – Cont.

- A separate definition has been accepted for TP2 for the case of a cable connection.
- Numerous presentations took into account die parasitic capacitance of 0.25pF.
- A sweep run was performed on PKG return loss taking into account: (such a sweep is shown on slide 10)
  - 0.25pF die parasitic capacitance
  - Ball discontinuity
  - PKG trace characteristic impedance manufacturing tolerance
  - Die DC impedance tolerance

  ➔ PKG TP0/TP5 (for COM) and TP0a/TP5a (measured taking into account worst case fixture) limits were proposed.

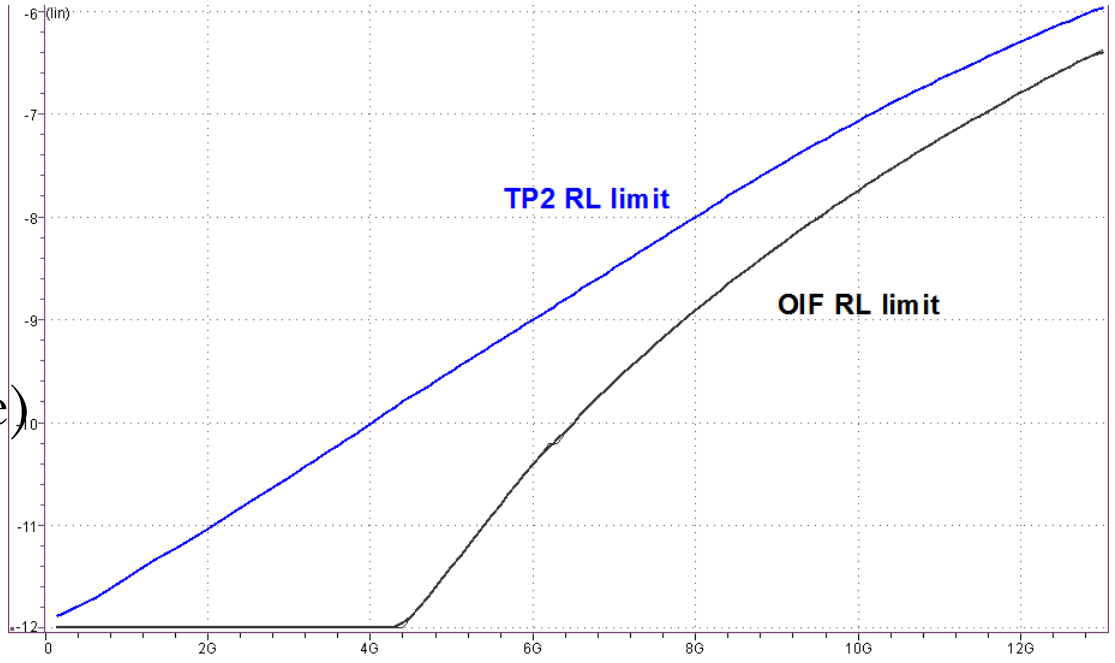
D1.3 RL Main Issues

- Comparing TP0a measured return loss to TP2 measured return loss raise a question whether TP2 return loss can be achieved with TP0 specified return loss.
- TP0a suggested return loss (taking into account worst case fixture) indicates it may be problematic to get TP2 return loss with short traces.
- Violation seen between 2GHz – 6GHz



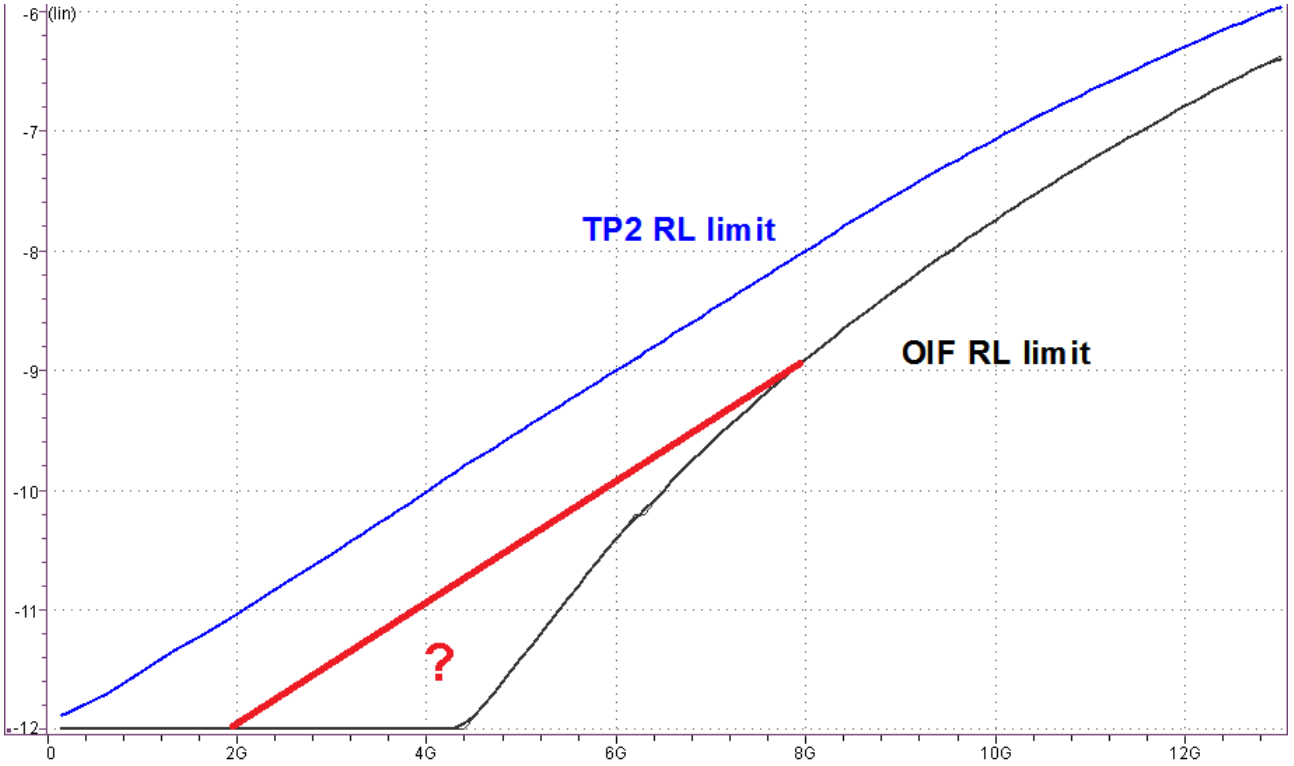
OIF-25G-LR Return Loss Limit (@TP0)

- The OIF defined a return loss limit that main companies claimed “doable”.
- The margin taken between the OIF RL limit and TP2 limit is inconsistent through frequency + does not correlate to TP0 ➔ TP2 interconnect loss.
- TP0 RL @ 13GHz <TP2 RL ?
- Unexplained margin between ~2GHz and 8GHz (next slide)



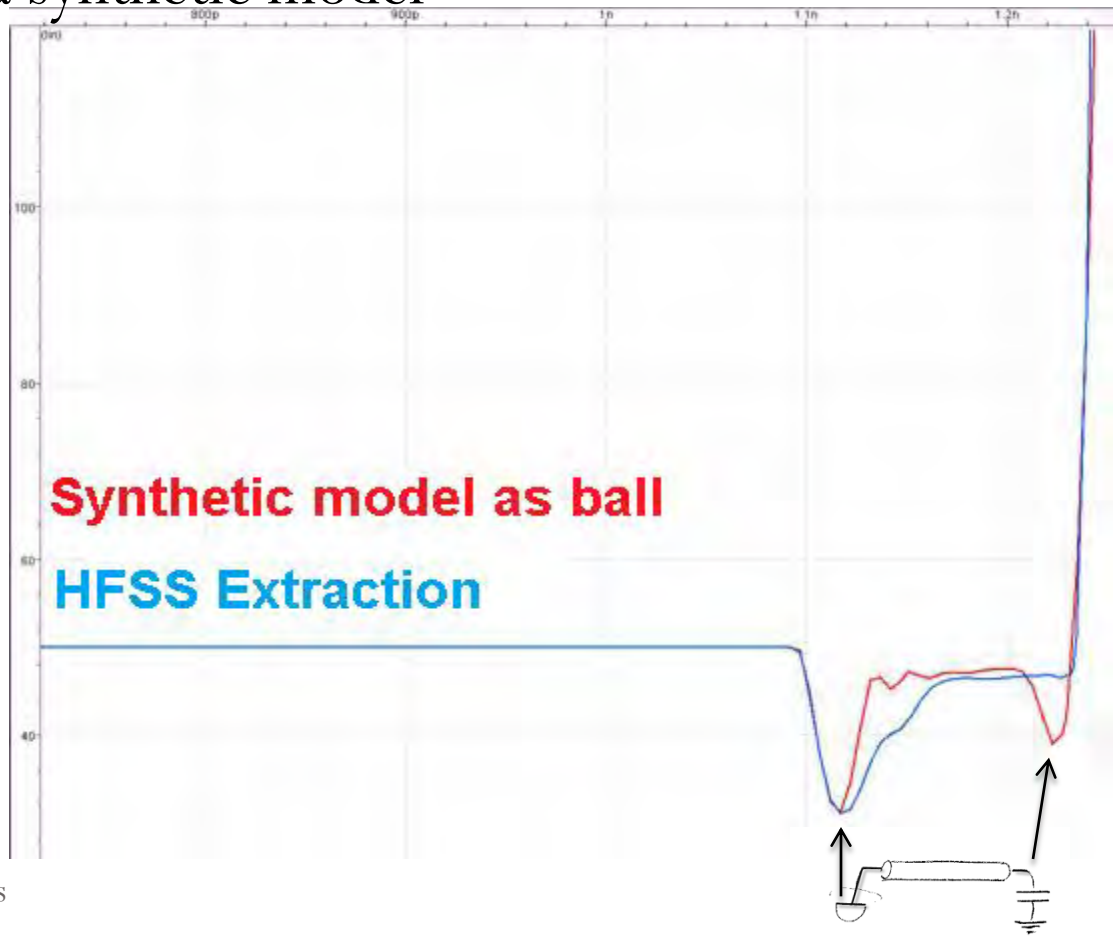
The OIF-25G-LR Return Loss vs. TP2

- Unexplained margin between ~2GHz and ~8GHz



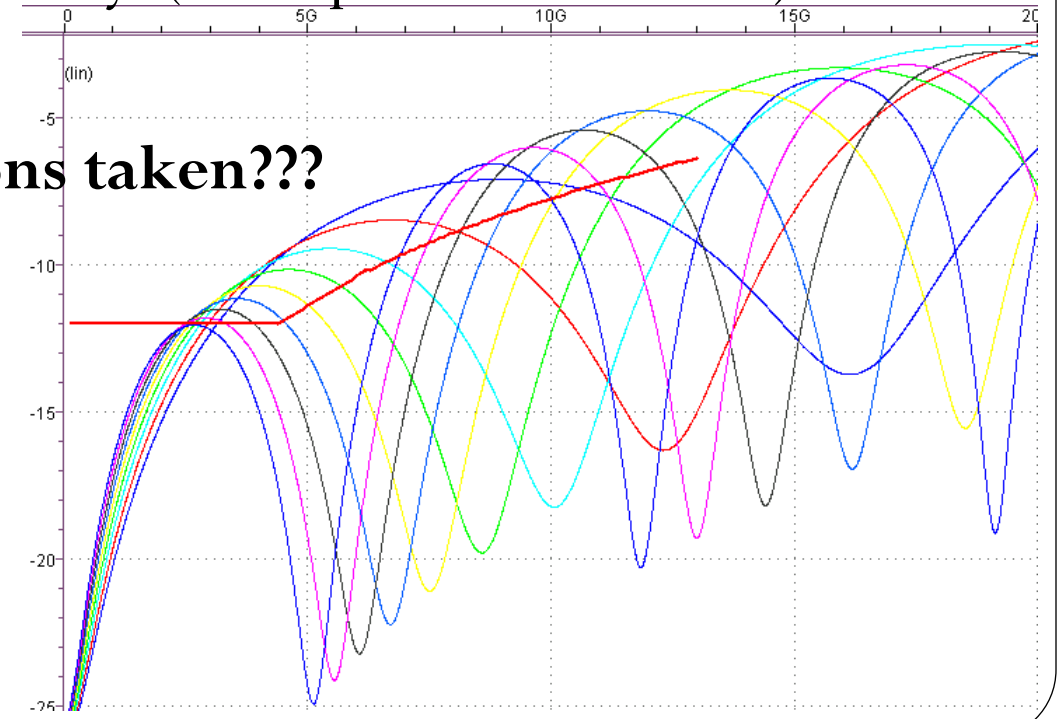
Correlated Synthetic Model as Ball

- A correlation was performed between HFSS extracted ball discontinuity and a synthetic model



Simulating PKG Return Loss

- PKG trace impedance = 82.5Ω
- Die impedance tolerance (10%)
- Die parasitic capacitance = 0.25pF
- Optimized ball discontinuity. (1mm pitch – 4 in a row)



- **Different assumptions taken???**
- **Is the analysis too simplified?**

Ways to Proceed (straw poll)

1. Agree on a PKG return loss based on OIF (with required agreed corrections) – Agree it is achievable without using patents. – Can someone provide a simulation / measurement / proof ?
2. Base PKG return loss on a tightened PKG parameters simulation + tight routing constrains to allow TP2 current limit.
3. Base PKG return loss on current PKG parameters (according to slide 10) simulation, define routing constrain to TP2 and update TP2 limit accordingly (high frequency can be tighter, low frequency should be looser).

Suggested Measured RL @ TP0a/TP5a

- Suggest that the measured return loss @TP0a/TP5a be higher than:
  RL@TP>aF+b (F in GHz) between F1 and F2

F1	F2	a	b
0.05	2	-1.025	12.05
2	9	-0.42	10.83
9	15	-0.07	7.65
15	20	-0.46	13.6