Clause 94 comment resolution
Addresses various comments

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Introduction

- This presentation provides proposed responses to a grab bag of comments.

Comments 90 and 228
100GBASE-KP4 overhead registers

Comments 90 and 228

Cl **94** *SC* **94.2.12** *P* **249** *L* **39** # 90

Healey, Adam LSI Corporation

Comment Type **T** *Comment Status* **X**

In Table 94-4, the register numbers for PMA overhead control and status are TBD.

SuggestedRemedy

Define the register numbers.

Proposed Response *Response Status* **O**

Cl **94** *SC* **94.2.12** *P* **249** *L* **39** # 228

Brown, Matthew Applied Micro

Comment Type **T** *Comment Status* **X**

MDIO status and control register fields have been specified for the PMA overhead, but specific MDIO register address is TBD. The registers are annotated in Table 94-4 and Table 94-5.

SuggestedRemedy

Provide specific MDIO register address for each of the PMA OH register fields.

Proposed Response *Response Status* **O**

Introduction

- 100GBASE-KP4 PMA overhead behavior specified in 94.2.2.3 (transmit) and 94.2.4.1 (receive).
- Mapping of variables to MDIO registers specified in Table 94-4 (status) and Table 94-5 (control).
  - Register addresses are specified as TBD.
- No specification in Clause 45.
- Need 6 new MDIO registers for overhead control and status fields.
- As suggested by Hugh Barrass, use register addresses 1.162 to 1.166.

PMA overhead control register mapping (table 94-4)

- Update table 94-4 as shown below. Changes are indicated by underline.

MDIO control variable	PMA/PMD register name	Register/bit numbers	PMA control variable
PMA transmit overhead pattern	PMA overhead control 1	1.162.7:0	TX_OH_pattern
PMA transmit overhead sequence 0	PMA overhead control 1	1.162.13:8	TX_OH_sequence_0
PMA transmit overhead sequence 1	PMA overhead control 2	1.163.4:0	TX_OH_sequence_1
PMA transmit overhead sequence 2	PMA overhead control 2	1.163.9:5	TX_OH_sequence_2
PMA transmit overhead sequence 3	PMA overhead control 2	1.163.14:10	TX_OH_sequence_3
PMA receive overhead pattern	PMA overhead control 3	1.164.7:0	RX_OH_pattern

PMA overhead status registers mapping (table 94-5)

- Update table 94-5 as shown below. Changes are indicated by underline.

MDIO control variable	PMA/PMD register name	Register/bit numbers	PMA control variable
PMA receive overhead sequence 0	PMA overhead status 1	1.165.5:0	RX_OH_sequence_0
PMA receive overhead sequence 1	PMA overhead status 1	1.165.11:6	RX_OH_sequence_1
PMA receive overhead sequence 2	PMA overhead status 2	1.166.5:0	RX_OH_sequence_2
PMA receive overhead sequence 3	PMA overhead status 2	1.166.11:6	RX_OH_sequence_3

Add new section 45.2.1.89a

45.2.1.89a PMA overhead control 1, 2, and 3 registers (1.162, 1.163, 1.164)

Assignment of bits in the PMA overhead control 1, 2, and 3 registers is shown in Table 45-68a. These bits shall be reset to the default values indicated in Table 45-68a upon PHY reset. For the 100GBASE-KP4 PHY the use of these registers is specified in 94.2.2.3 and 94.2.4.1.

Table 45-68a PMA overhead control 1, 2, and 3 register bit definitions

Bits	Name	Description	R/W
1.162.7:0	PMA transmit overhead pattern	Bit pattern for 8-bit transmit overhead group	R/W
		Default = 01100110	
1.162.13:8	PMA transmit overhead sequence 0	Sequence of overhead groups for lane 0	R/W
		Default = 00110	
1.162.15:14	Reserved	Value always 0, writes ignored	R/W
1.163.4:0	PMA transmit overhead sequence 1	Sequence of overhead groups for lane 1	R/W
		Default = 01010	
1.163.9:5	PMA transmit overhead sequence 2	Sequence of overhead groups for lane 2	R/W
		Default = 10101	
1.163.14:10	PMA transmit overhead sequence 3	Sequence of overhead groups for lane 3	R/W
		Default = 11001	
1.163.15	Reserved	Value always 0, writes ignored	R/W
1.164.7:0	PMA receive overhead pattern	Bit pattern for 8-bit receive overhead group	R/W
		Default = 01100110	
1.164.15:8	Reserved	Value always 0, writes ignored	R/W

Add new section 45.2.1.89b

45.2.1.89a PMA overhead status 1 and 2 registers (1.165, 1.166)

Assignment of bits in the PMA overhead status 1 and 2 registers is shown in Table 45-68b. These bits shall be reset to all zeros upon PHY reset. For the 100GBASE-KP4 PHY the use of these registers is specified in 94.2.4.1.

Table 45-68b PMA overhead status 1 and 2 register bit definitions

Bits	Name	Description	RO
1.165.5:0	PMA receive status 0	Sequence of overhead groups for lane 0	RO
1.165.11:6	PMA receive status 1	Sequence of overhead groups for lane 1	RO
1.165.15:12	Reserved	Value always 0, writes ignored	RO
1.166.5:0	PMA receive status 2	Sequence of overhead groups for lane 2	RO
1.166.11:6	PMA receive status 3	Sequence of overhead groups for lane 3	RO
1.166.15:12	Reserved	Value always 0, writes ignored	RO

Comment #19
Additive noise spectral bound

Comment #19

Cl **94** *SC* **94.3.13.4.1** *P* **277** *L* **32** # 19

Moore, Charles Avago Technologies

Comment Type **T** *Comment Status* **X**

The test channel Gaussian white noise source is not well speced. It cannot be ideally white an Gaussian. Need limits.

SuggestedRemedy

Add to 94.3.13.4.1:

The noise, measured at TP5A, due to the test channel Gaussian white noise source must have a crest factor at least 4 and be flat to within +/-3dB from 0.5 GHz to 6.875 GHz with the noise spectra density at 6.875 GHz no more than 1.5 dB below its maximum value. The added white Gausian noise is the RMS value of the noise over the frequency range from 0 to 6.875 GHz.

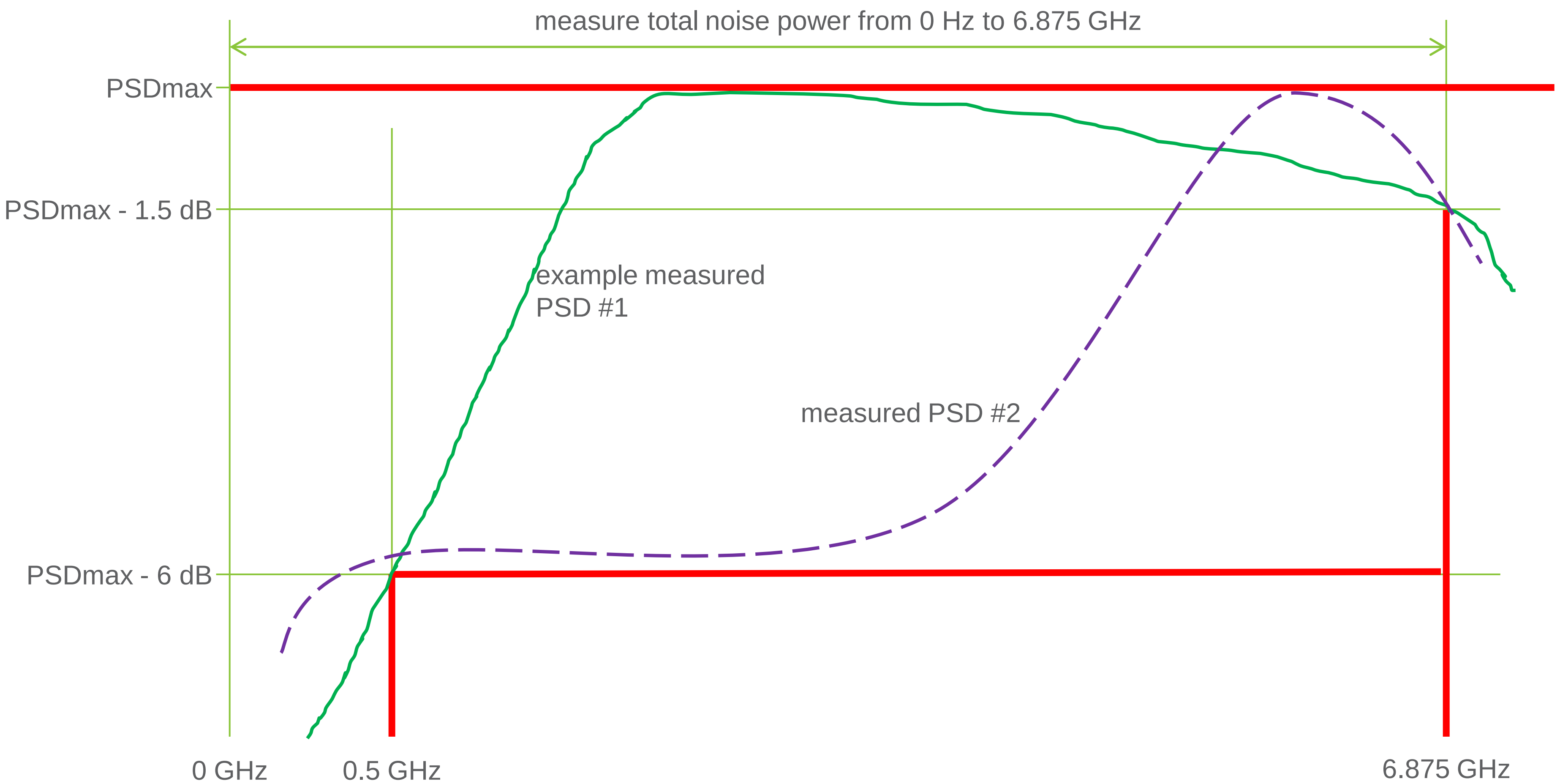
Proposed Response *Response Status* **W**

[CommentType not specified. Set to T.]

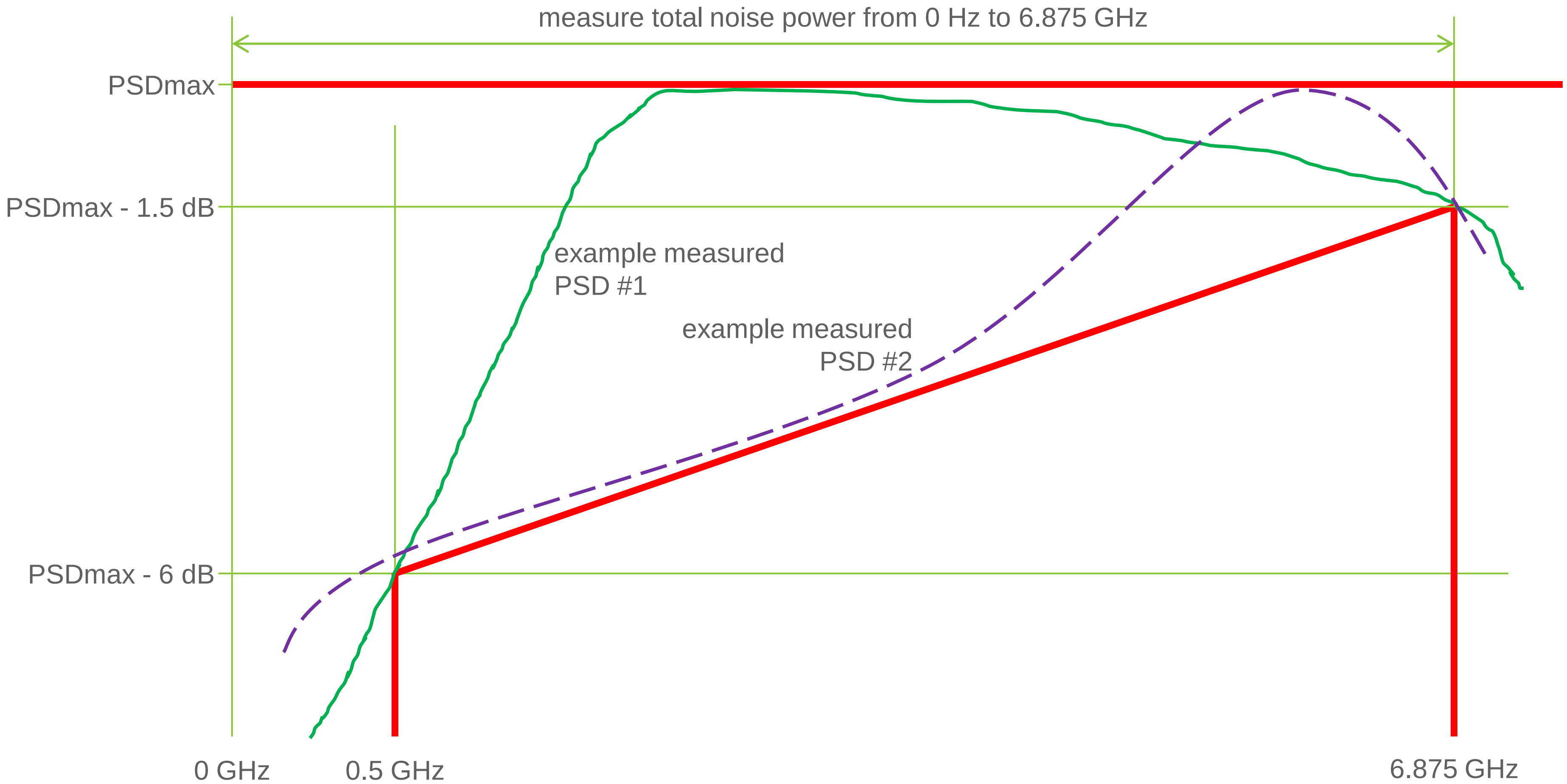
The following slide show a spectral density template depicting the description in comment #19.

The subsequent slide shows an alternative template that provides the general qualities but bounds the spectral density a bit tighter.

Noise power spectral density (PSD) template #1



Noise power spectral density (PSD) template #2



Noise spectral bound

- Which template style is appropriate?
- Other modifications?
- Is the noise white and/or Gaussian?
  - By allowance for +/- 3 dB variation over frequency, the noise is not flat in frequency, so it is not white.
  - Since the noise is truncated to a crest factor of 4 it is not Gaussian, though it may have a PDF similar to Gaussian to 4 * sigma.

Suggested text

- Assuming template #1.
  - The noise, measured at TP5A, due to the test channel noise source must have a crest factor of at least 4 and shall vary by no more than +/-3dB from 0.5 GHz to 6.875 GHz with the noise spectral density at 6.875 GHz no more than 1.5 dB below its maximum value. The noise level is the RMS value of the noise over the frequency range from 0 to 6.875 GHz.
- Assuming template #2.
  - The noise, measured at TP5A, due to the test channel noise source must have a crest factor of at least 4 and must and a PSD(f) within a range bounded by PSDmax and a straight line from PSDmax minus 6 dB at 0.5 GHz and PSDmax minus 1.5 dB at 6.875 GHz (see Figure 94-xx). The noise level is the RMS value of the noise over the frequency range from 0 to 6.875 GHz.

Comment #114
SNDR measurement window

Comment #114

Cl **94** *SC* **94.3.12.9** *P* **275** *L* **29** # 114

Healey, Adam LSI Corporation

Comment Type **T** *Comment Status* **X**

The RMS distortion error is computed for each phase m = {1, 2, ..., M} and the maximum value is used to compute SNDR. It unclear why all phases should be considered since a practical receiver will sample close to the center of the eye and distortion around the transitions will not be seen. Given that an averaged waveform is the basis for the SNDR measurement, EOJ is likely to be the major source of distortion around the transitions but this parameter is bounded separately. Note that it can be shown that the 19 dB SNDR requirement cannot be satisified if EOJ is 3% (maximum allowed value).

SuggestedRemedy

Constrain the computation of RMS distortion error to a window spanning no more than [-0.25, 0.25] UI relative to some a nominal sampling point near the eye center.

Proposed Response *Response Status* **O**

Proposed changes to 94.3.12.9.

- Add the following steps after step 1:
  - 2. Calculate the linear fit waveform z(k)=P*X1, where P and X1 are determined according to 94.3.12.6.1.
  - 3. Determine the mean zero crossing point, t_{ZC}, from z(k).
  - 4. Resample e(k) with M_0 samples per UI to yield $e(k_0)$, where: M_0 is a multiple of 4 and equal to or greater than 8; and the first sample, e(0), is aligned with t_{ZC}.
- Change step 2 to the following:
  - 5. Calculate the standard deviation, σ_e, of $e(k_0)$, where $mod(k_0,M_0) = \{M_0/4,\ldots,3*M_0/4-1\}$. This is the output noise and distortion error.

Comment #226
COM budget considerations

Comment #226

Cl **94** *SC* **94.4.1** *P* **279** *L* **18** # 226

Brown, Matthew Applied Micro

Comment Type **T** *Comment Status* **X**

The editor's note points out that the required COM value of 4 dB includes allocation for receiver package penalty and transmitter step size.

It is important for consistent interpretation that the scope of the COM value be clearly defined.

SuggestedRemedy

Add text and/or table that explains the penalties taken into consideration by the specified COM value. A proposal will be provided.

Proposed Response *Response Status* **O**

The editor’s note includes the following text: “The COM value 4 dB, includes:(a) allocation of 1 dB to address the penalty due to the receiver package insertion loss, and(b) allocation for transmitter step size penalty. See comment Draft 1.2 comments 47 and 181.”

Proposed text

- Add the following sentence to the first paragraph in 94.4.1.
  - The specified COM value includes allocation for receiver implementation limitations including the package insertion loss and allocation for non-zero transmitter tap step size.

Comment #229
Peak of p(k)

Comment #229

CI 94 SC 94.3.12.6.2 P 272 L 50 # 229

Brown, Matthew Applied Micro

Comment Type T *Comment Status* X

The peak value of p(k) should be increased to enforce faster transition time at the transmitter. It is reasonable to expect that the transition time should be similar to that achievable by a PAM2 transmitter. In other words, the assumed transmitter bandwidth may be doubled and the peak value of p(k) can be derived on this basis. The current transmitter bandwidth assumption is 0.375*fb.

SuggestedRemedy

Select a value for peak value of p(k) such that worst case transmitter bandwidth is 0.75*fb.

Proposed Response *Response Status* O

Proposed update

- Analysis and suggested value will be provided in an updated version of this presentation.

Thanks!