RS-FEC Operating Modes and Analysis regarding marking error blocks

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RS-FEC Receiver Modes*

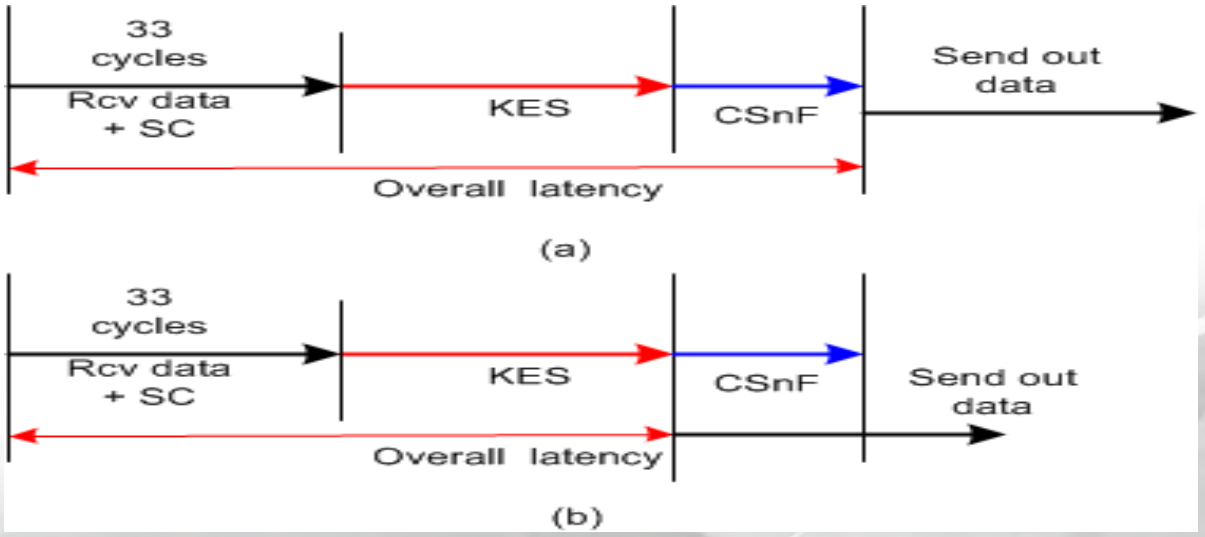
- Mode-A: perform error correction and mark error FEC blocks
- Mode-C: perform error correction, but not mark error blocks
- Mode-B: bypass data (except reverse transcoding), not mark error blocks
- Mode-D: perform error detection and mark error blocks

* Please also refer to Adee Ran's presentation in IEEE p802.3bj, Jan. 2013

Mode-A and C

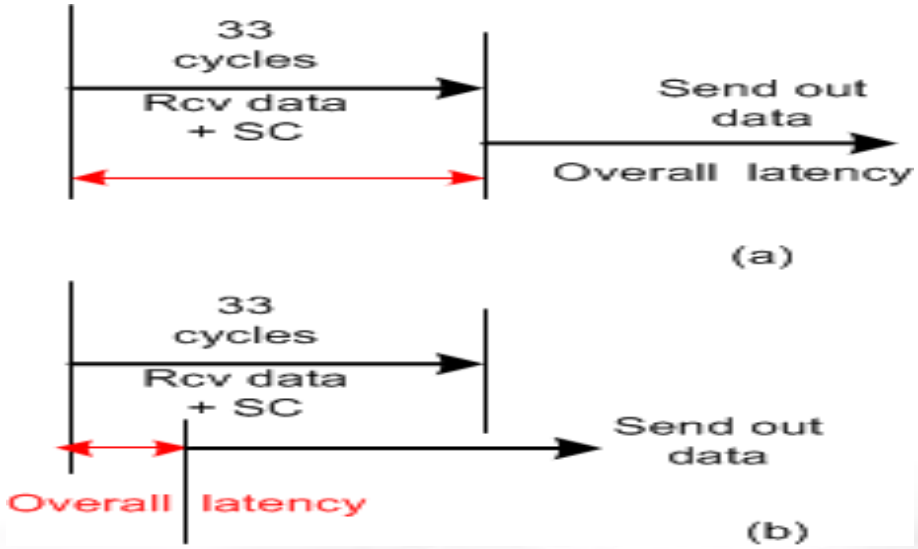
- With regular operations, one can achieve 100ns or less latency as shown in Fig. (a), e.g., 51ns+(14+14)x1.55ns/c + 5ns = 99.4ns, 80ns or even 70ns of latency is possible at increased cost.

- A simple way to save latency is shown in Fig (b). In this case, the RS-FEC decoder starts to correct data and send it out before checking if the current block is decodable or not. It could save 10 ~ 25ns of latency in general. However, to achieve comparable MTTFPA as Mode A, the BERo should be around 1e-18 or lower. Considering input BER or SER to the FEC, it should be about 6 times lower.



Mode-B and Mode-D

- For Mode-D, with regular operations, one can achieve ~55ns latency as shown in Fig. (a).
- However, there's a way to cheat latency as shown in Fig (b). The is actually Mode-B, which is really risky to network unless a kind of trailing detection is performed and marking error blocks is implemented, which leads to Mode-D.

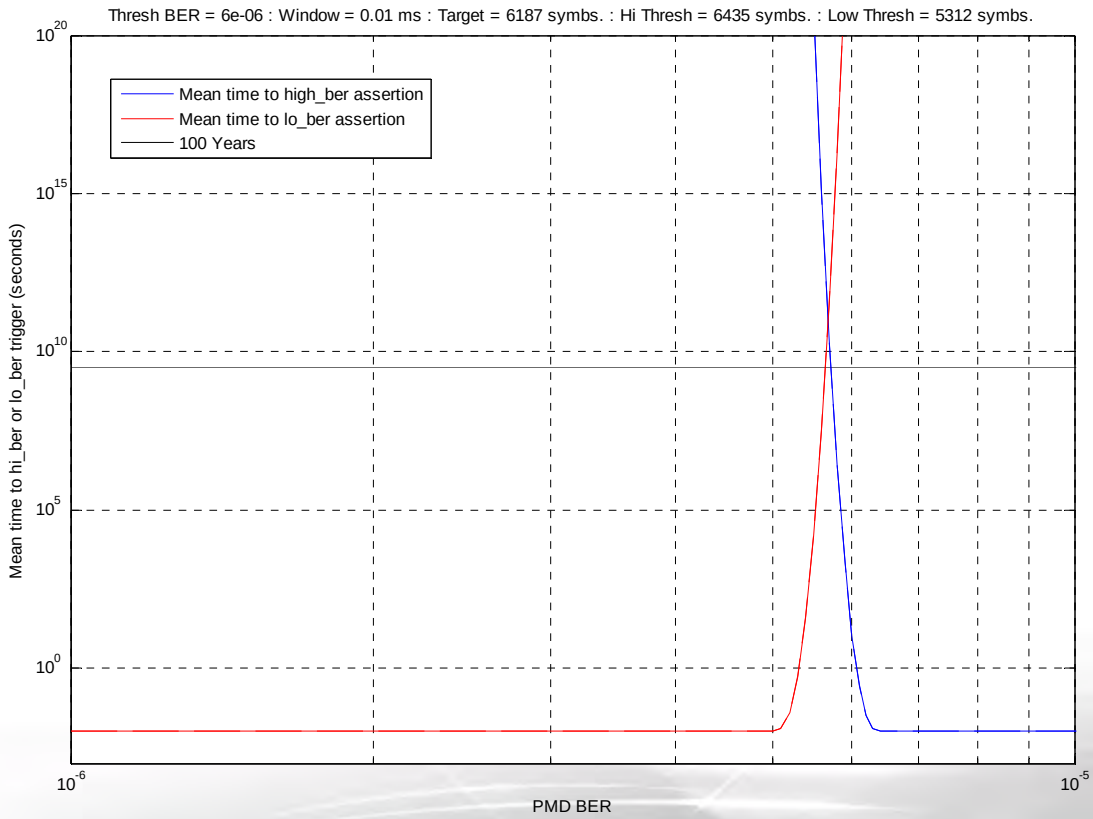


Comments (I)

- Mode-C can be allowed if a max BER or SER (RS symbol error rate) input to FEC is specified.
  - In 1 ms, the total RS symbol errors (at input of FEC) should be about 600 ~ 700 when targeting an output BER of 1e-18 or equivalent FER. Setting an threshold at hundreds should be robust and reliable for the system to switch modes.
    - ✓ **Suggest to count total RS symbol errors in an observation window, e.g., 1ms, or 2^14 (valid) FEC blocks, and use it as the major metric to determine operating mode A or C.**
  - A hysteresis scheme can be adopted, e.g., only switch to Mode-C when seeing SER < 480 per 16K FEC blocks, must switch back to Mode-A if seeing a SER > 520 per 16K FEC blocks.
- Mode-B is risky, should not be allowed.

Simulation and Analysis

- Increasing the window time for the detection of errored RS symbols improves the performance of the hi_ber state machine for mode C.
- As an example results for a target PMD BER of 6e-6 using a 10ms window are presented below.



Comments (II)

- With a 10ms window hi_ber will be asserted in about one second if the PMD BER increases to 6e-6.
- If the PMD BER is 5.5e-6 then the mean time to hi_ber assertion is >100 years. i.e. The probability of false positive is very low, even for BERs that are close to the limit.
- If the PMD is higher than 6e-6 the mean time to hi_ber assert is 10ms.
- Once in the hi_ber state we can use a lower threshold of symbol errors to indicate when to exit the hi_ber state. Again if we use 10ms as a window size this system is very reliable.
- However more work is needed to tune the thresholds and state machine. We also need to make sure the system is robust to different DFE coefficients. This is work in progress.