IEEE 802.3bj/D1.0 100GBASE-CR4
Test Points and Parameters

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Purpose

- **Provide values for Clause 92 - 100GBASE-CR4 parameters to be determined (TBD's).**

Contributors

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802.3bj Transmitter characteristics at TP2

Parameter	Subclause reference	Value	Units
Signaling rate, per lane	92.8.3.9	25.78125±100 ppm	GBd
Unit interval nominal	92.8.3.9	38.787879	ps
Differential peak-to-peak output voltage (max) with Tx disabled		30	mV
Common-mode voltage limits	72.7.1.4	0 to 0.8 [1.9]	V
Differential output return loss (min)	92.8.3.1	See Equation (92–1)	dB
Common-mode AC output voltage (max., RMS)		30	mV
Amplitude peak-to-peak (max)	72.7.1.4	1200[a]	mV
Transmitter DC amplitude[b]	92.8.3.3	0.34 min, 0.6 max	V
Linear fit pulse (min)[c]	92.8.3.3	0.52 [0.63] x Transmitter DC amplitude	V
Transmitted waveform max RMS normalized error (linear fit), "*e*" abs coefficient step size minimum precursor fullscale range minimum post cursor fullscale range	 92.8.3.3 92.8.3.3.2 92.8.3.3.3 92.8.3.3.3	 0.037 0.0083 min, 0.05 max 1.54 4	
Far-end transmit output noise (max) Low insertion loss channel High insertion loss channel	92.8.3.2	 2 Equation (92–2) 1 Equation (92–3)	mV
Max output jitter (peak-to-peak) Random jitter[d] Duty Cycle Distortion[e] Total jitter excluding data dependent jitter[f]		 0.15 0.035 0.28 [0.25]	 UI UI UI

[a]The 100GBASE-CR4 Style-1 connector may support 100GBASE-CR4 or XLPPI interfaces. For implementations that support both interfaces, the transmitter should not exceed the XLPPI voltage maximum until a 100GBASE-CR4 cable assembly has been identified.
[b]The transmitter DC amplitude is the sum of linear fit pulse response $p(k)$ from step 3) divided by M from step 3).
[c]The peak of the linear fit pulse response $p(k)$ from step 3).
[d]Random jitter is specified at a BER of 10^{-12}
[e] See 72.7.1.9 for duty cycle distortion definition.
[f]Total jitter at a BER of 10^{-12} measured per 83A.5.1 excluding data dependent jitter (DDJ). DDJ is a jitter component where jitter that is not correlated to the data pattern has been removed. DDJ is measured with PRBS9 as specified in 83.5.10.

(92–1)

$$Return\_loss(f) \geq \begin{cases} 12 - 1.24\sqrt{f} & 0.01 \leq f < 10.31 \\ 6.3 - 13\log_{10}(f/13.75) & 10.31 \leq f \leq 25 \end{cases} \quad \text{(dB)}$$

where

f is the frequency in GHz
$Return\_loss(f)$ is the return loss at frequency f

(92–2)

$$RMSl_{dev} \leq \sqrt{\sigma_l^2 + 2^2} \text{ (mV)}$$

(92–3)

$$RMSh_{dev} \leq \sqrt{\sigma_h^2 + 1^2} \text{ (mV)}$$

Table values: Charles Moore, Avago Technologies

802.3bj Receiver characteristics at TP3

Table 92–7—Receiver characteristics at TP3 summary

Parameter	Subclause reference	Value	Units
Bit error ratio	92.8.4.3	10^{-12} or better	
Signaling rate, per lane	92.8.4.4	25.78125 ± 100 ppm	GBd
Unit interval (UI) nominal	92.8.4.4	38.787879	ps
Differential peak-to-peak input amplitude tolerance (max)	72.7.2.4	1200	mV
Differential input return loss (min)[a]	92.8.4.1	Equation (92–17)	dB
Differential to common-mode input return loss		10 min from 10 MHz to 25 GHz	dB

[a]Relative to 100 Ω differential.

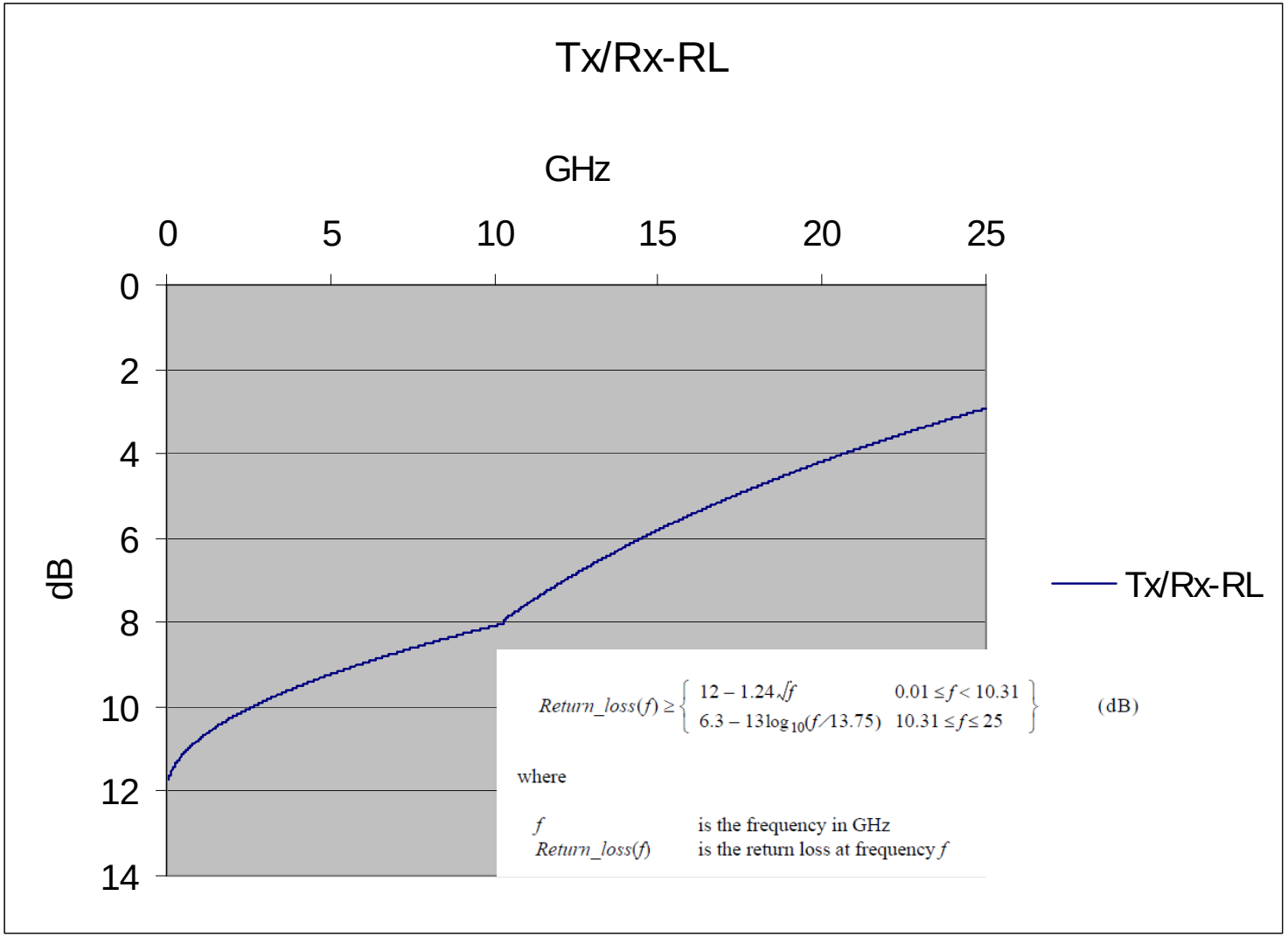
Table values: Charles Moore, Avago Technologies

$$Return\_loss(f) \geq \begin{cases} 12 - 1.24\sqrt{f} & 0.01 \leq f < 10.31 \\ 6.3 - 13\log_{10}(f/13.75) & 10.31 \leq f \leq 25 \end{cases} \quad \text{(dB)} \qquad (92\text{–}17)$$

where

f is the frequency in GHz
$Return\_loss(f)$ is the return loss at frequency f

Tx and Rx – Return Loss



802.3bj Receiver interference tolerance test and parameters

Table 92–8—100GBASE-CR4 interference tolerance parameters

Parameter	Test 1 values	Test 2 values	Units
Maximum BER	10^{-12}	10^{-12}	
Fitted insertion loss coefficients	$a_1 = 2.82$ $a_2 = 0.08$ $a_4 = 0.02$	$a_1 = 4.59$ $a_2 = 0.19$ $a_4 = 0.02$	dB/√GHz dB/GHz dB/GHz^2
Applied SJ[a] (peak-to-peak)	0.115	0.115	UI
Applied RJ[b] (peak-to-peak)	0.13	0.13	UI
Applied DCD (peak-to-peak)	0.035	0.035	UI
Calibrated far-end crosstalk (RMS)	6.3	2.2	mV
Calibrated ICN (RMS) – σ_{nx}	3.7	3.7	mV

[a]Applied SJ frequency >15 MHz, specified at TP0.
[b]Applied random jitter at TP0 is specified at 10^{-12}.

Table values: Charles Moore, Avago Technologies

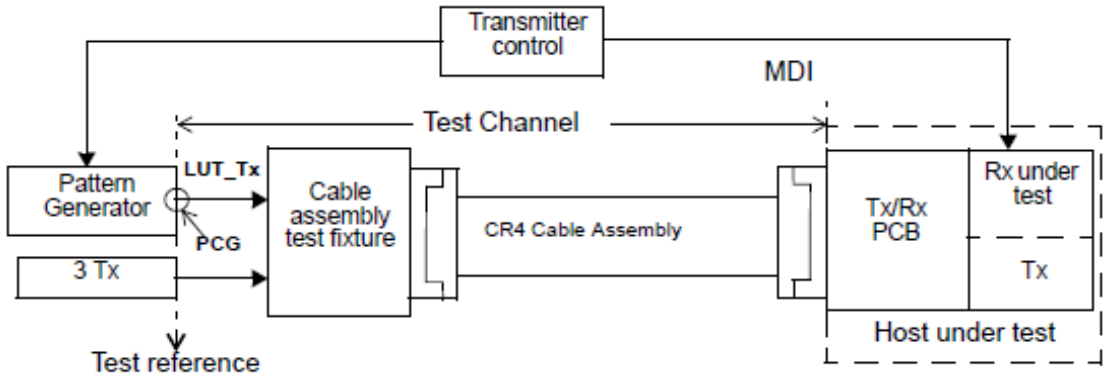


Figure 92–7—Interference tolerance test setup

802.3bj Channel definition and test points

TP0 to TP5	The 100GBASE-CR4 channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.

- 92A.2 Transmitter characteristics at TP0 [93.8.1]
- 92A.3 Receiver characteristics at TP5 [93.8.2]
- 92A.4 Transmitter and receiver differential printed circuit board trace loss [max and min]
- 92A.5 Channel insertion loss (35 dB and 30 dB)
- 92A.6 Channel return loss
- 92A.7 Channel insertion loss deviation (ILD)
- 92A.8 Channel integrated crosstalk noise (ICN)

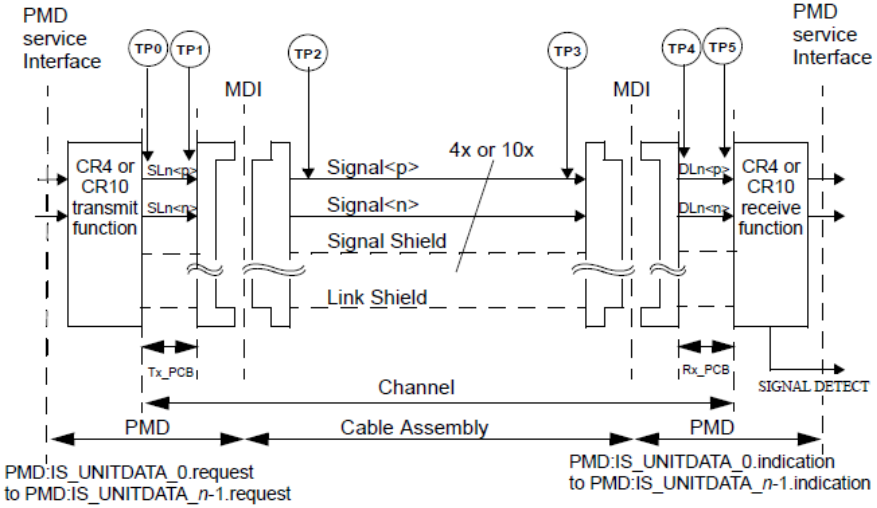


Figure 85–2—40GBASE-CR4 or 100GBASE-CR10 link (half link is illustrated)

$$IL_{PCB}(f) \geq IL_{PCBmin}(f) = 0.184(0.0694 + 0.4284\sqrt{f} + 0.9322f) \quad \text{(dB)} \qquad (92A\text{–}2)$$

for 10 MHz $\leq f \leq$ 18750 MHz.

1.25 @12.89 GHz

where

f	is the frequency in MHz
$IL_{PCB}(f)$	is the insertion loss for the transmitter and receiver PCB
$IL_{PCBmin}(f)$	is the minimum insertion loss for the transmitter and receiver PCB

802.3bj cable assembly characteristics and test points

TP1 to TP4	All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 92–2. The cable assembly test fixture of Figure 92–13 or its functional equivalent, is required for measuring the cable assembly specifications in 92.10 at TP1 and TP4.

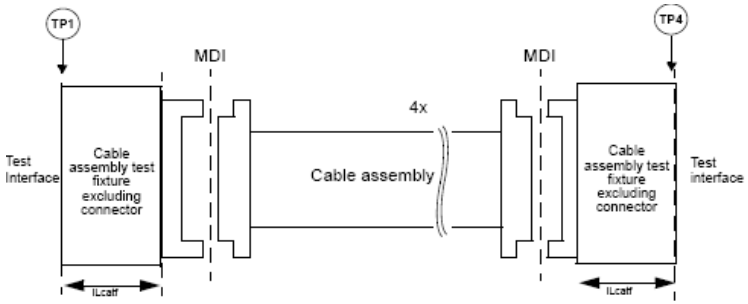


Figure 92–13—Cable assembly test fixtures

Table 92–9—Cable assembly differential characteristics summary

Description	Reference	Value	Unit
Maximum insertion loss at 12.8906 GHz	92.10.2	22.64	dB
Minimum insertion loss at 12.8906 GHz		4	dB
Insertion loss deviation at 12.8906 GHz	92.10.3	max = 2.97 min = –2.97	dB
Minimum return loss at 12.8906 GHz	92.10.5	6.0	dB
MDNEXT loss	92.10.5	Equation (92–26)	dB
MDFEXT loss	92.10.6	Equation (92–27)	dB
Maximum integrated crosstalk noise	92.10.7	Equation (92–33)	mV

TBD

802.3bj Test fixtures; test points and parameters

The test fixtures are specified in mated state Figure 92-14

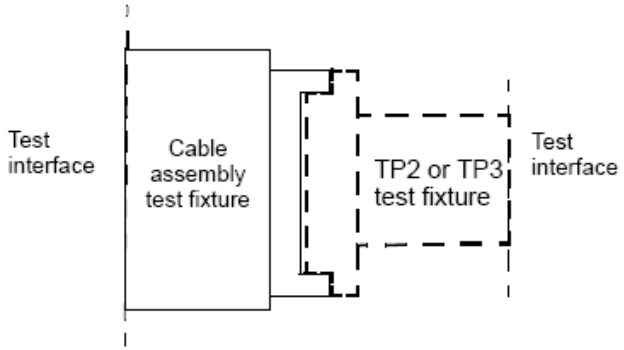


Figure 92–14—Mated test fixtures

- 92.10.8 Cable assembly test fixture
- 92.10.9 Mated test fixtures
- 92.10.9.1 Mated test fixtures insertion loss
- 92.10.9.2 Mated test fixtures return loss
- 92.10.9.3 Mated test fixtures common-mode return loss
- 92.10.9.4 Mated test fixtures common-mode conversion loss
- 92.10.9.5 Mated test fixtures integrated crosstalk noise