Package Representation Fine-Tuning

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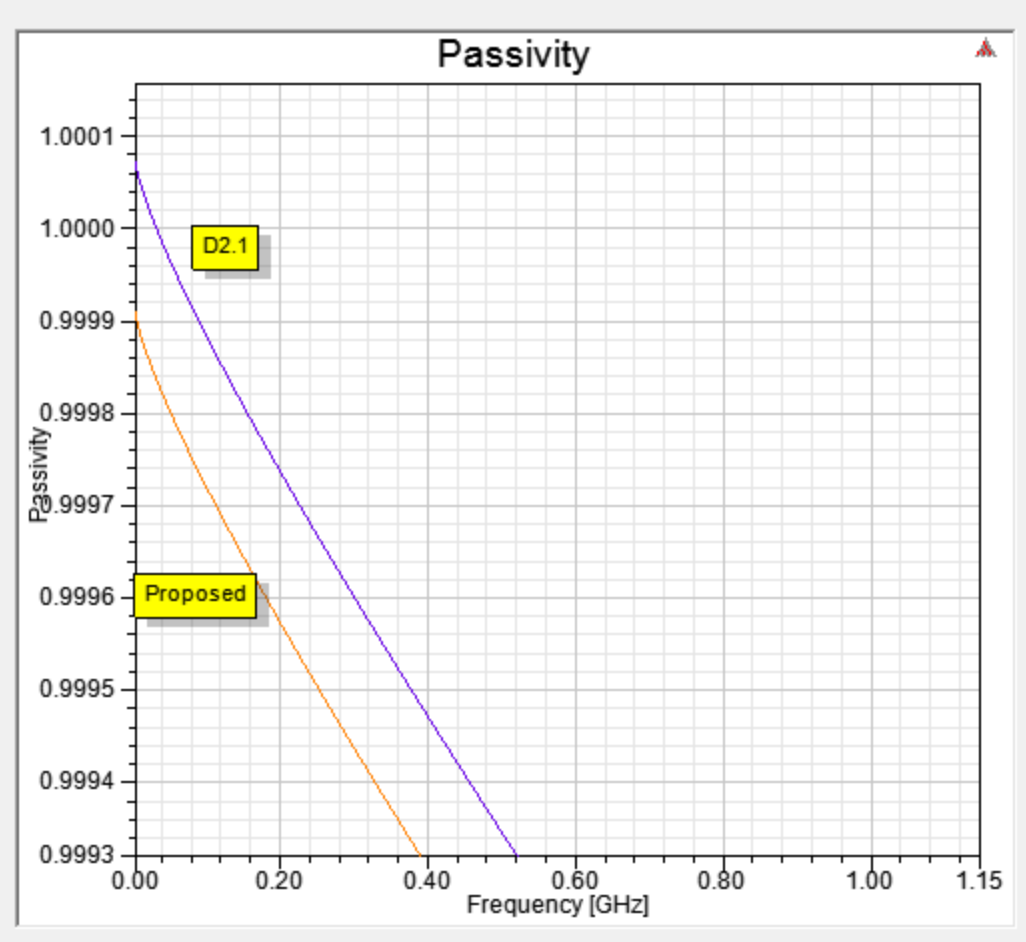
PKG Transmission Line Passivity

Clause 93a package transmission line representation in draft D2.1 is very slightly non-passive.



Proposed Changes for γ's and ρ's for 1 mm Package Segment

The suggested remedy for Comment #69: Replace the coefficients in Table 93A–2—"Transmission line model parameters"

D2.1

gamma complex([-0.0010037 -0.0003539 -0.001027 0 -1.178e-05], [0 -0.003355 -0.03818 0 3.363e-05])
rho complex([0.0011007 3.679e-18 -0.0003235 -1.021e-20 1.722e-07], [0 -0.008124 -3.545e-20 7.44e-06 -1.8e-21])

Proposed

gamma complex([-1.067e-03 -3.551e-04 -1.027e-03 0.000 -1.179e-05] ,[000 -3.357e-03 -3.818e-02 0.000 3.360e-05])
rho complex([1.001e-03 -8.004e-18 -3.233e-04 3.228e-20 1.721e-07] ,[000 -8.120e-03 -3.349e-18 7.435e-06 8.747e-21])

A Minuscule Impact on COM Result

```
Files set is: FCI_CC_Long_Link_Pair_15_to_Pair_7--FCI_CC_Long_Link_Pair_15_to_Pair_7_Through

ans =

     channel_operating_margin_dB: 4.6841
            peak_interference_mV: 26.0500
    peak_channel_interference_mV: 20.8900
                   peak_ISI_mV: 19.6500
      peak_MDXTK_interference_mV: 5.8400
                         icn_mV: 2.3457
     peak_MDNEXT_interference_mV: 5.3300
     peak_MDFEXT_interference_mV: 1.7100
    available_signal_after_eq_mV: 44.6697
              fit_loss_dB_at_Fnq: 18.7823
                    IL_dB_at_Fnq: 19.7159
                  baud_rate_GHz: 25.7813
                        ILD_RMS: 0.8157
             equivalent_ISI_ICN: 0.0012
      ctle_zero_poles_acdcgaindB: [5.7444e+09 2.5781e+10 6.4453e+09]
                    acdcgaindB: -1.0000
                     txle_taps: [-0.1800 0.6800 -0.1400]
                      dfe_taps: [14x1 double]
                sci_noise_FD_RMS: 0.1925
                cci_noise_TD_BER: 0.0058
    max_peak_interference_at_BER: 0.0209
                            FOM: 16.6489
                       dfe4_rss: 0.1991
                     file_names: [8x78 char]
```

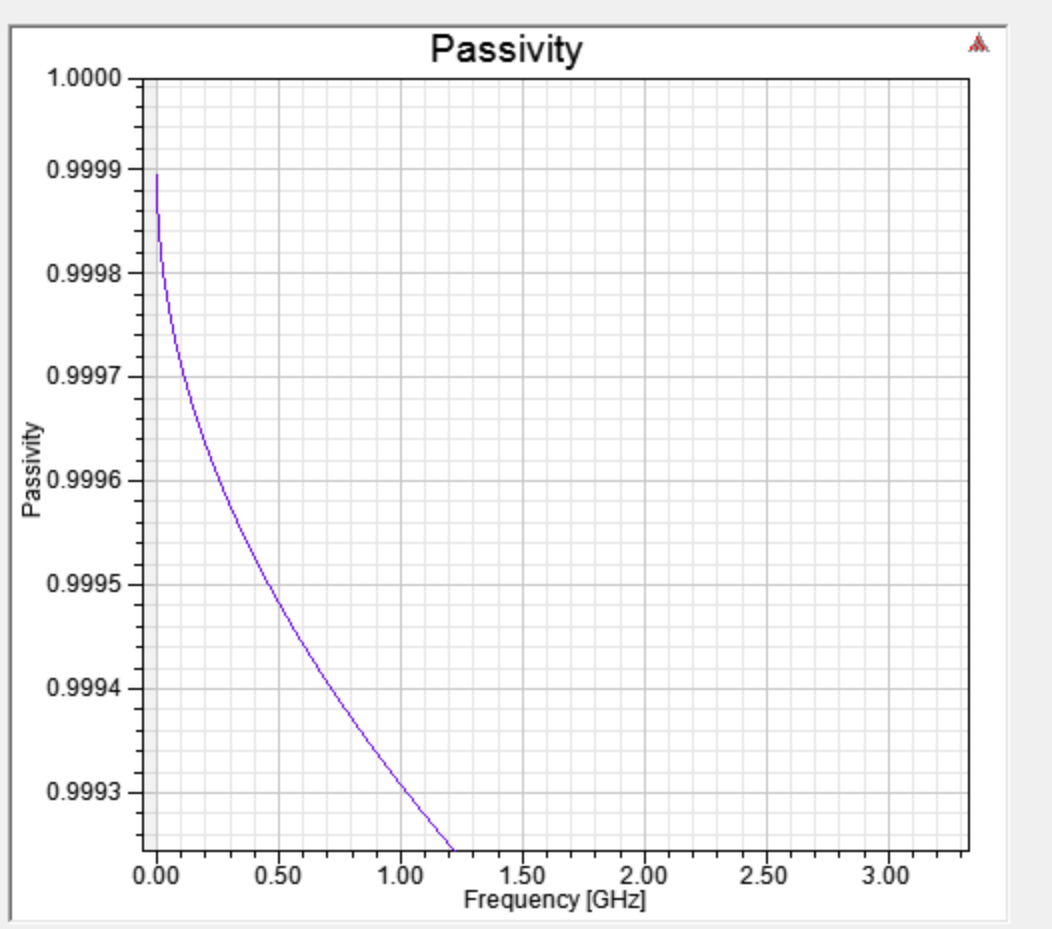
Proposed

```
     channel_operating_margin_dB: 4.6844
            peak_interference_mV: 26.0900
    peak_channel_interference_mV: 20.9300
                   peak_ISI_mV: 19.6900
      peak_MDXTK_interference_mV: 5.8600
                         icn_mV: 2.3457
     peak_MDNEXT_interference_mV: 5.3500
     peak_MDFEXT_interference_mV: 1.7100
    available_signal_after_eq_mV: 44.7399
              fit_loss_dB_at_Fnq: 18.7823
                    IL_dB_at_Fnq: 19.7159
                  baud_rate_GHz: 25.7813
                        ILD_RMS: 0.8157
             equivalent_ISI_ICN: 0.0012
      ctle_zero_poles_acdcgaindB: [5.7444e+09 2.5781e+10 6.4453e+09]
                    acdcgaindB: -1.0000
                     txle_taps: [-0.1800 0.6800 -0.1400]
                      dfe_taps: [14x1 double]
                sci_noise_FD_RMS: 0.1925
                cci_noise_TD_BER: 0.0059
    max_peak_interference_at_BER: 0.0209
                            FOM: 16.6451
                       dfe4_rss: 0.1993
                     file_names: [8x78 char]
```

D2.1

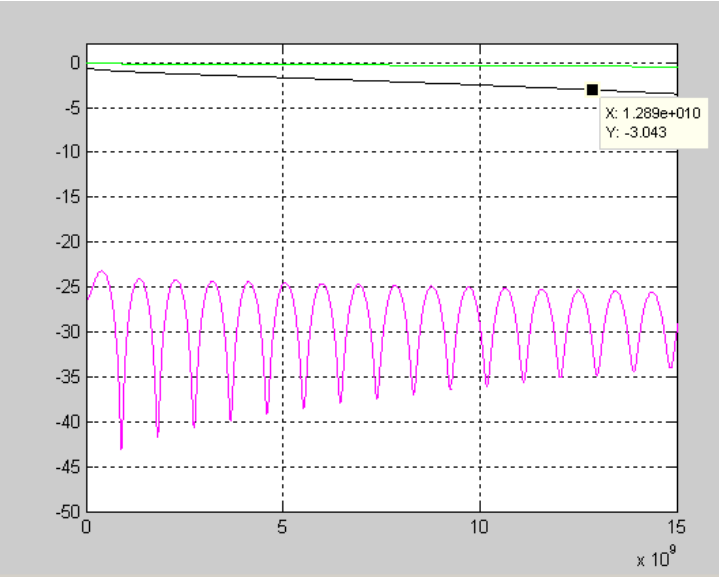
1mm CR4 Host-Board Model is Passive

➔No change is required to the host board T-Line representation coefficients



100GBase-CR4 Cross-talk Assumptions (Comment #77)

- In Draft 2.1 a CR4 host board representation was adopted according to dudek_3bj_02a_0513 and benartsi_3bj_02_0513
- A host board insertion loss of 6.26dB @ 12.89GHz was used.
- Examining the different paths of the signal it is evident that the high amount of loss is not the worst case for crosstalk impact paths, that may be routed with lower loss.
- Propose:
  - Add 6.26dB (185mm) as the Tx and Rx host board representation of the thru signal path channel, no change to D2.1 thru path implementation.
  - For NEXT and FEXT channels: add 6.26dB to Rx Host board side and 3dB (90mm) to Tx side of channel (editorial license granted)



100GBase-CR4 Host Board Representation

- In Draft 2.1 a CR4 host board representation was adopted.
- Current representation lacks discontinuities, i.e. device via break-out + connector vias (as cable MCBs can have a very optimized via construction).
- An extra 1 dB of margin (4dB instead of 3dB) was taken to account for lack of host board crosstalk as well as discontinuities.
- Analysis is still pending whether this margin is enough and whether there is a need for capacitive discontinuities at host board ends.

Thank you!

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Questions?