Defining Test Points in a Copper Back Plane / Mid Plane Implementation

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Summary: This presentation will describe possible test points and begin discussion of a Normative Channel Definition.

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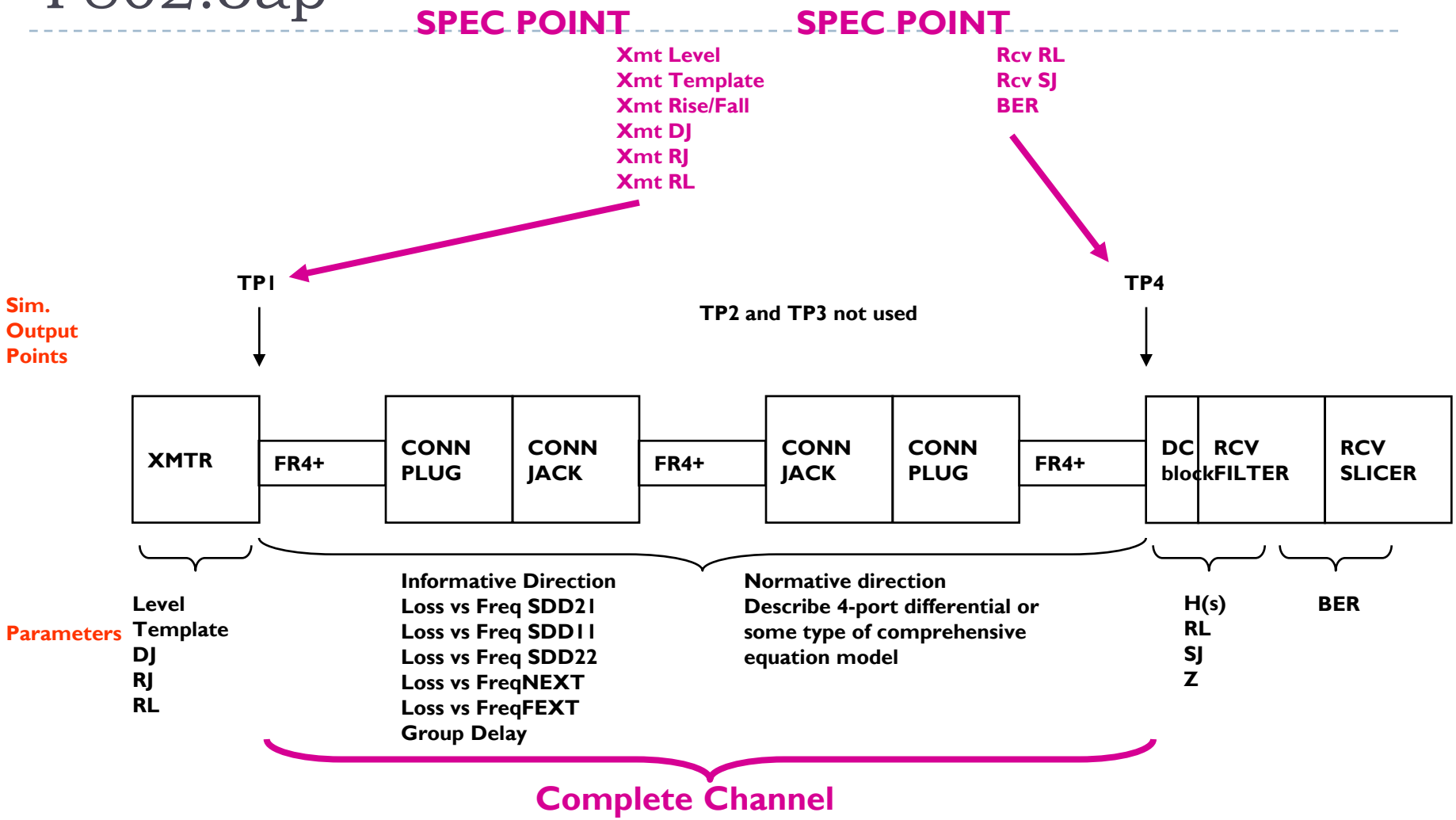
Outline

- Review test points from IEEE802.3ap
- Review proposed P802.3bj cabling test points
- Discuss test point concerns
- Propose back plane test points
- Discuss Normative Channel

ADHOC - Proposed Model for Simulation P802.3ap



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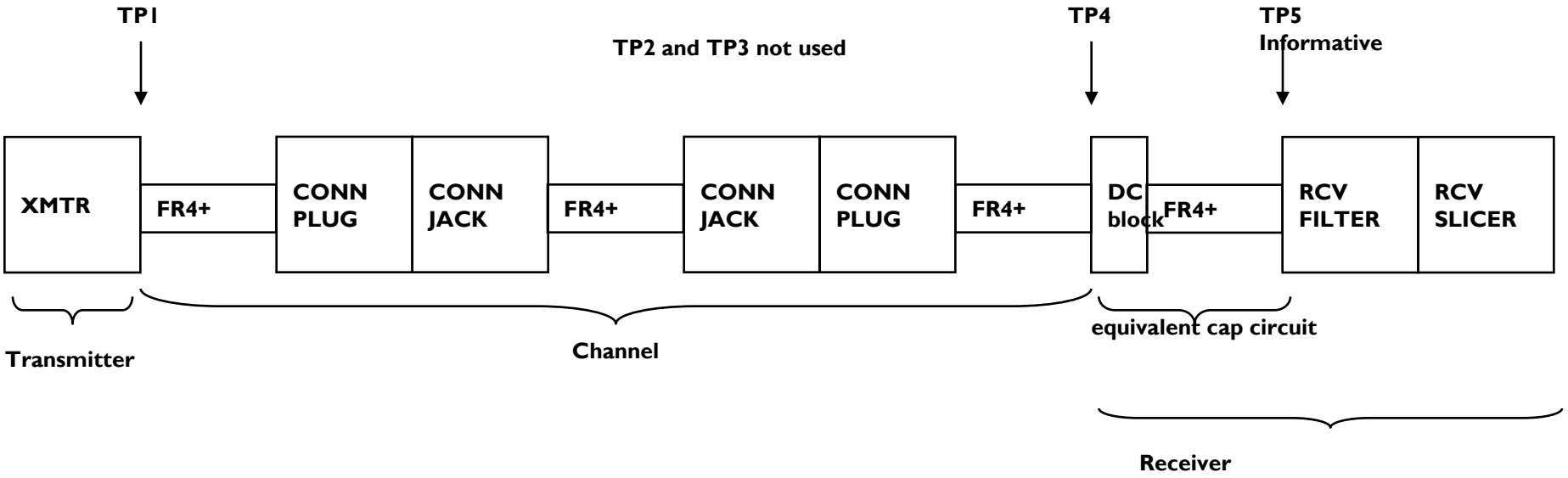
ADHOC - NEW Proposed Model for Simulation P802.3ap



Reference P802.3ap-D33.pdf Feb21, 2007

69B.2 Reference model

The backplane interconnect is defined between test points TP1 and TP4 as shown in Figure 69B–1. The transmitter and receiver blocks include all off-chip components associated with the respective block. For example, external AC-coupling capacitors, if required, are to be included in the receiver block.

Informative characteristics and methods of calculation for the insertion loss, insertion loss deviation, return loss, crosstalk, and the ratio of insertion loss to crosstalk between TP1 and TP4 are defined in 69B.4.3, 69B.4.4, 69B.4.5, 69B.4.6, and 69B.4.6.4 respectively. These characteristics may be applied to a specific implementation of the full path (including transmitter and receiver packaging and supporting components) for a complete assessment of system performance and the interaction of these components.

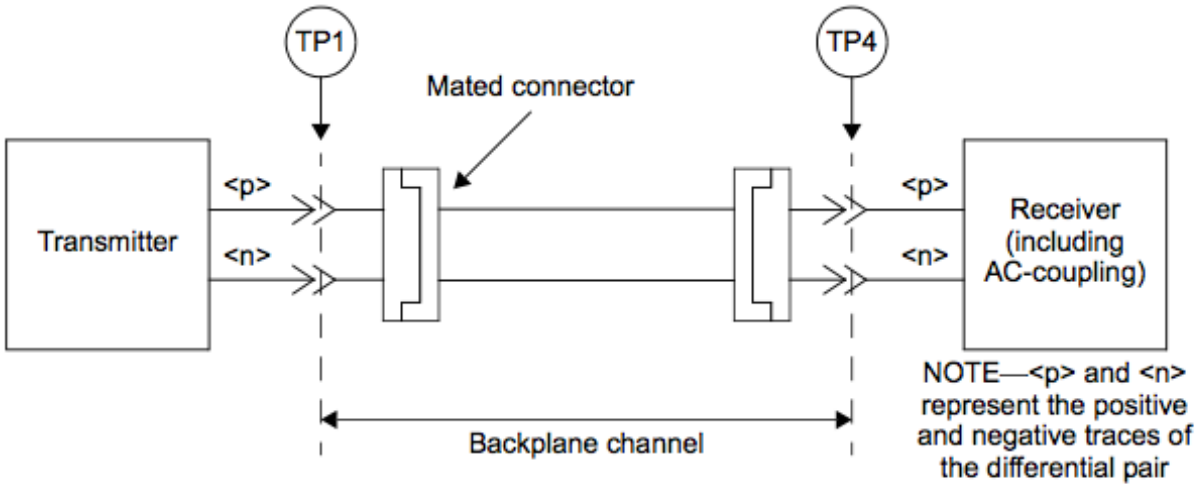


Figure 69B–1—Interconnect reference model

•Adopt Figure 85-2 and Table 85-4 as baseline for 802.3bj with applicable changes for naming transmit and receive functions and figure and clause numbering.

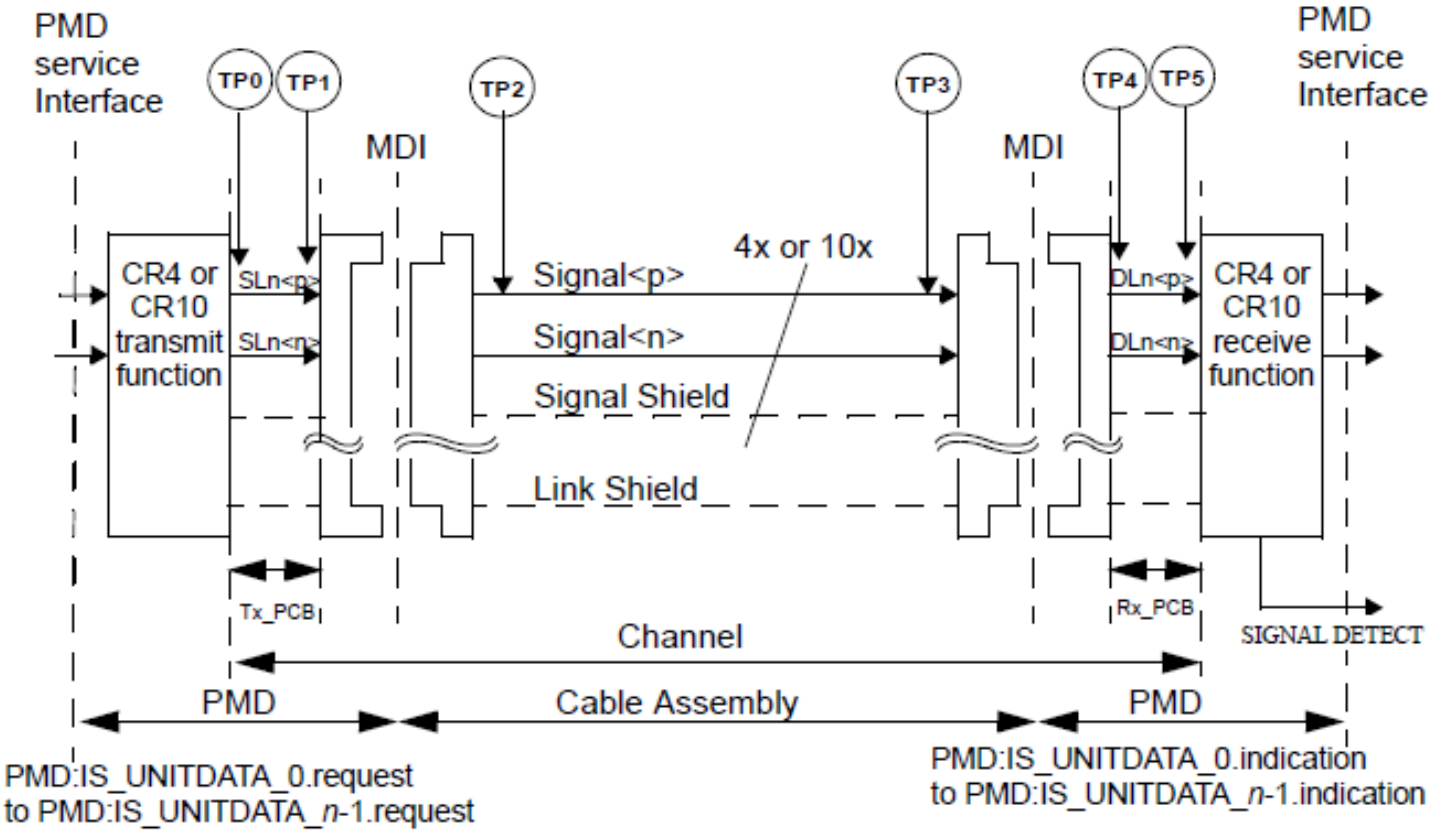


Figure 85–2—40GBASE-CR4 or 100GBASE-CR10 link (half link is illustrated)

P802.3bj test point specifications

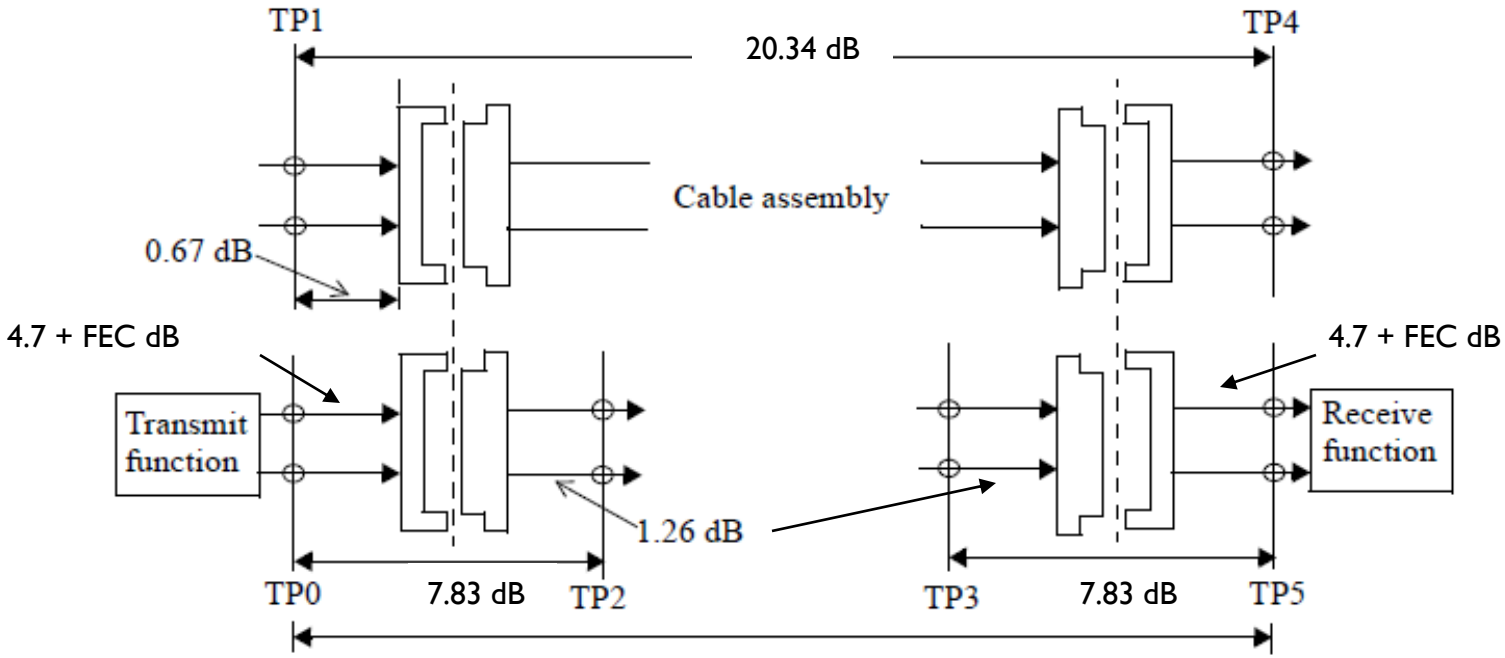
- Table 85-4

Table 85–4—40GBASE-CR4 and 100GBASE-CR10 test points

Test points	Description
TP0 to TP5	The 40GBASE-CR4 and 100GBASE-CR10 channels including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 85–2. The cable assembly test fixture of Figure 85–13 or its functional equivalent, is required for measuring the cable assembly specifications in 85.10 at TP1 and TP4.
TP0 to TP1 TP4 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 85.8.3 and 85.8.4. The maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is specified in 85.8.3.4.
TP2	Unless specified otherwise, all transmitter measurements and tests defined in Table 85–5 are made at TP2 utilizing the test fixture specified in 85.8.3.5.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 85.8.4 are made at TP3 utilizing the test fixture specified in 85.8.3.5.

P802.3bj Channel insertion loss budget >30 dB @ 12.89 GHz

Channel insertion loss budgets at 12.89 GHz



5 meter cable	3.2 dB/m	16 dB
Connector*	1.5 dB	3 dB
CA-TF loss	.67 dB	1.34 dB
cable assembly		20.34 dB
Tx/Rx PCB	4.7 + FEC dB	9.4 + FEC dB

- Adopt channel insertion loss budget as baseline for 802.3bj
>30 dB channel insertion loss budget.

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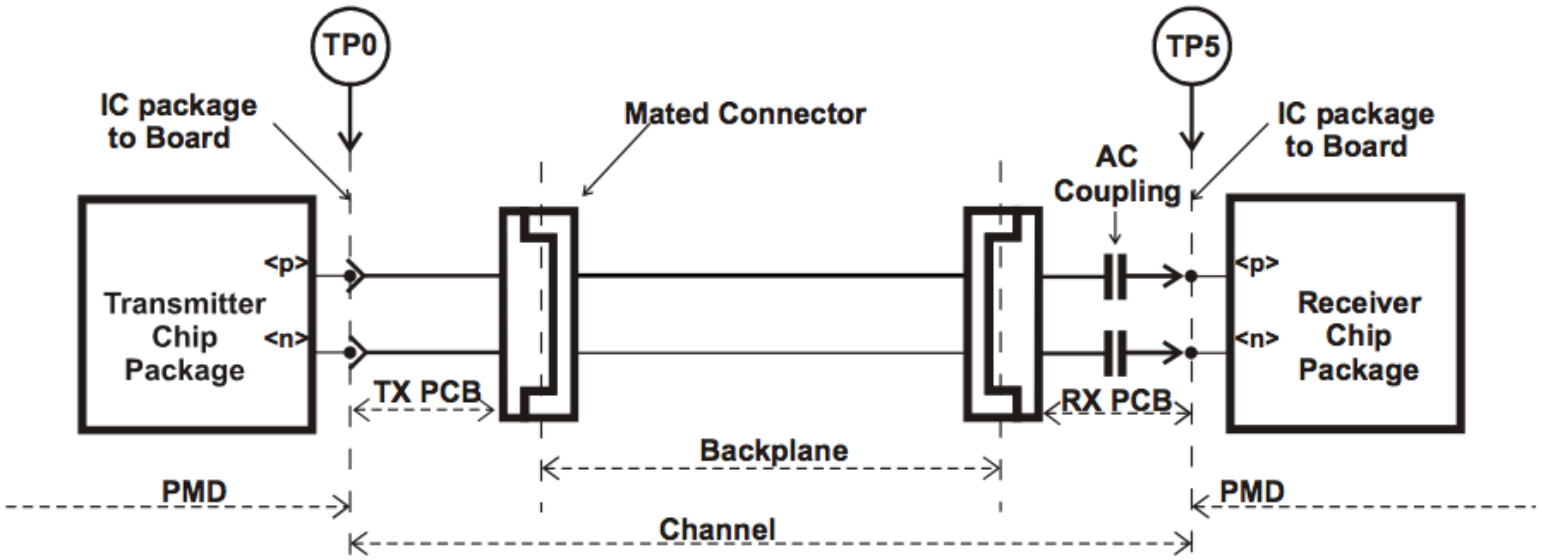
Back Plane Test Point Proposal from Jan 2012

Recommended backplane test points



Considerations:

- Aligned with the cable specification
- TP0 and TP5 defined; rationale on next slide

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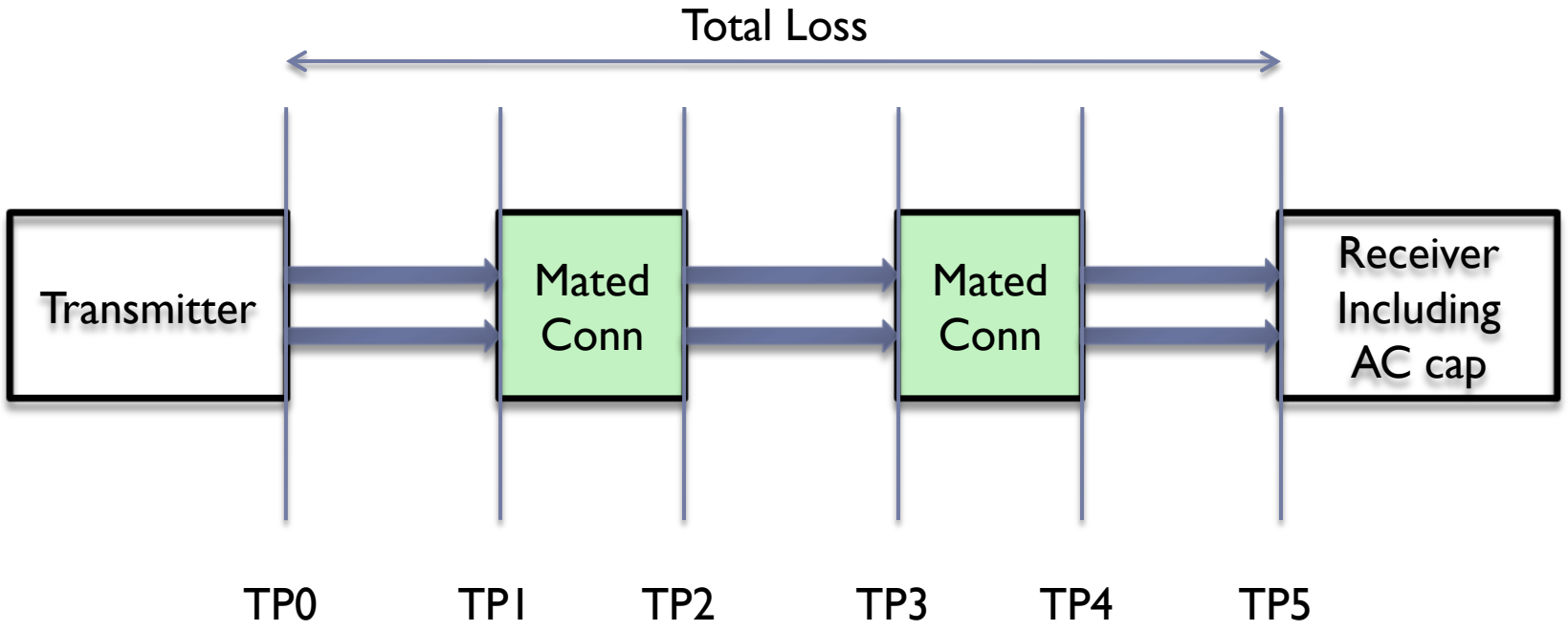
Test Point Concerns

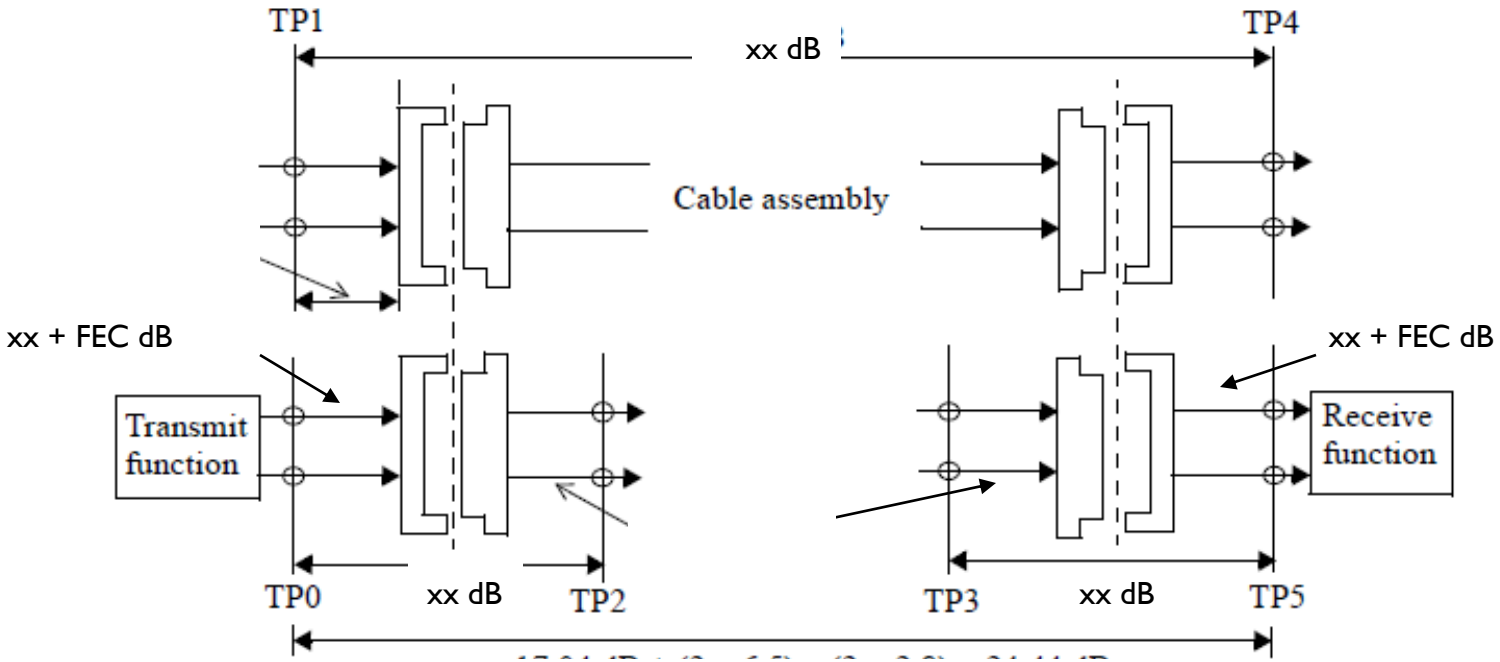
- P802.3ap
  - There was a lot of discussion on the package and the DC blocking capacitor being part of the channel.
  - There was never a solid proposal on how to allocate the capacitor characteristics to the channel.
  - The receiver was to assume the characteristics of the capacitor.
- Proposed P802.3bj Copper Cabling
  - No concerns at this time. The proposed method looks feasible.
- Possible Test Point Proposal P802.3bj Back Plane
  - This method proposes the capacitor be part of the channel.
  - There is not an established method to accurately characterize the effects of the capacitor as a function of the channel.

Back Plane Test Point Proposal

- Propose using diminico_01a_0112.pdf as the basis for the back plane channel with the terms adjusted relevant to back plane.
- Propose the Capacitor function be owned by the receiver as in P802.3ap.



Use the following breakout from Proposed Copper Cabling to define IL measurements



From diminico_01a_0112.pdf

Such a method would allow for the definition and measurement of a channel defined as Normative.
Defines partitioning points for testability / measurement points that sum for the completed channel.

Defining a Normative Channel

- Establish TP0 – TP5 locations.
- Define test fixtures using TP0 – TP5 that allow measuring and isolating TP0 – TP2, TP1 – TP4, and TP3 – TP5.
- Allows for test and verification of the channel independent of the transmitter, transmitter package, receiver, and receiver package.
  - Removes the need for advanced vendor models
  - Removes the need to share channel models with vendors
  - Reduces system testing and verification

Thank You!