IBM STG

Should the FEC be Optional for the NRZ PHY?

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Introduction

- NRZ signal integrity simulations across posted backplane and copper cable channels concluded that*:
  - Medium strength FEC required to support 25G transmission across channels having up to 35dB of loss at 12.9GHz
  - FEC may not be required for 25G transmission across channels having less than 30dB loss at 12.9GHz
    - Simulated channels however are well behaved (low Xtalk, low ILD)
    - Simulated link margins can quickly vanish due to several factors
      - Higher ILD/Xtalk, differential skew, manufacturing variability, lower cost package, Energy Efficient Ethernet induced supply bounce, etc…

*meghelli_01_0911, beukema_01_1111

Optional FEC as in 10GBase-KR?

- Several medium strength FEC options have been suggested for the 4-lane 100G NRZ PHY*
  - The option 1 recommended by the FEC consensus building group has low latency, low power/area and yet provide close to 5dB of effective coding gain
  - Estimated power and area numbers in 40nm technology node are conservative and actual implementation can be far more efficient

Option	FEC Code RS(n, k, t, m)	Trans-coding	Effective Gain BER= 10^{-15}	Overall Latency	Total Area (40nm gates)	Total Power	Input BER for 10^{-15} BER	Input BER for 10^{-12} BER
1	RS(528, 514, 7, 10)	256b/257b	4.87 dB	94.3 ns	244k	90 mW	4.68×10^{-6}	2.34×10^{-5}

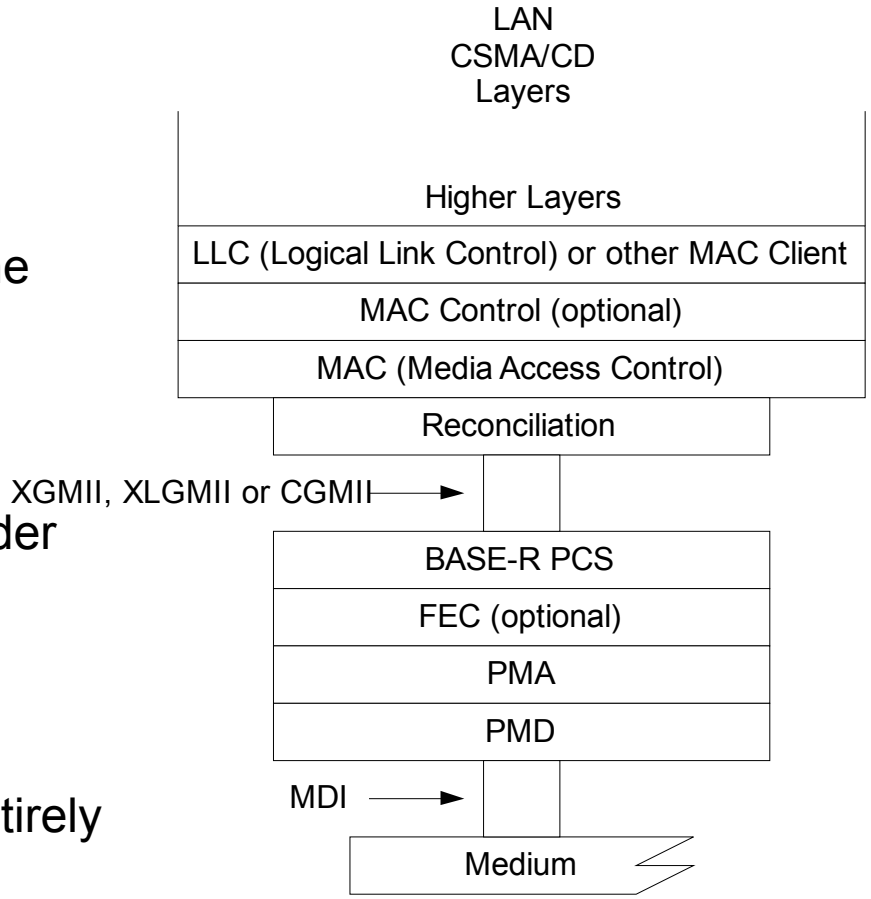
- But we did not really discussed the FEC usage options, or maybe the thought is that, like in 10GBase-KR, it will be optional… but should it be?

*Gustlin_01_0312

10GBASE-KR FEC *(Clause 74)*

FEC sublayer

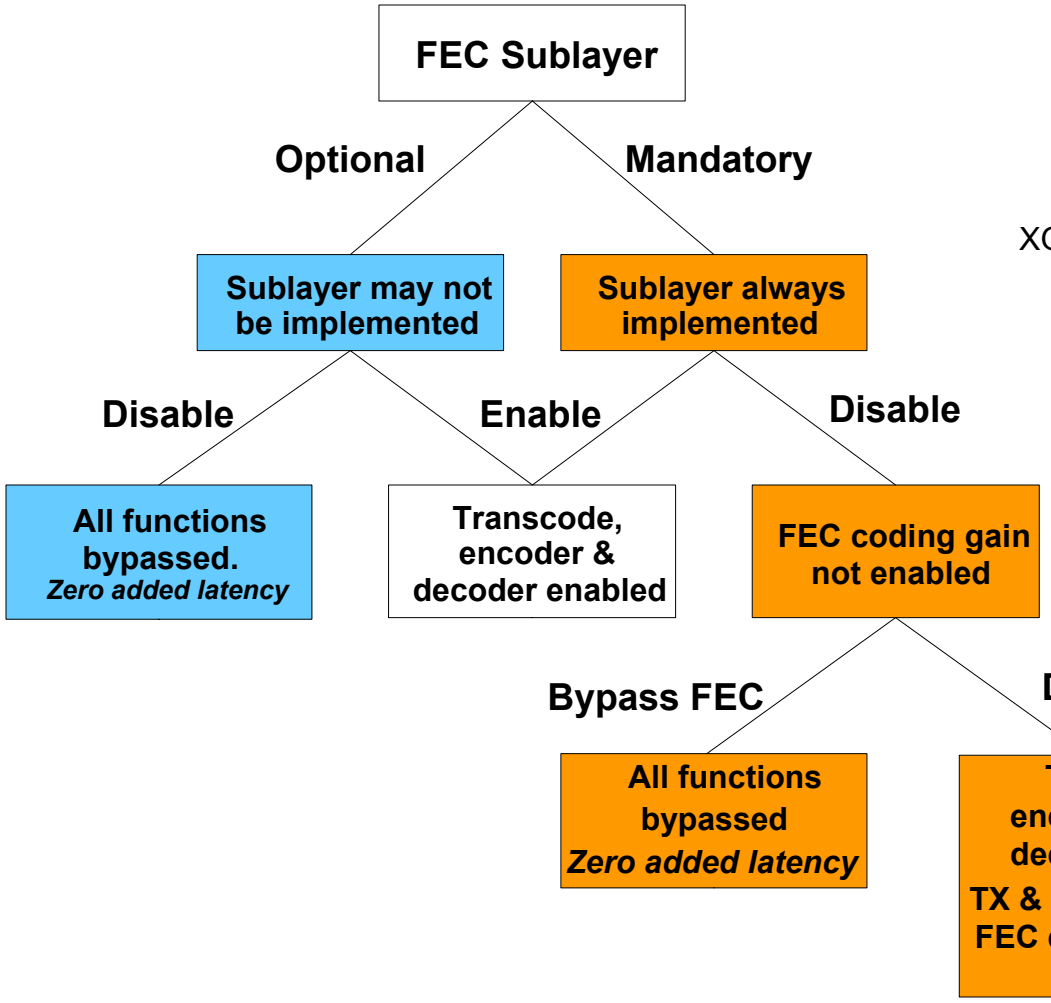
- Is optional
  - A compliant device may not include the sublayer at all
- Contains transcoding & FEC
  - No provision for turning off FEC decoder only
- Can be enabled / disabled
  - Bypasses FEC encoder & decoder entirely
  - Zero latency adder when disabled

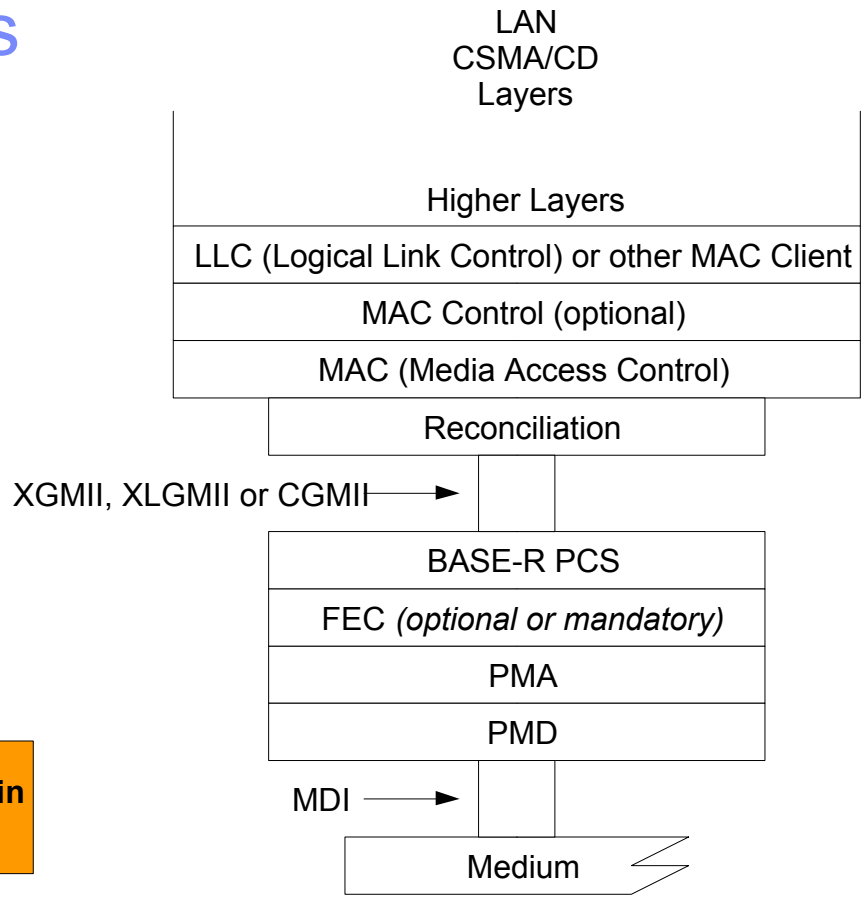


74.8.2 FEC Enable

The FEC sublayer shall have capability to enable or disable the FEC function. An MDIO interface or an equivalent management interface shall be provided to access the variable FEC_Enable for the BASE-R PHY (refer to 45.2.1.90 register bit 1.171.0). When FEC_Enable variable bit is set to a one, this enables the FEC for the BASE-R PHY. When the variable is set to zero, the FEC is disabled in the BASE-R PHY. This variable shall be set to zero upon execution of PHY reset. When the FEC function is disabled, the PHY shall have a mechanism to bypass the FEC Encode and Decode functions so as not to cause additional latency associated with encoding or decoding functions.

100GBASE-KR4 FEC Options





Why FEC Should not be Optional?

- Backplane proposed new objective (for NRZ PHY):
  - Define a 4 lane PHY for operation over a printed circuit board backplane with a total channel insertion loss of **<= 35 dB at 12.9 GHz**
  - Simulation data has shown that **FEC is required to meet this proposed loss objective***
- 30dB loss budget for the 5m copper cable links difficult to close
  - Only 4.7dB allocated to each Tx/Rx host cards
- Proposed FEC amenable for a mandatory implementation
  - 0% speed overhead, Low power/area for substantial SNR boost (close to 5dB effective SNR gain), Low latency when enabled (~94ns or better)
- FEC can be bypassed or disabled if deemed not necessary (lower loss channel, lower Xtalk, lower ILD, etc…)
- FEC increases robustness of the systems, and can lower their cost

*beukema_01_1111.ppt