

Two Backplane Markets,  
Two Backplane Channels,  
Two Signaling Schemes,  
Two PHYs

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IEEE 802.3bj 100Gb/s Backplane and Copper Cable Task Force

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# Outline

- Design Space Challenges
- Problem Statement and Solution
- PAM-2 Loss limit
- PAM-4 Loss limit
- Summary
- Proposal for new objectives
- Backup

# The Design Space Challenge

	New Backplane (based on 802.3bj)	Legacy Backplanes (based on 802.3ba)
Platform cost tolerance		
Design constraints		
Design variability		
Performance/Power Req't		

Can one 25G PHY satisfy the whole design space needed to be covered?

\* Two backplane channel represent two distinct media

Reference: nowell\_01\_0112.pdf

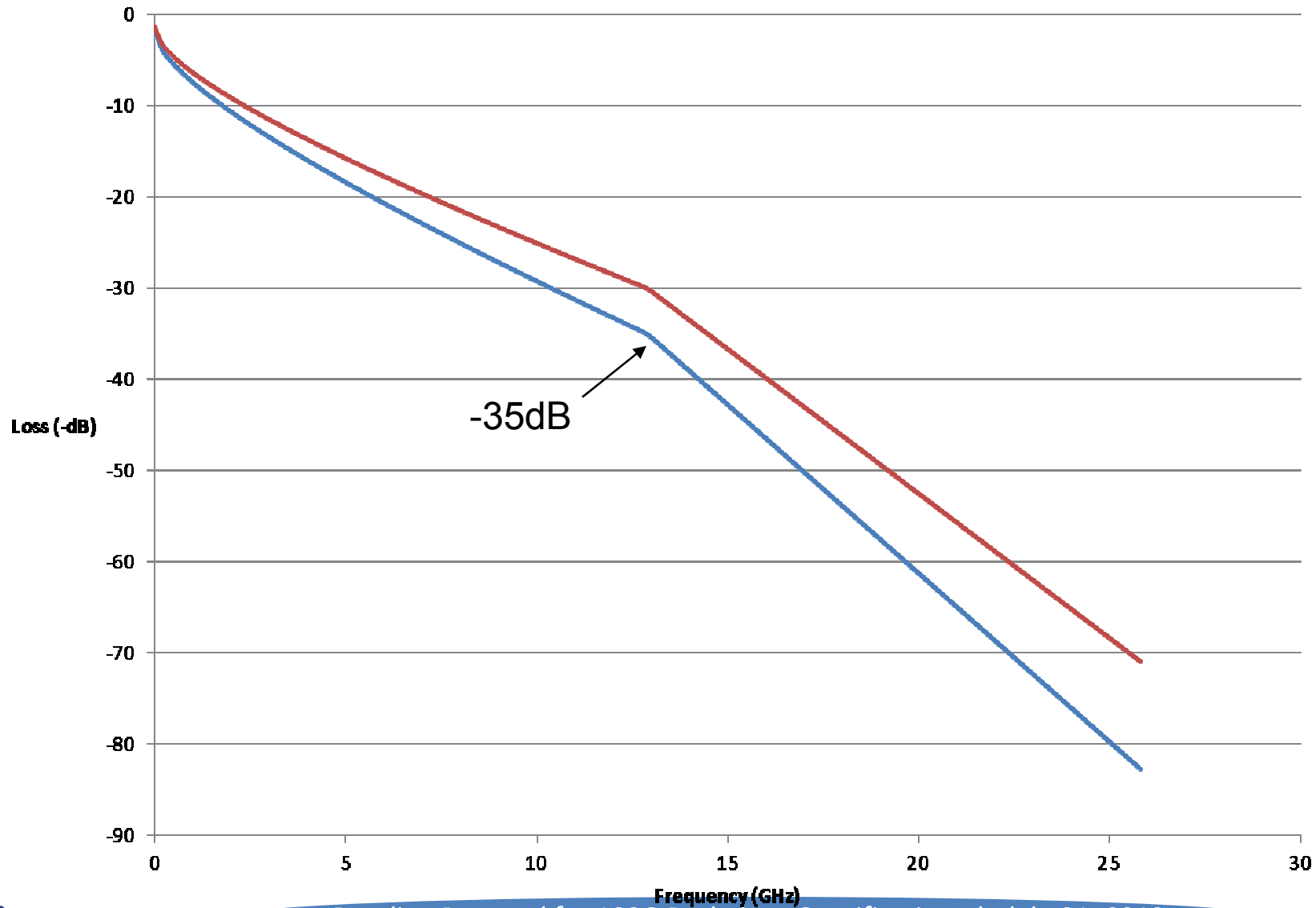
## Problem Statement and Solution

- Material presented to the SG and TF demonstrates that there are two backplane markets for 100 Gb/s Ethernet
  - High end network equipment and HPC
  - Blade server/ATCA/mid range network equipment
- In order to achieve Broad Market Potential, the standard should serve both markets.

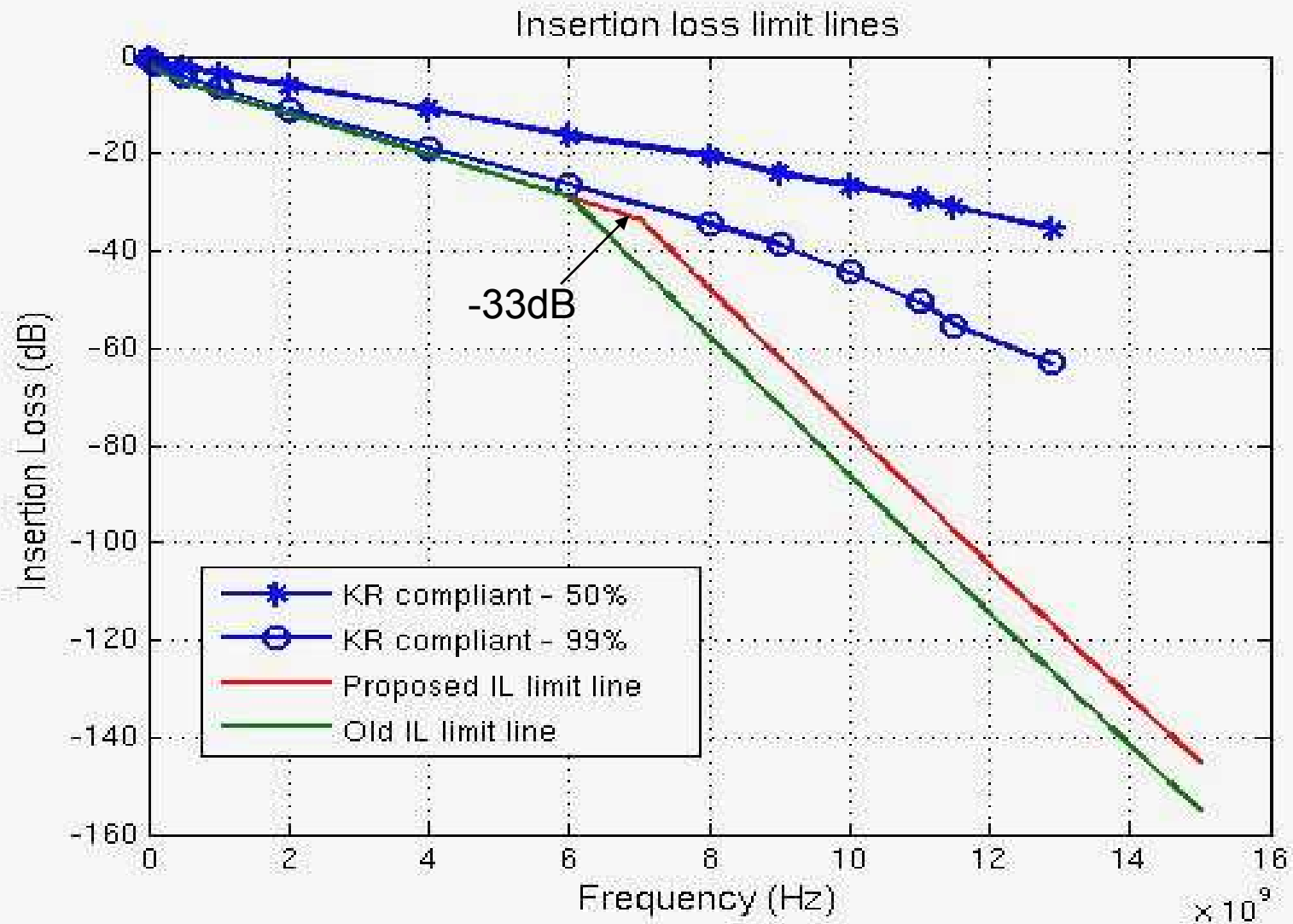
Two Signaling schemes and Two Phys could serve both markets

# PAM2 Proposed Loss Limits to 12.89 GHz

Maximum Loss



# PAM4 Proposed Loss Limits to 7.0 GHz



Reference: frazier\_01\_0112.pdf

# Baseline Proposal Presentation for PAM 2 and PAM 4 Signaling

- Mike Dudek / Mike Li – Baseline Proposal for 100G Backplane Specification Using PAM-2
- Matt Brown / Sudeep Bhoja – Baseline Proposal for 100G Backplane Specification Using PAM-4



# Summary

- Broad market potential can be achieved by two Backplane Channels, two Signaling Schemes, and two PHYs
- Two backplane channels represent two distinct media
- Previous presentations at IEEE demonstrated the feasibility of a PAM2 PHY and PAM4 PHY solution
- Two baseline proposals are ready to be voted on

# Proposed Objectives Change

- Define a 4 lane PHY for operation over a printed circuit board backplane with a total channel insertion loss of  $\leq 35$  dB at 12.9 GHz.
- Define a 4 lane PHY for operation over a printed circuit board backplane with a total channel insertion loss of  $\leq 33$  dB at 7.0 GHz

Note: Interoperability between the two PHYS is not required.

## Recommended Motion -1

Replace the existing backplane PHY objective:

Define a 4-lane 100 Gb/s backplane PHY for operation over links consistent with copper traces on “improved FR-4” (as defined by IEEE P802.3ap or better materials to be defined by the Task Force) with lengths up to at least 1m.

To the following two objectives:

- Define a 4 lane PHY for operation over a printed circuit board backplane with a total channel insertion loss of  $\leq 35$  dB at 12.9 GHz
- Define a 4 lane PHY for operation over a printed circuit board backplane with a total channel insertion loss of  $\leq 33$  dB at 7.0 GHz

Moved by:

Seconded by:

## Recommended Motion -2

Move that dudek\_01\_0312.pdf and brown\_01\_0312.pdf be adopted as baselines.

Backup

# PAM2 IEEE Uploaded example channels meeting BER requirement with FEC (many without FEC)

