Return loss at TP2 for 100GBASE-CR4

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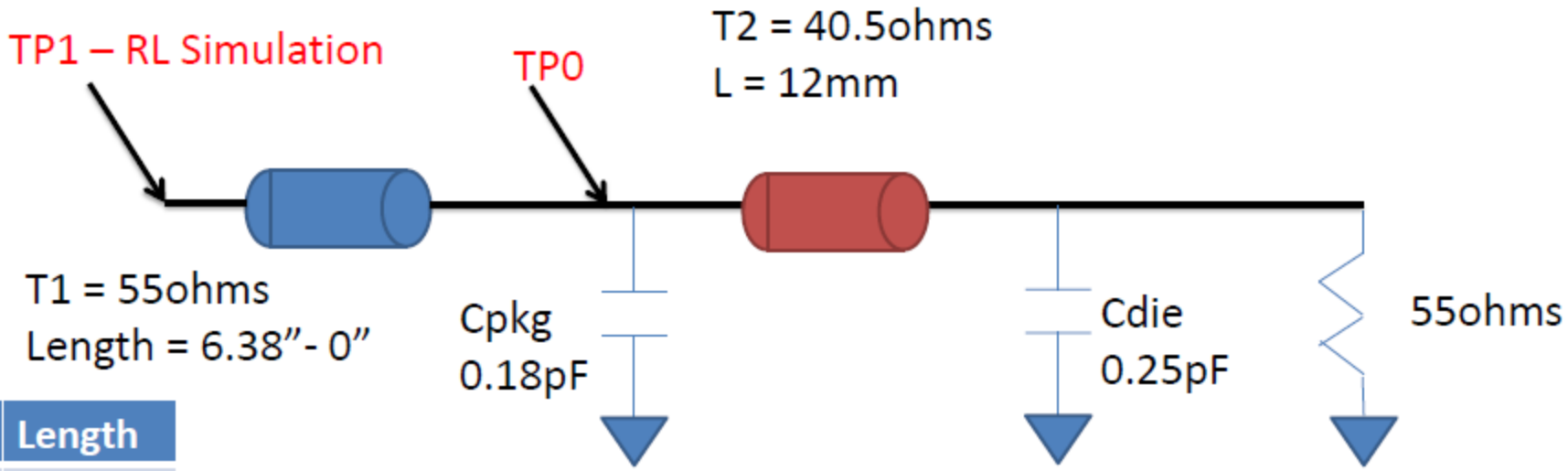
Outline

This presentation investigates the return loss specification at TP2 in 802.3bj draft 3.1 and compares it with the COM model as well as with a synthetic model. It is in support of comment r01-49

The process is as follows (1-3 already discussed during the preparation meetings, 4-5 added).

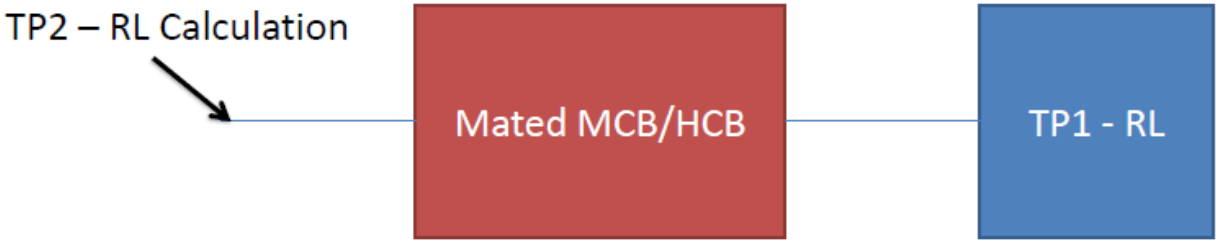
1. A representation of the COM model was used for TP0. A representative PCB Tline model was used to get from TP0 to TP1. The length of the transmission line was varied to provide losses that varied from zero to the loss used for the COM Cable calculation. This is to represent hosts with trace lengths with the same loss as the MCB (same as the recommended min loss of the host within <0.1dB at all frequencies) to the recommended max loss of the host.
2. Analytical calculations (assuming worst case addition of reflections from the mated MCB/HCB and TP1) were used to generate the return loss at TP2, which are then compared with the clause 92 specification for the return loss at TP2. Note that this assumes that the host connector has a return loss no worse than the one used on the MCB.
3. In addition S parameters from a measured MCB/HCB were concatenated to get from TP1 to TP2 and these were compared with the clause 92 specification for the return loss at TP2.
4. Additional simulations and extractions were performed to verify the conclusions and adjust the suggestion for TP2 differential return loss according to a system model that would be as close as possible to actual system while taking into account manufacturing tolerance.
5. Cross impedance simulation was done to conclude the worst case manufacturing tolerance related TP2 RL.

TP1 Simulation setup



T1 Loss	Length
6.26dB	6.38”
5dB	5.1”
4dB	4.08”
3dB	3.05”
2dB	2.04”
1dB	1.02”
0dB	No line

TP2 Return loss derivation

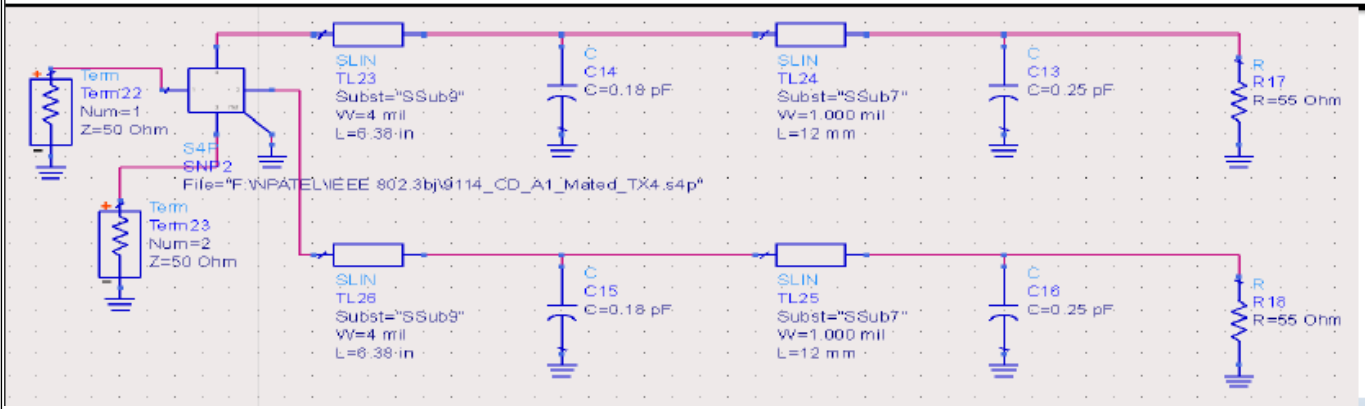


Analytic method

TP2 RL Equation

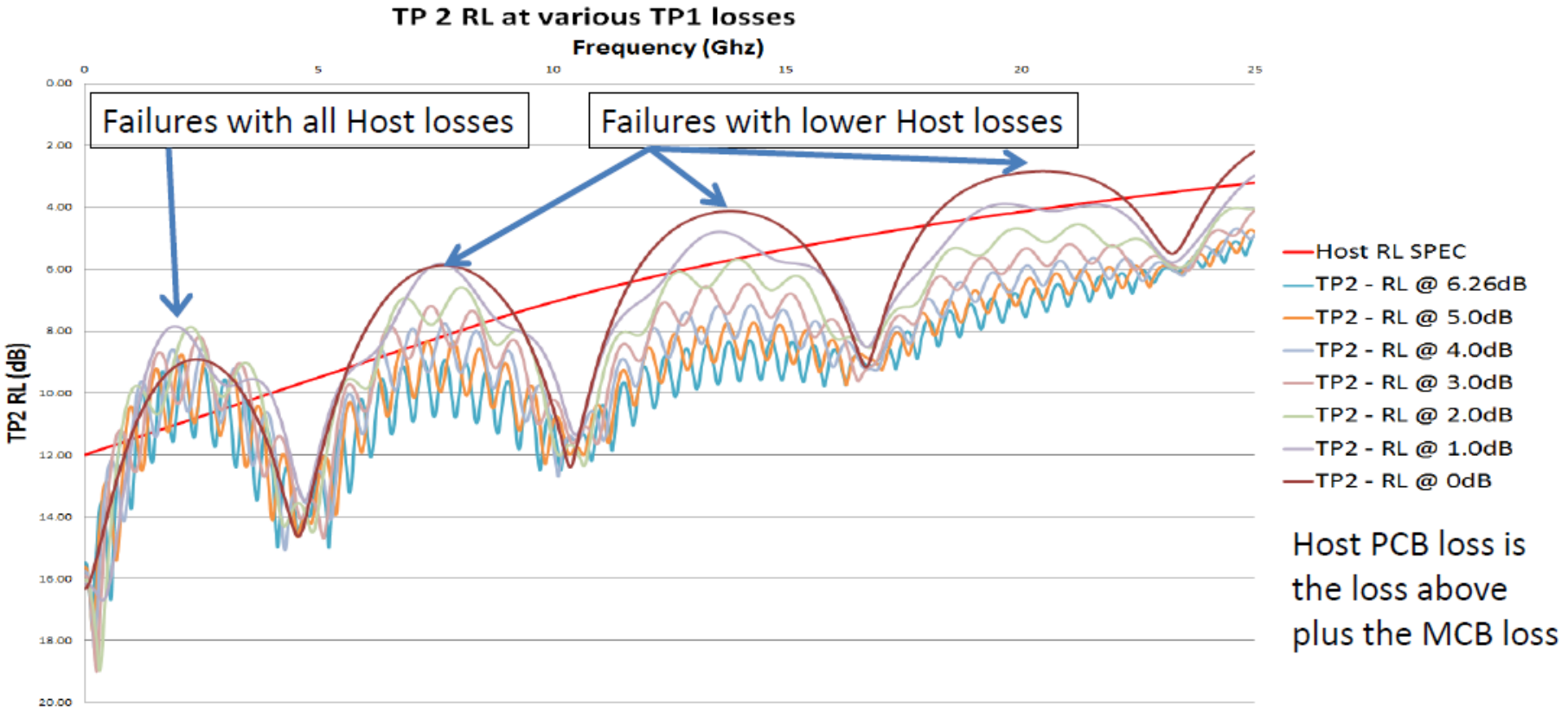
TP2 RL = -20*log10(10^(-(MCB_HCB_RL/20) + 10^(TP1_RL+2*MCB_HCB_IL) /20)

RL – Return Loss
IL - Insertion Loss



Method 2
Simulation using mated MCB/HCB measured S Parameters

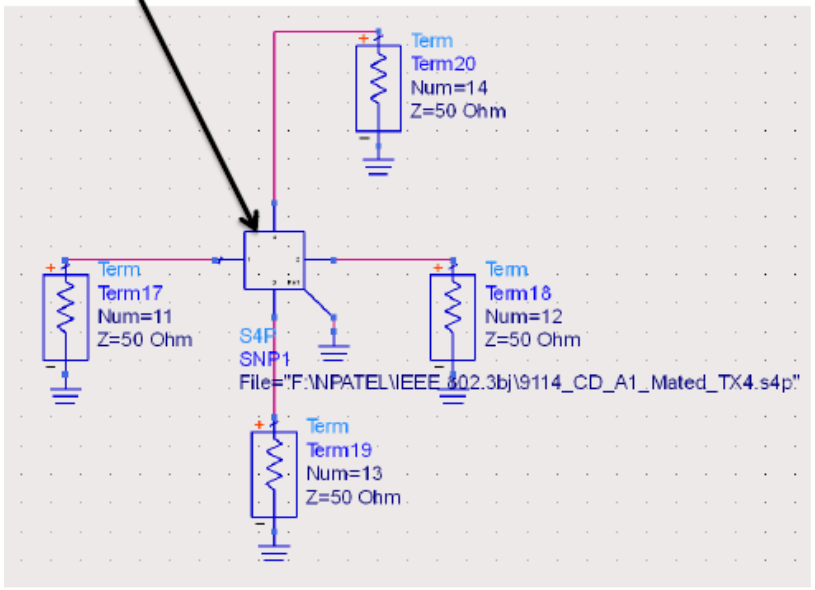
TP2 Return Loss – Analytic Method



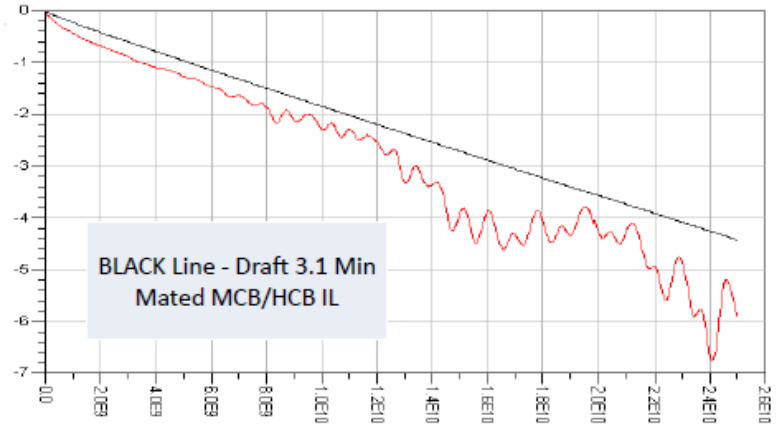
Host PCB loss is the loss above plus the MCB loss

Mated MCB/HCB S-parameter file

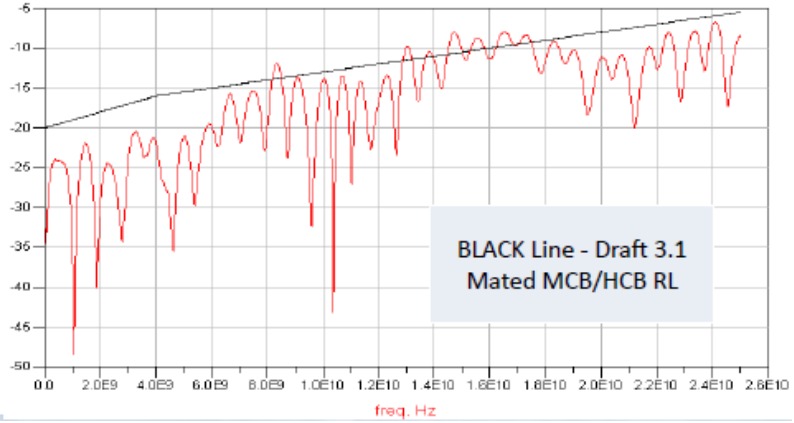
Mated MCB/HCB S-prameter file from C. Diminico. Note that it is expected that the out of spec return loss will be corrected with changes to the MCB



Insertion Loss dB



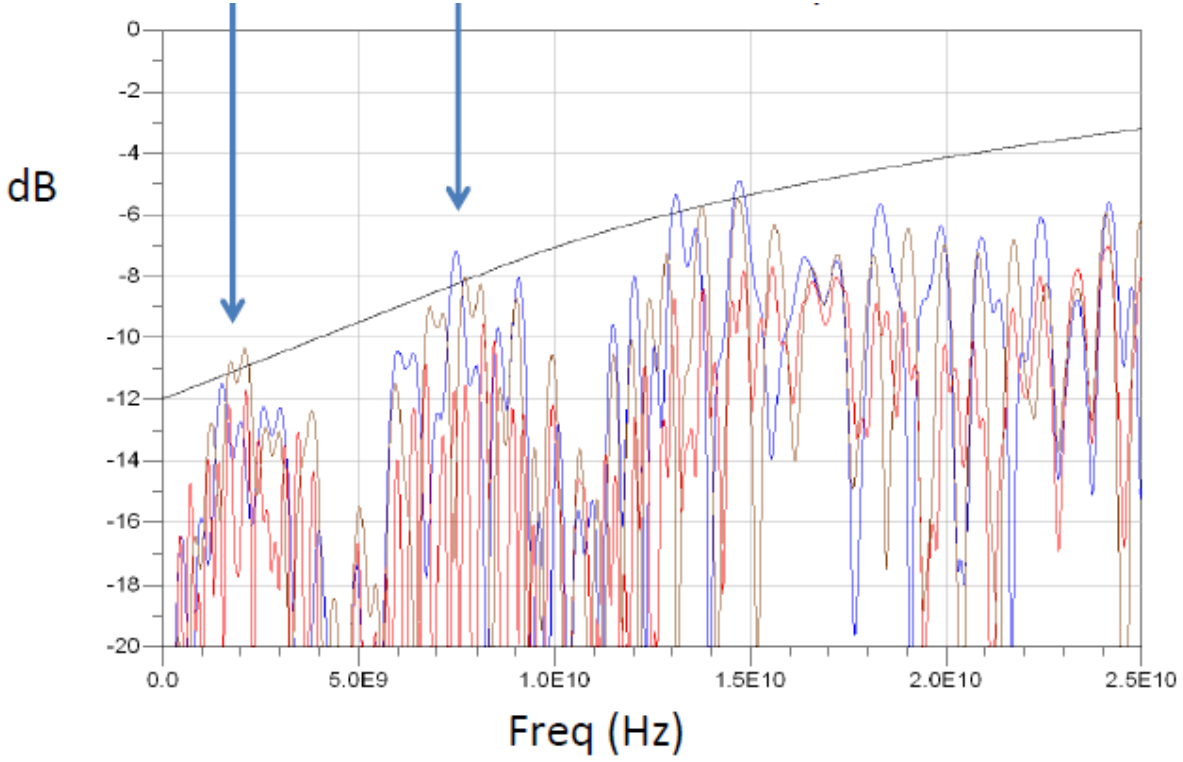
Return Loss dB



TP2 Return Loss – Method 2 (measured MCB/HCB)

- Fails spec at these frequencies even though HCB/MCB is in spec at these frequencies

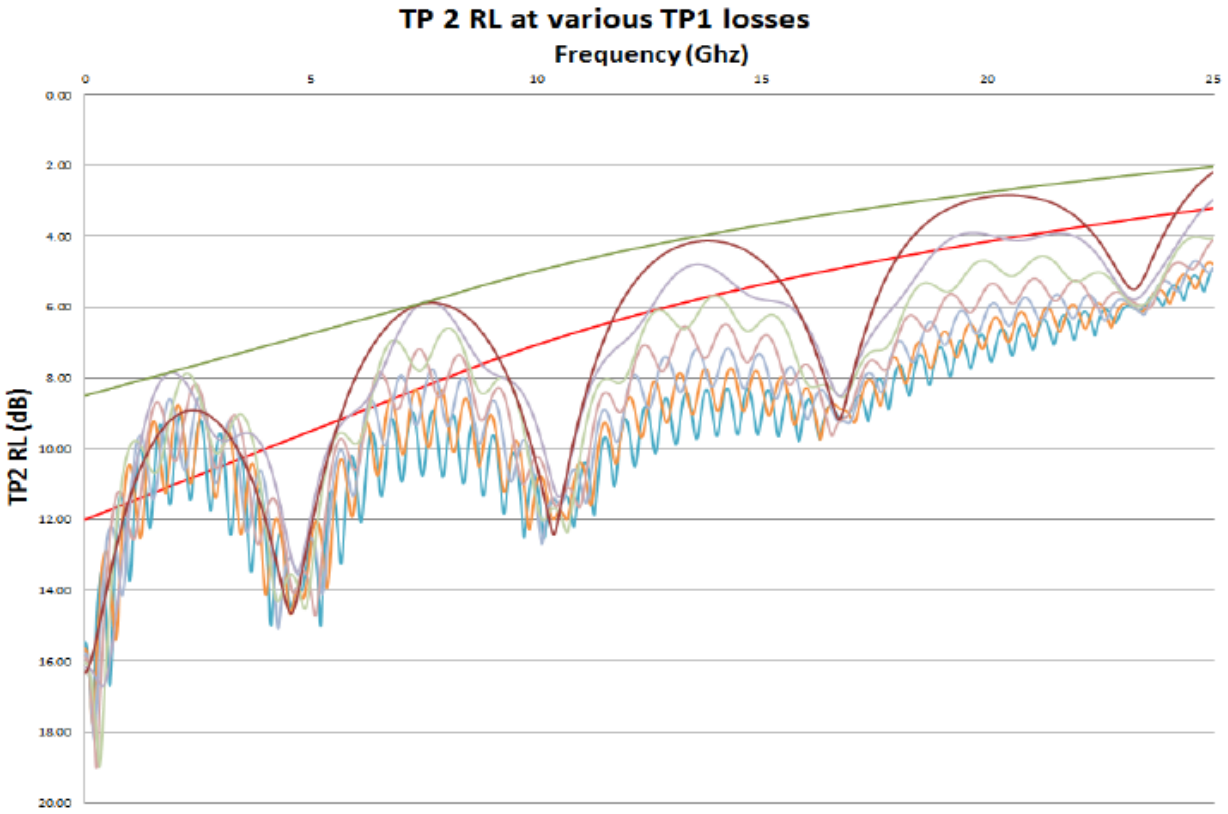
Also note that the HCB is above 100 Ohm impedance whereas lower impedance would be worst case.



Black – Host RL Spec
Red – TP2 RL @ 6.26dB
Brown – TP2 RL @ 1dB
Blue – TP2 RL @ 0dB

Host PCB loss is the loss above plus the MCB loss

TP2 Return Loss – First Analytic Method



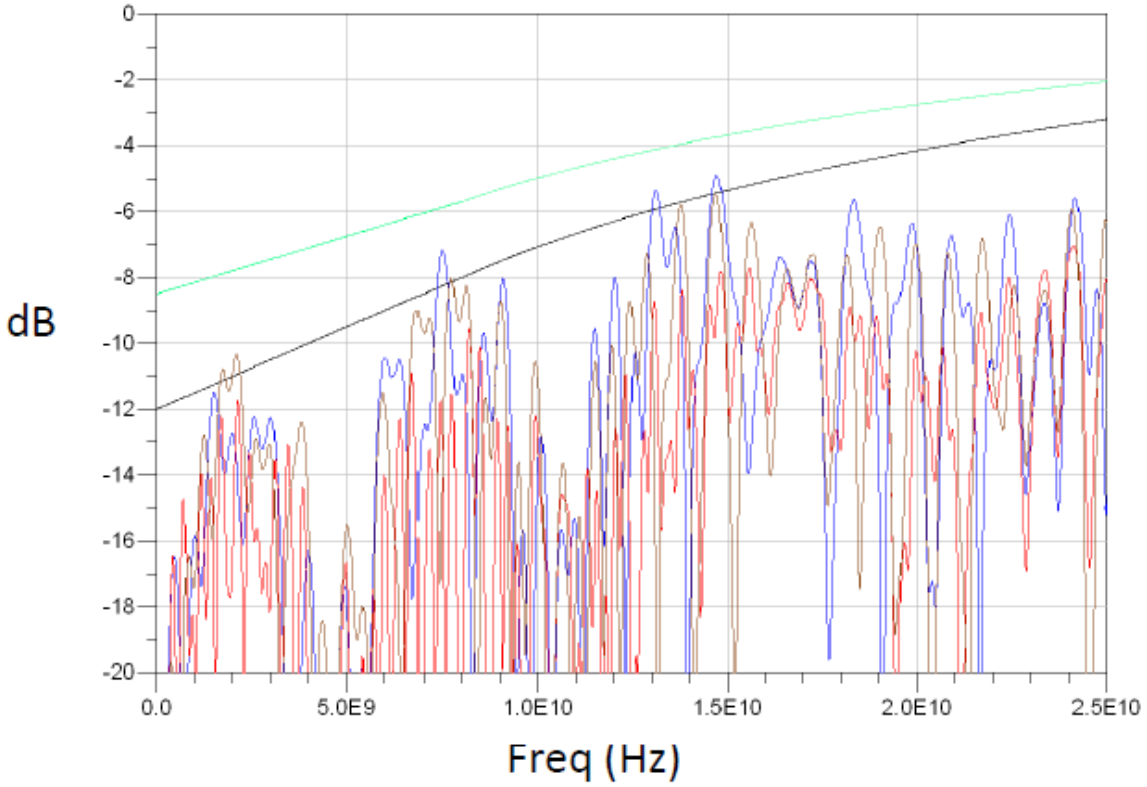
- Host RL SPEC
- TP2 - RL @ 6.26dB
- TP2 - RL @ 5.0dB
- TP2 - RL @ 4.0dB
- TP2 - RL @ 3.0dB
- TP2 - RL @ 2.0dB
- TP2 - RL @ 1.0dB
- TP2 - RL @ 0dB
- Proposed Host RL SPEC

Host PCB loss is this loss plus the MCB loss

$8.5 - 0.35 \times f$ $\quad 0.01 \le f \le 8$

$3.9 - 7.4 \times \log_{10}(f/14)$ $\quad 8 < f \le 19$

TP2 Return Loss – Method 2



Black – Host RL Spec

Red – TP2 RL @ 6.26dB + MCB

Brown – TP2 RL @ 1dB +MCB

Blue – TP2 RL @ 0dB+MCB

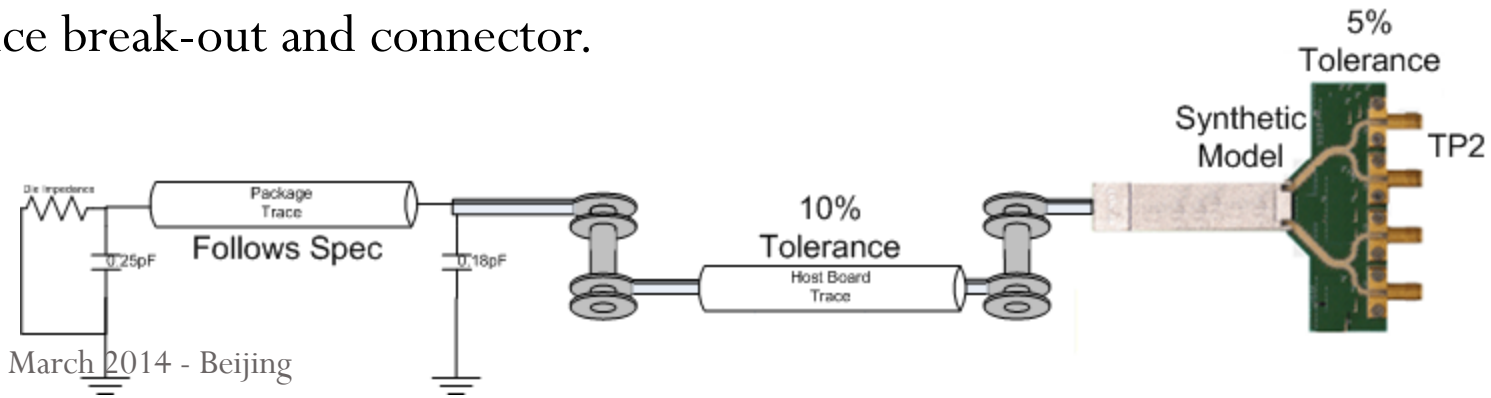
Green – Proposed RL Spec

$8.5 - 0.35 \times f$ $\quad 0.01 \le f \le 8$

$3.9 - 7.4 \times \log_{10}(f/14)$ $\quad 8 < f \le 19$

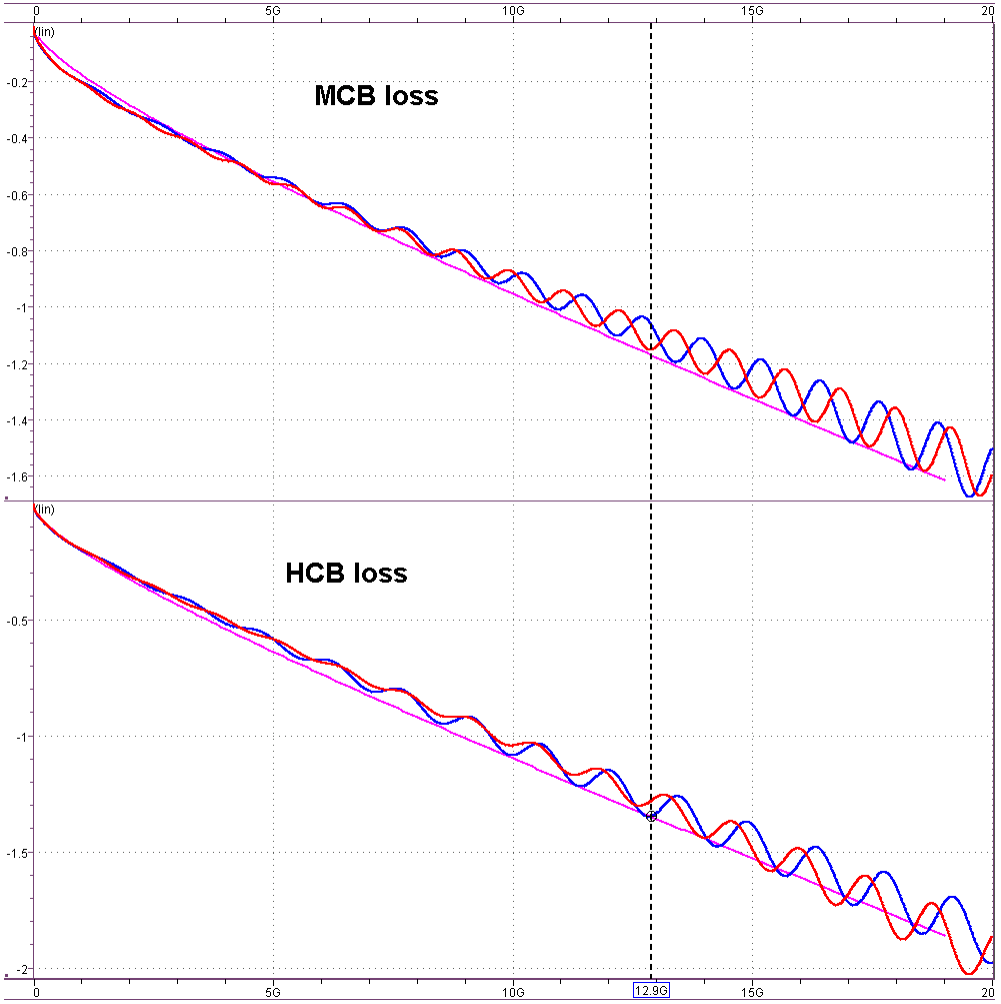
System Model Assumptions – Method #3

- The following assumptions were taken:
  - Package model follows the actual 12 mm package based on the S-parameters used to create the draft 3.1 package model + discontinuities.
  - Host board nominal impedance is 100Ω ±10% (standard manufacturing tolerance)
  - HCB and MCB nominal impedance is 100Ω±5% (justification on slide #12)
  - Low host board loss will result in worst case return loss @TP2 and therefore a 3dB (in backup slides)/1.7dB loss cases were taken (Loss from TP0 to the connector inclusive).
  - Optimized via structures were included in the analysis (10mil stub) @ device break-out and connector.



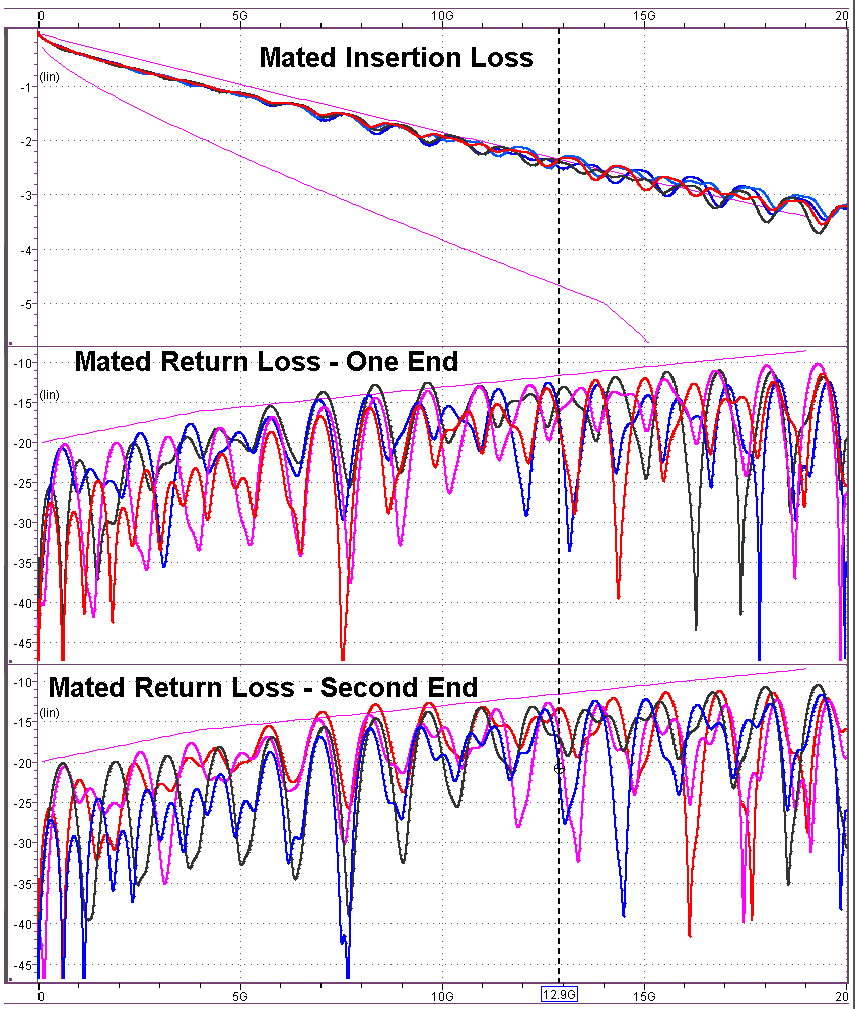
Models Used for simulation Compliance Boards

- HCB and MCB loss vs. draft 3.1



Models Used for simulation Mated Compliance Boards

- Mated HCB and MCB Including ±5% impedance manufacturing tolerance (Well justified by the Mated RL result).
- Loss is at the minimum allowed ➔ WC influence on TP2 ret loss.
- Return loss is at the limit, or even with minor violations. ➔ WC influence on TP2 ret loss.
- Both conditions above aimed at finding the worst case RL.
- The above justifies that the TP2 suggested RL to be presented on slide #14 is met in worst case conditions provided the host connector is no worse return loss than the MCB connector.



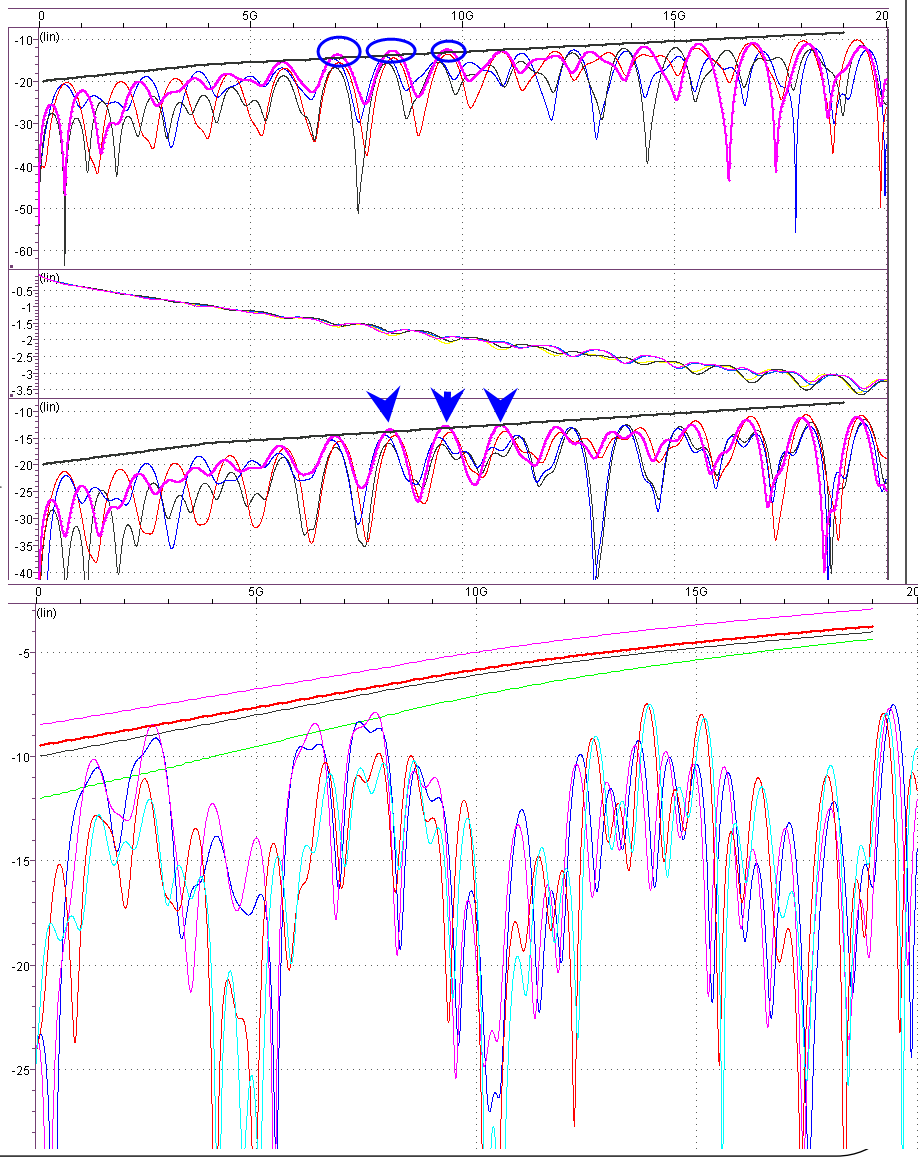
Examining Extreme Low Host Board Loss

- MCB specification is ~1.2dB @ Nyquist, but MCB, unlike host boards is extremely synthetic and clean.
- Host boards will (the least) have:
  - Additional vias (at device break-out and close to the connector)
  - Higher trace loss.
- Examining an optimized via structure (Meg6) indicates a loss of ~0.25dB @ Nyquist
- Though further loss may be introduced by ILD (due to vias matching to the trace) let's assume that after concatenating the vias the resulting loss would be the same as an ideal mathematical loss adder ➔ the total loss was tuned to be ~**1.7dB @ Nyquist** after actually concatenating the vias and the trace.

Examining Extreme Low Host Board Loss – Cont.

- Initial analysis (The 3dB host loss case see back up) was performed with HCB/MCB tolerance that still had mated RL violations (encircled).
- A further tune to the HCB lowered the amount of violation (It is not reasonable to take margin on top of margin on top on margin… and some violation still exists in this analysis…)
- If this case is to be included a limit is suggested (Red line),
  Return loss @TP2 >

9.5 - 0.37*f	$0.01 \le f \le 8$
$4.75-7.4*LOG_{10}(f/14)$	$8 \le f \le 19$

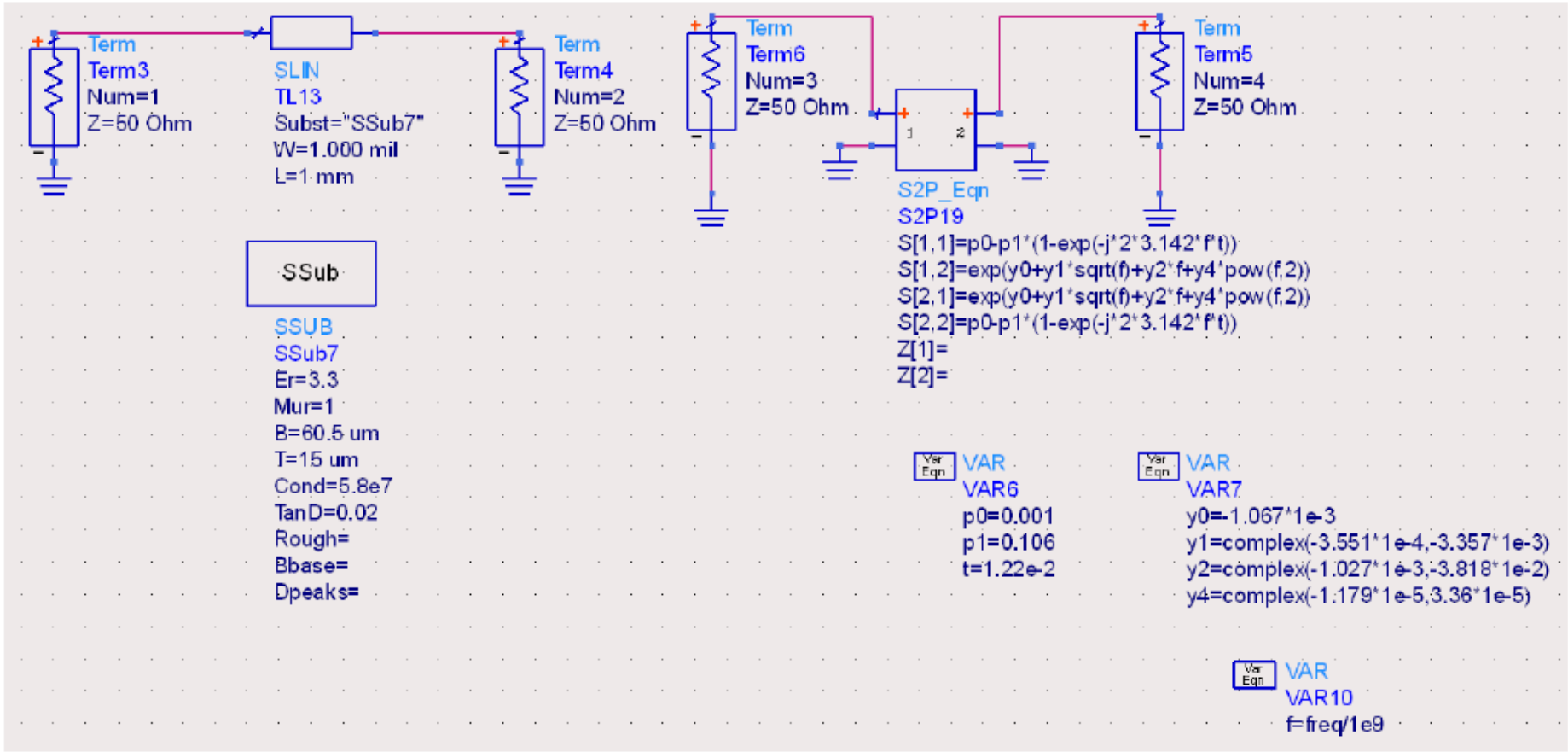


Summary, Conclusion and Suggestions

- There is an issue that with a worst case IC and host as used in the COM model for testing cables. The specification for the return loss at TP2 is not met with compliance boards that just meet their specification.
- It is expected that hosts with short traces will perform better than hosts with long traces and therefore should not be an issue. However if there are concerns with this then a cable COM test case could be created to create maximum reflections by using the short package without the TP0 to TP1 transmission line. This new test case would either be in addition to the existing two cases (short and long package with 6.2dB TP0 to TP1 loss) or could replace the existing short package test case.
- A main parameter is the amount of minimal host board loss we define as reasonable. In the analysis a 1.7dB @ Nyquist was considered based on an ideally short trace with two optimized vias.
- To account for impedance variations TP2 return loss limit should be updated. Three possible suggestions were introduced allowing a bit different minimal amount of host trace loss and assumptions.
  Suggest Using the equation from slide 14 (Red in graphs), which allows 1.7dB loss with a marginal HCB.
- Since loosening the limit is aimed at allowing low loss host boards to pass with manufacturing tolerance, but will now introduce margin to higher loss boards caution is needed.
- Editorial license granted

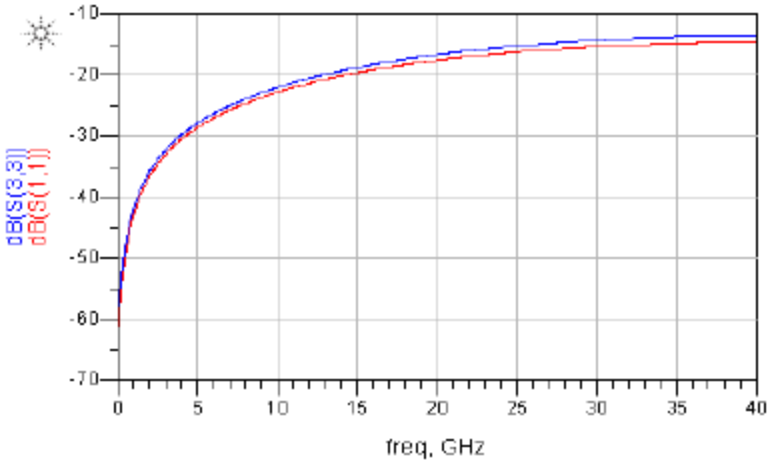
Backup

Comparing zp Tline vs S-param equations

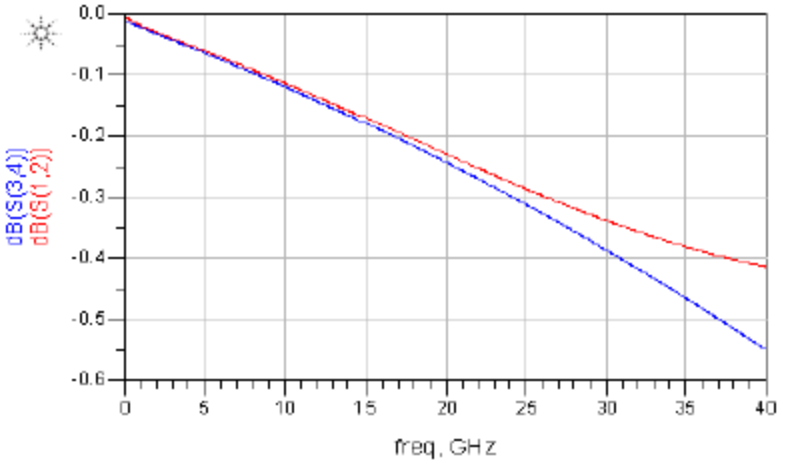


Comparing zp Tline vs S-param equations

Return Loss
L= 1mm
Red – Tline
Blue – S parameter equation

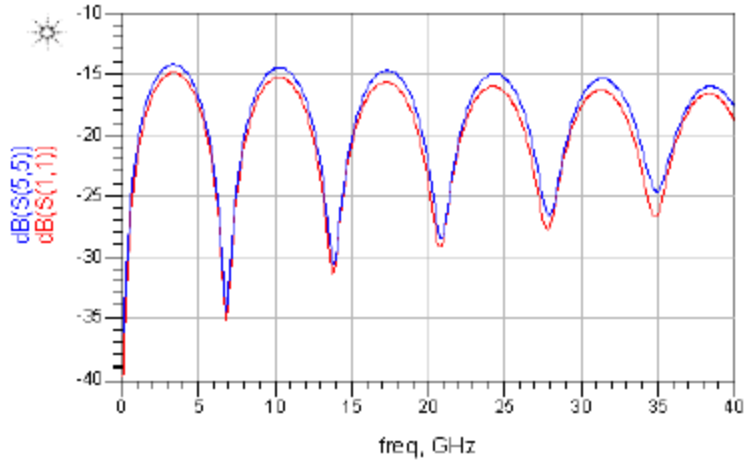


Insertion Loss
L= 1mm
Red – Tline
Blue – S parameter equation

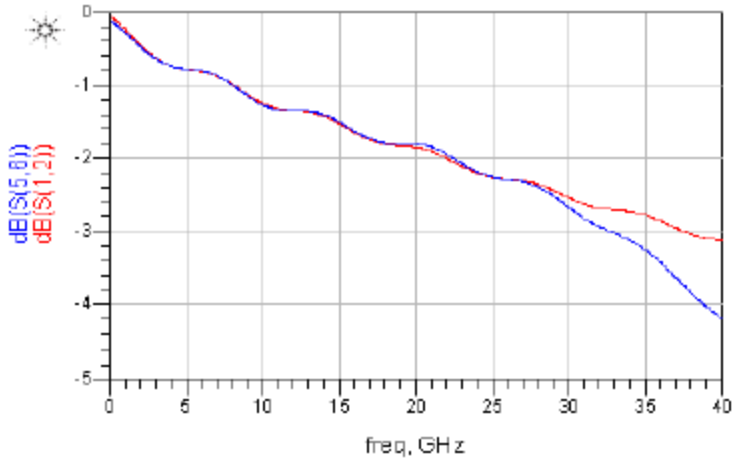


Comparing zp Tline vs S-param equations

Return Loss
L= 12mm
Red – Tline
Blue – S parameter equation



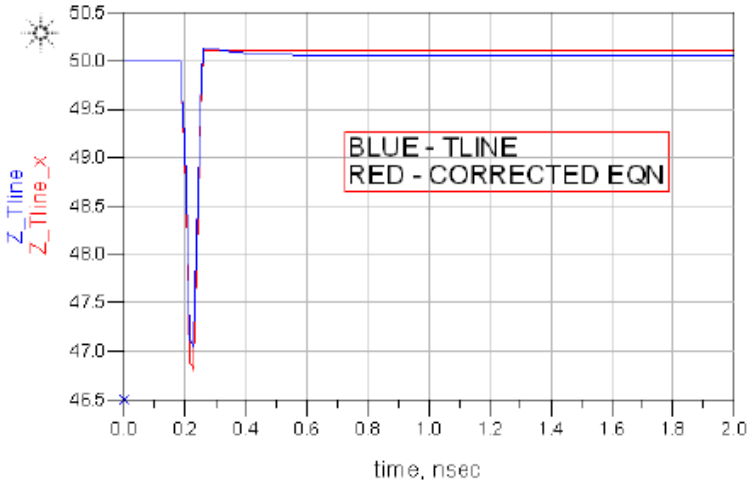
Insertion Loss
L= 12mm
Red – Tline
Blue – S parameter equation



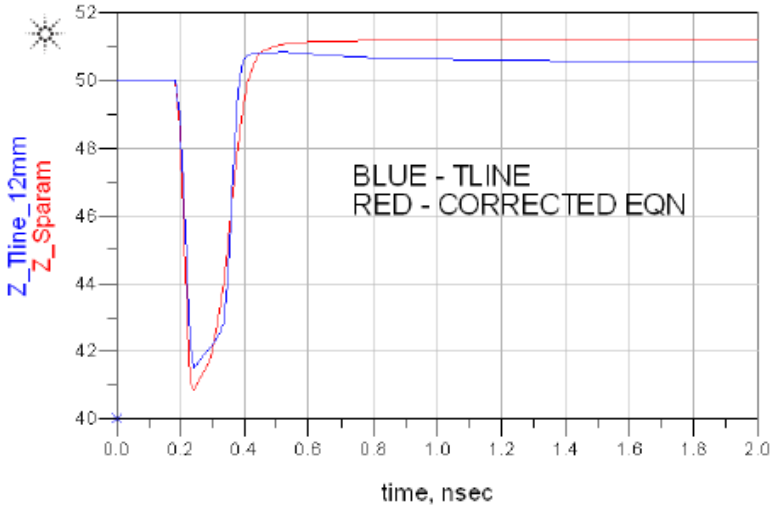
TDR Tline vs. S-param

30ps rise time

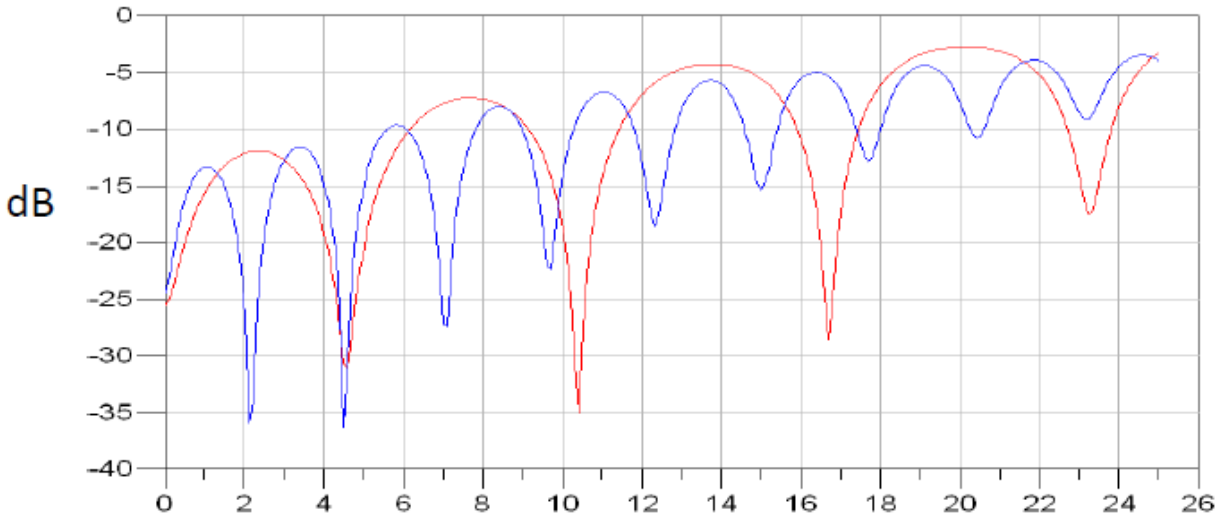
1mm



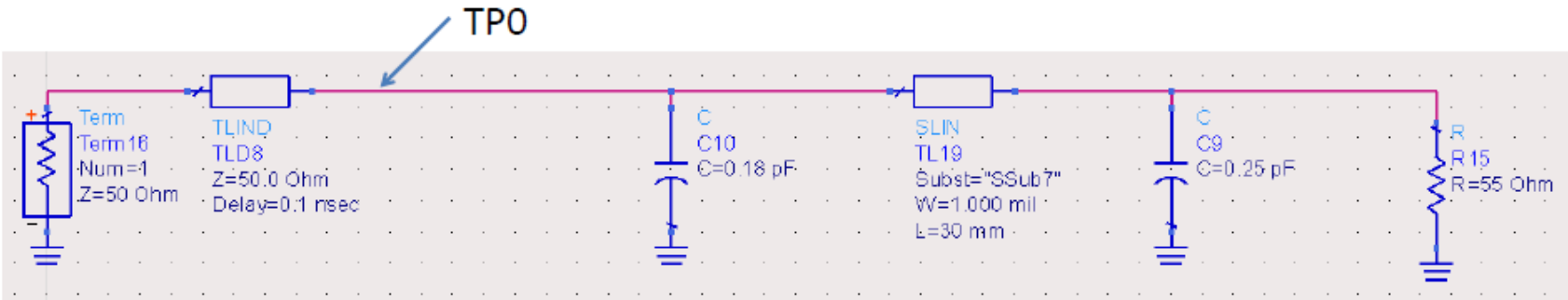
12mm



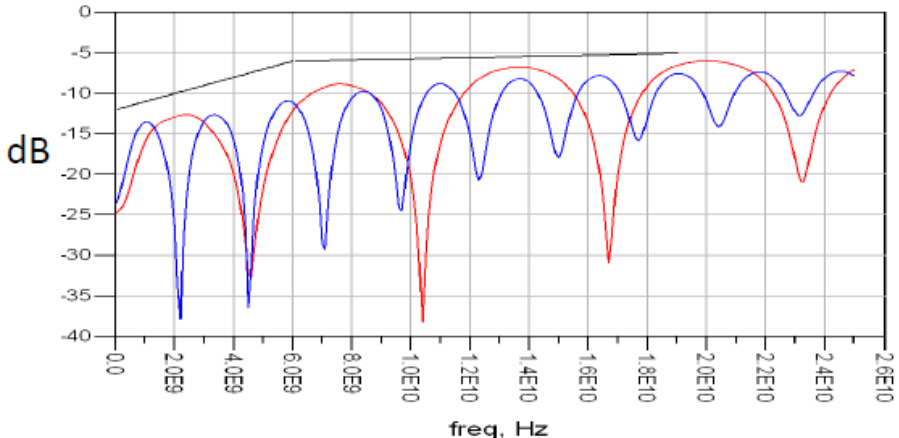
S11 – TP0 – Return loss



Red line – Return loss for 12mm
BLUE line – Return loss for 30mm



S11 – TP0a – Tline test fixture – 50ohms

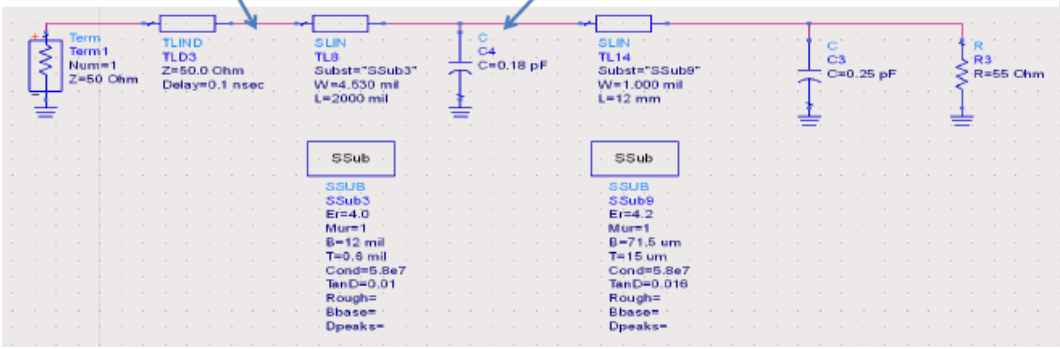


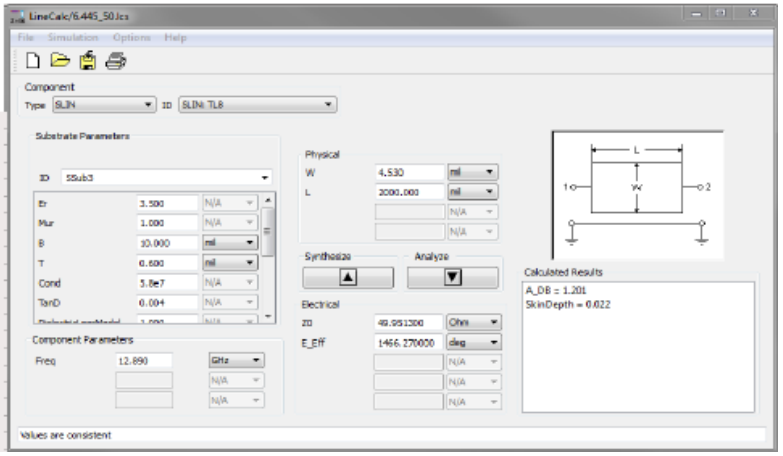
Black line - $RL_d(f) \geq \begin{cases} 12.05 - f & 0.05 \leq f \leq 6 \\ 6.5 - 0.075f & 6 < f \leq 19 \end{cases}$ dB (93–3)

Red line – Return loss for 12mm

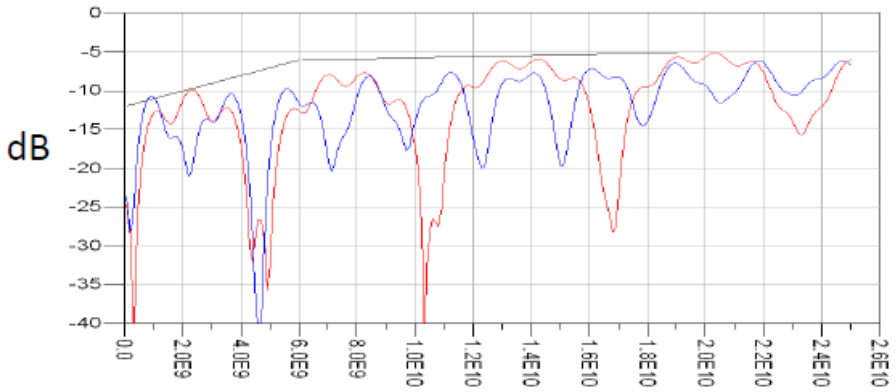
BLUE line – Return loss for 30mm

1.2dB loss at 12.89 Ghz for 2" Tline





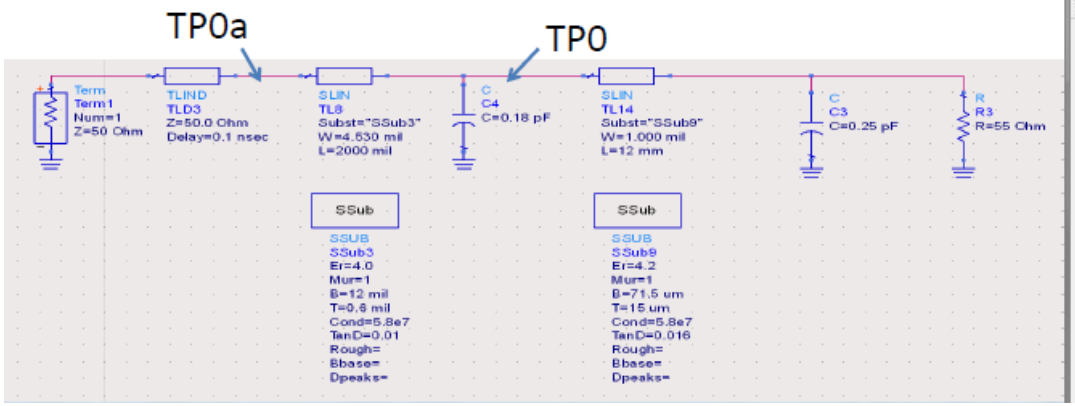
S11 – TP0a – Tline test fixture – 55ohms



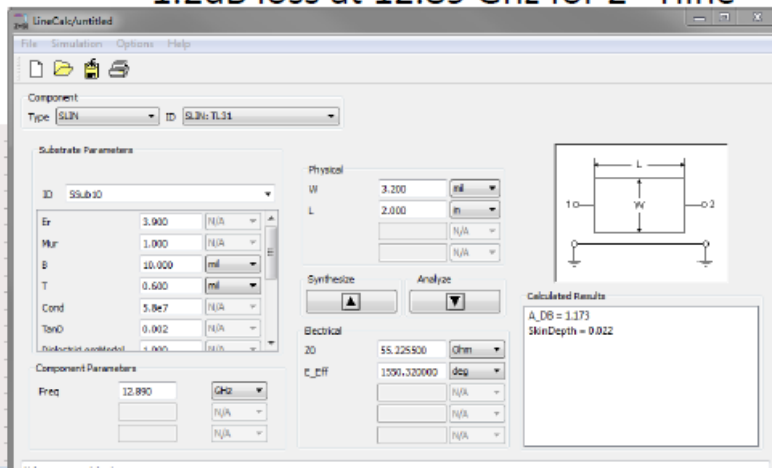
Black line - $RL_d(f) \geq \begin{Bmatrix} 12.05 - f & 0.05 \leq f \leq 6 \\ 6.5 - 0.075f & 6 < f \leq 19 \end{Bmatrix}$ dB (93–3)

Red line – Return loss for 12mm

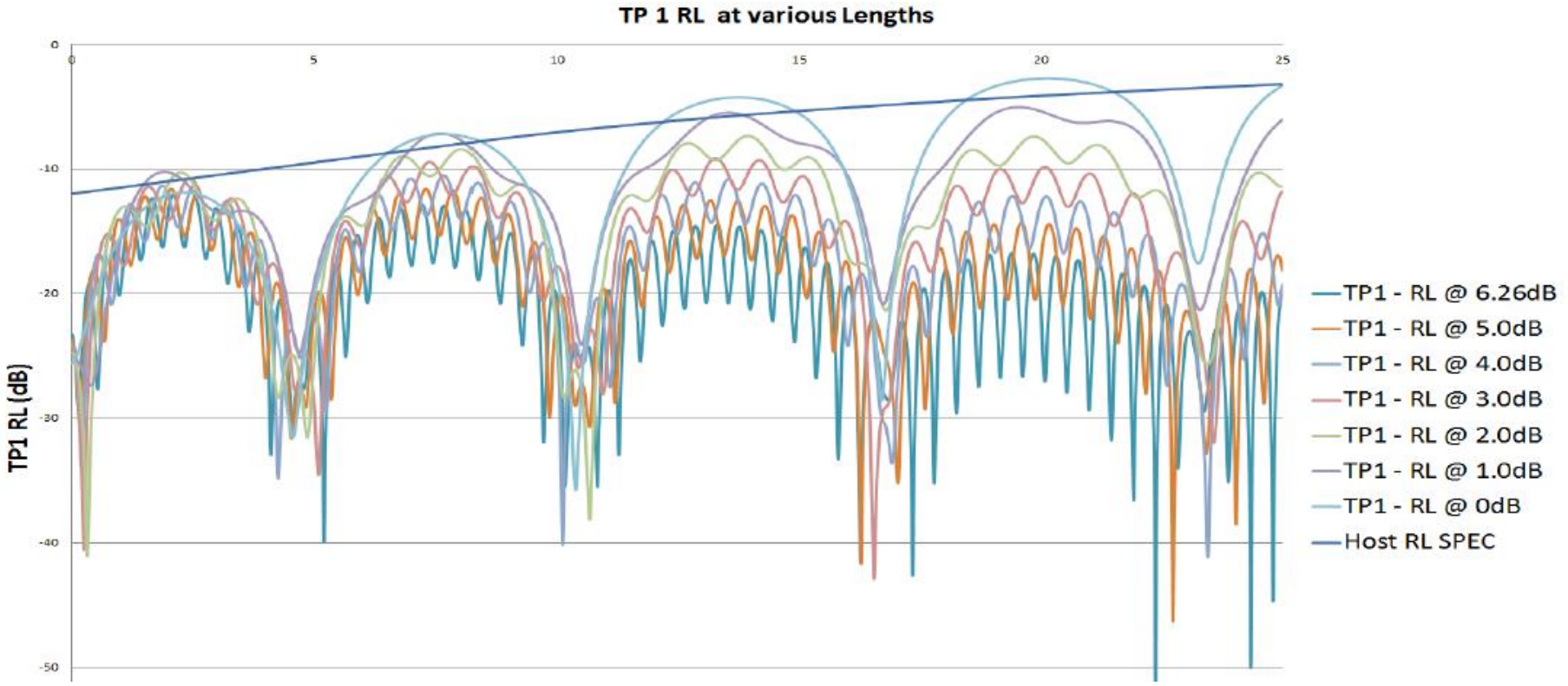
BLUE line – Return loss for 30mm



1.2dB loss at 12.89 Ghz for 2" Tline

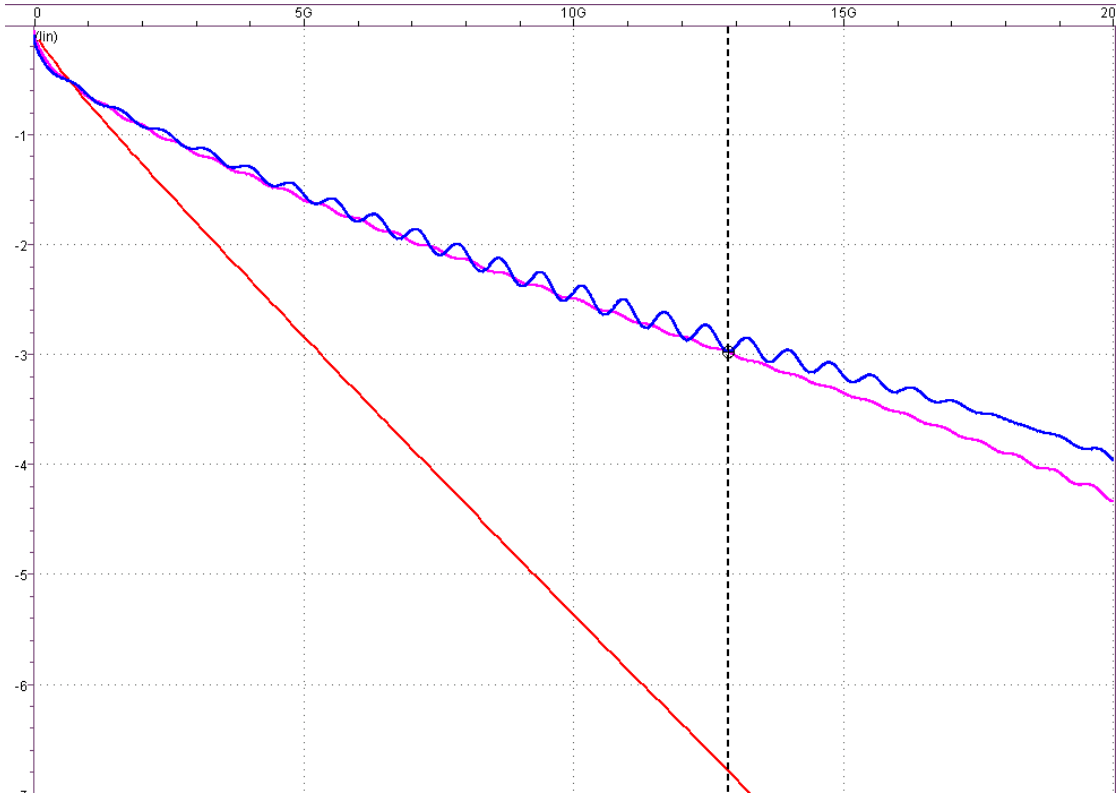


TP1 Return Loss



Models Used for simulation - Host Board - Method #3

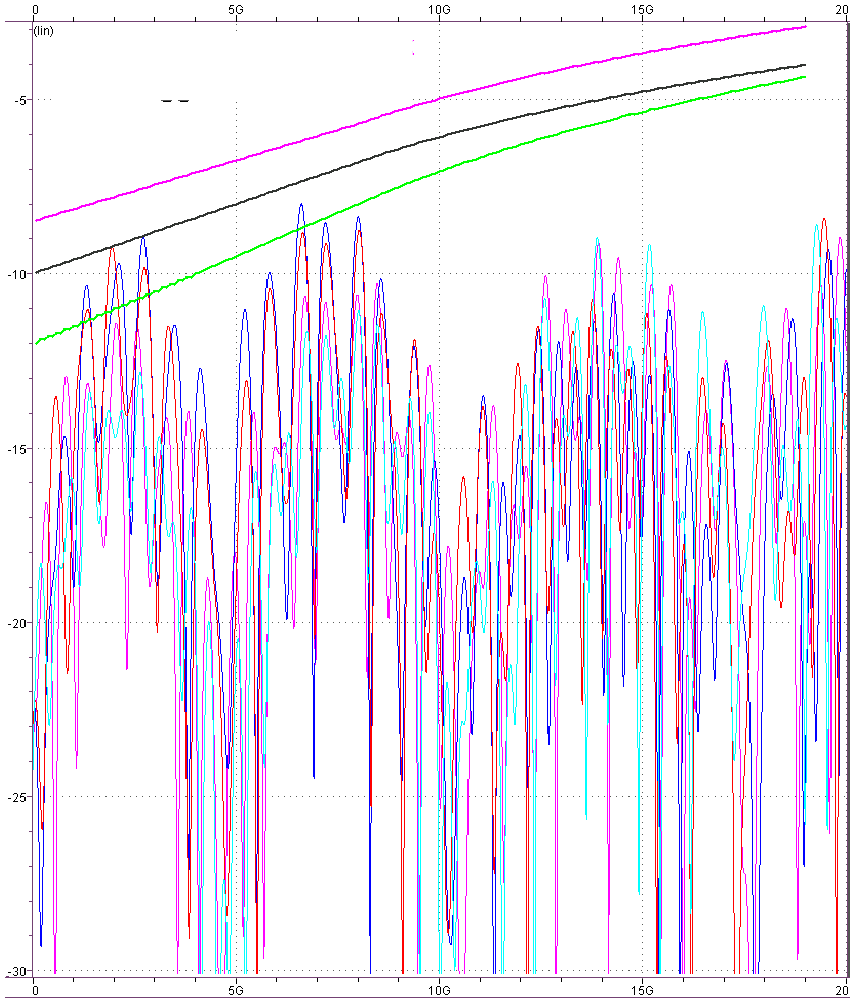
- Host board model targeted at 3dB loss (@12.89GHz) from device pads to connector.
- Optimized vias were included at the device break-out and at the connector footprint.
- 90Ω and 110Ω models.



Return loss @ TP2

- Return loss @TP2 was simulated taking into account all cross impedance variance combinations.
- Some impedance combinations fail the draft 3.1 return loss spec.
- A new limit is suggested to accommodate these cases (black line):
- Return loss @TP2 >

10 - 0.4*f	$0.01 \leq f \leq 8$
$5-7.4*LOG_{10}(f/14)$	$8 \leq f \leq 19$



None Cross impedance Cases