802.3bj Backplane Application:
AC Cap Location and Test Points

Joel Goergen (Cisco)

Beth Kochuparambil (Cisco)

IEEE 802.3bj - May 2012 Interim

Minneapolis, MN, USA

Supporters

- Rick Rabinovich – Alcatel-Lucent
- Brian Misek – Avago
- Charles Moore – Avago
- Matt Brown – AppliedMicro
- Umesh Chandra – Dell
- Bengt Kvist – Ericsson
- Yasuo Hidaka – Fujitsu
- Alex Umnov – Huawei
- Kent Lusted – Intel
- Rich Mellitz – Intel
- Liav Ben Artsi – Marvell
- Scott Irwin – MoSys
- Ed Sayre – Nesa
- Mohammad Kermani - Netapp
- Mike Dudek – Qlogic

Re“cap” of Last 2 Months

- Hosted series of calls for data collection and discussion.
- 36 individuals involved from 27 affiliations

  Adam Healey, Alex Umnov, Ali Ghiasi, Andy Zambell, Bengt Kvist, Beth Kochuparambil, Bhavesh Patel, Brian Misek, Charles Moore, Ed Sayre, Francois Tremblay, Ingvar Karlsson, Joe Pankow, Joel Goergen, John Lehman, Liav Ben Artsi, Madhumitha Rengarajan, Matt Brown, Megha Shanbhag, Merrick Moeller, Mike Dudek, Mohammad Kermani, Mounir Meghelli, Oren Sela, Pavel Zivny, Piers Dawe, Rich Mellitz, Rick Rabinovich, Ron Kennedy, Scott Irwin, Umesh Chandra, Vasu Pathasarathy, Wheling Cheng, Wolfgang Meier, Yasuo Hidaka, Ziad Hatab

- Collection of data of AC Cap impact
- Discussion of AC cap location & test points
- Some of the best work on channels shown in this effort; contributions are noteworthy!

- NOTE: Previous channels and link simulations did NOT include AC cap allocation.

Bringing Together Information…

Summary of Data from Calls

- **Location**
  - In the connector – not in massive volumes until 2013
  - On the motherboard – it won't fit in many applications
  - In the chip as electronic equivalent – tighter common mode specifications
  - In the barrel – expensive and not mass producible
  - In the board – expensive and difficult to control the process
- **Channel Testing and Verification**
  - Test systems usually bypass the blocking cap
  - 3rd party blocking is typically used to isolate the scope or bert equipment
  - Not a lot of public work has been done to define the loss budgets of the cap

- Joel Goergen (Cisco) – Discussion Points
- Review of previous test points: IEEE802.3ap & P802.3bj cabling adopted baseline

Reference P802.3ap-D33.pdf Feb21, 2007

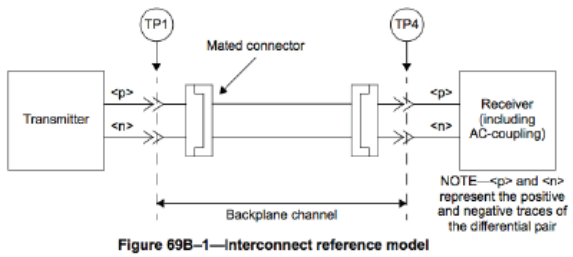

Figure 69B–1—Interconnect reference model

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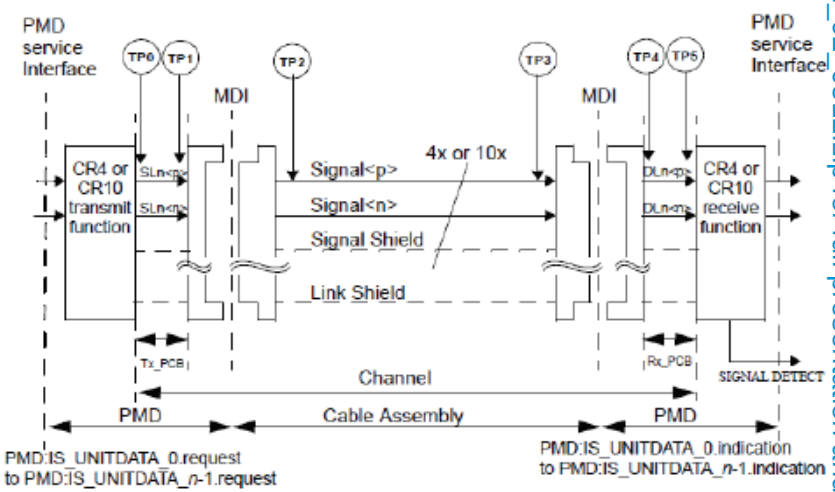


Figure 85–2—40GBASE-CR4 or 100GBASE-CR10 link (half link is illustrated)

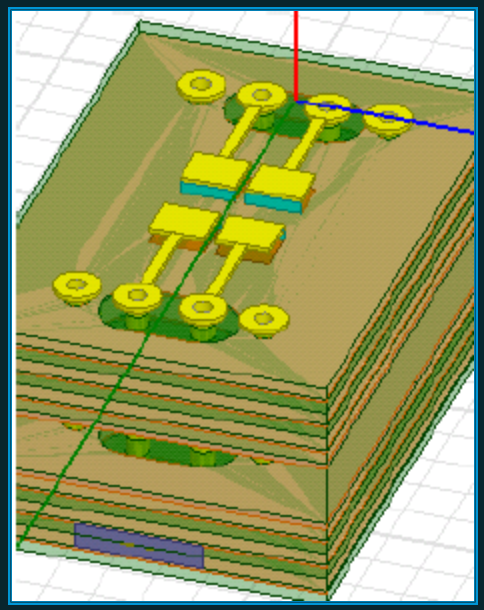
diminico_01a_0112.pdf

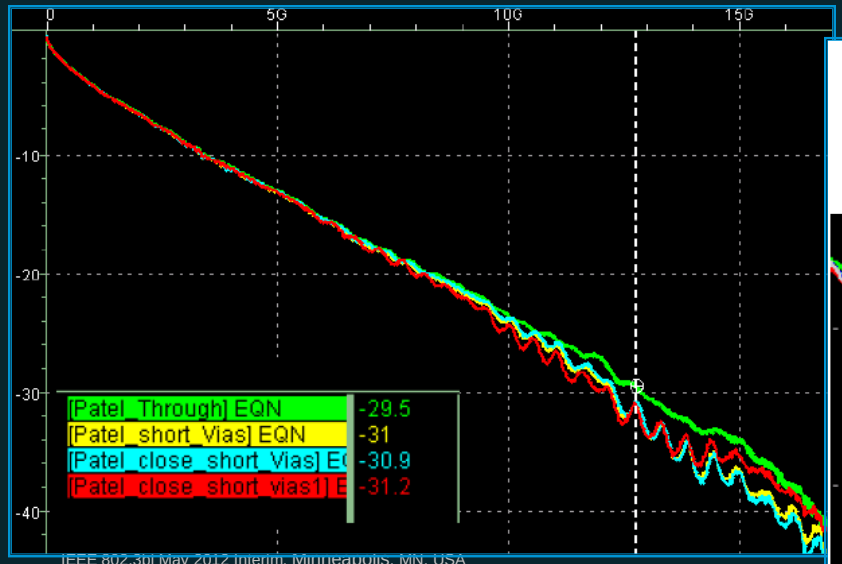
Summary/images from Joel Goergen (Cisco) See goergen_02_0512.zip for full presentation and details.

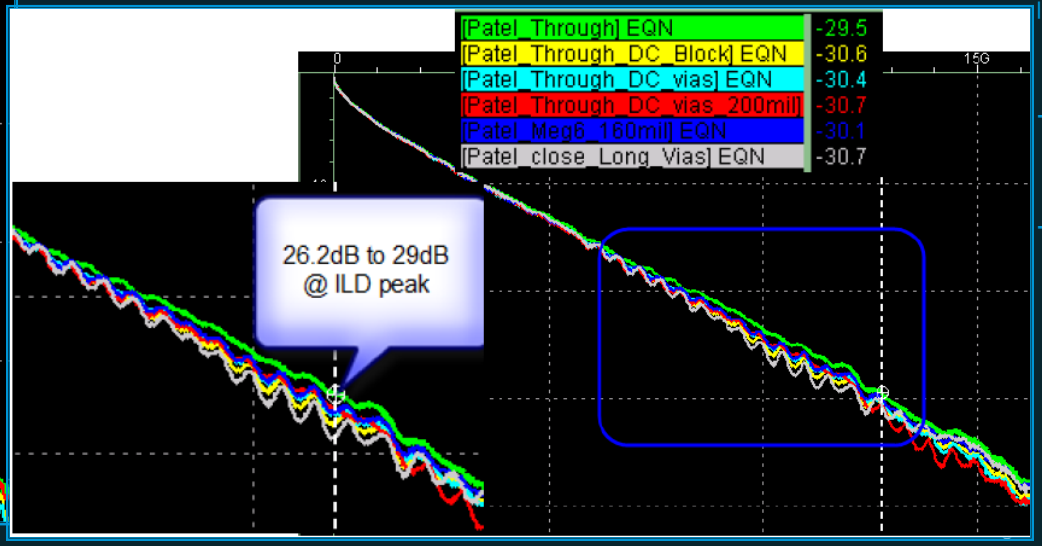
Summary of Data from Calls

- Liav Ben-Artsi (Marvell) – **Simulation**
- Link simulation cascading patel_03_0911THRU and meghelli_01_0112 w/ varied cap structures
  - 26mil via w/ 12-15mil stubs
  - 90mil via w/13mil stubs
- Cap/footprint penalty/impact:

  Up to 2.8dB extra loss at ILD peak



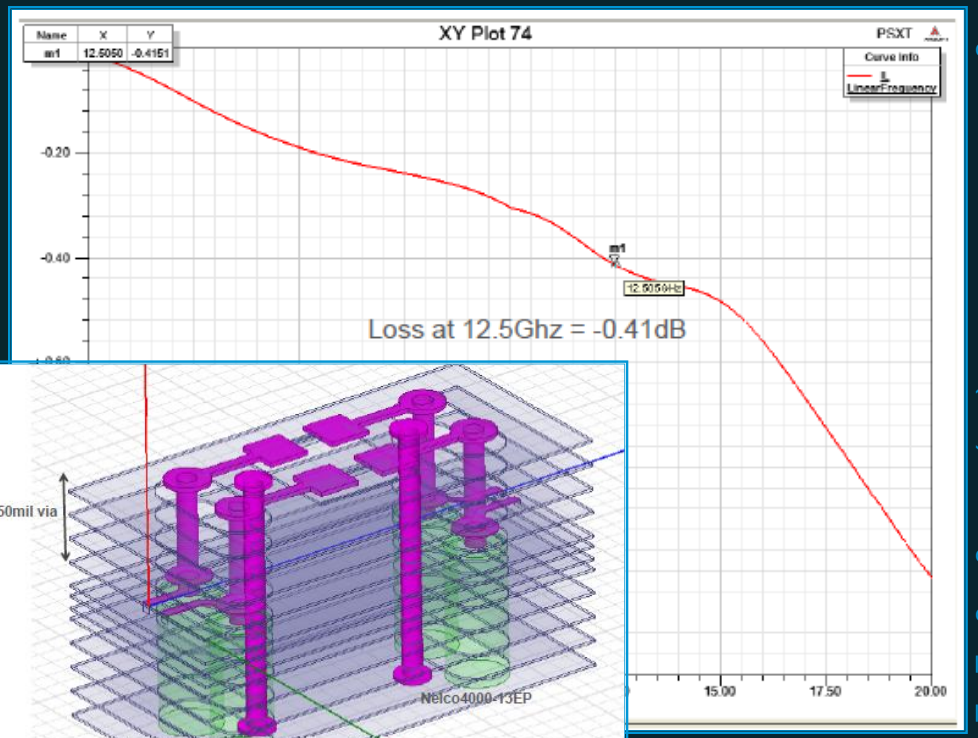


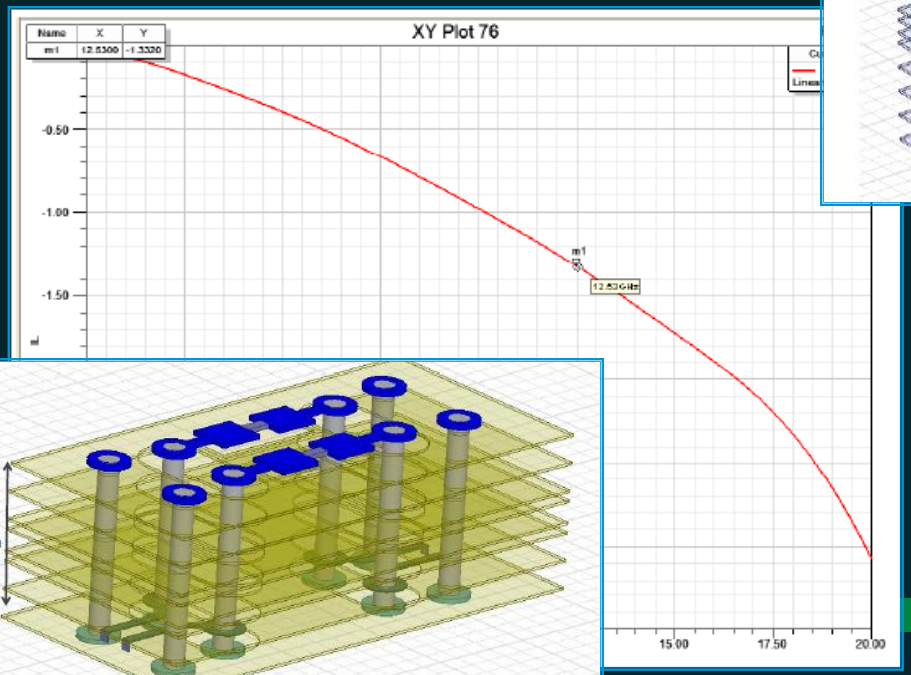


Summary/images from Liav BenArtsi (Marvell) See goergen_02_0512.zip for full presentation and details.

Summary of Data from Calls

- Umesh Chandra (Dell) – **Simulations**
- 3D simulation of only the footprint structure for various setup:
  - 50mil via w/4-8mil stub, 2 gnd vias
  - 70mil via w/15 mil stub, 4 gnd vias





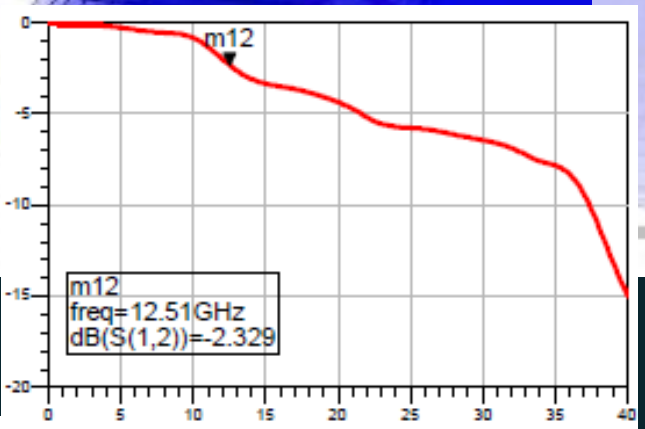
- Footprint-only penalty/impact : **0.42dB IL** (50mil via) and **1.33dB IL** (70mil via) **at 12.5G**

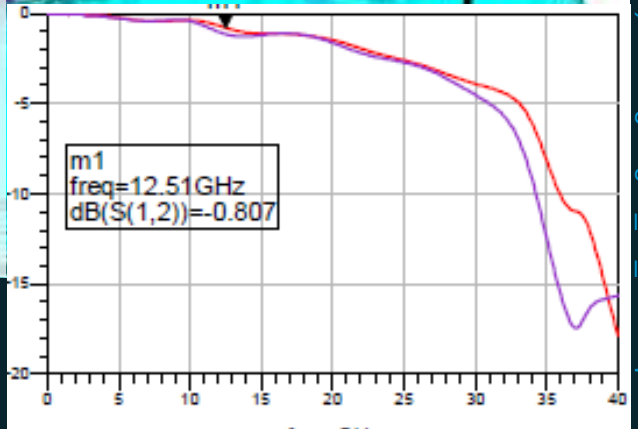
Summary/images from Umesh Chandra (Dell) See goergen_02_0512.zip for full presentation and details.

Summary of Data from Calls

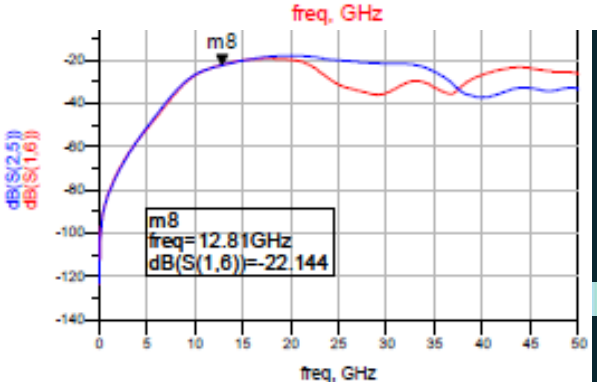
- Wheling Cheng (Juniper) – **Simulations**

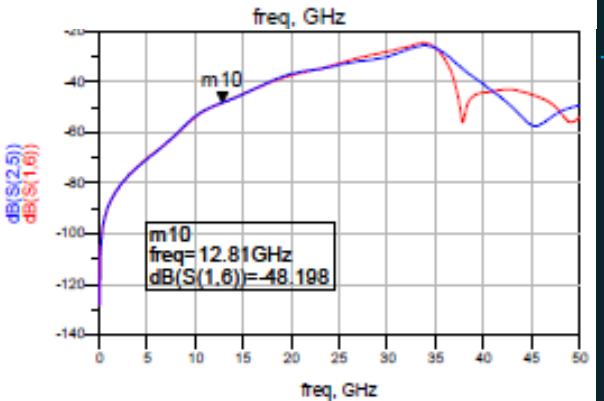
- 3D simulation of various footprint-only structures:
  - 135mil via with or without side gnd vias (both already have 2 gnd vias)





Footprint-only penalty/impact :
2.33dB IL/ ~21dB Xtalk
(↑ w/o side gnd) and (↓ w/ side gnd)
0.8dB IL/ ~48dB Xtalk.





Summary/images from Wheling Cheng (Juniper) See goergen_02_0512.zip for full presentation and details.

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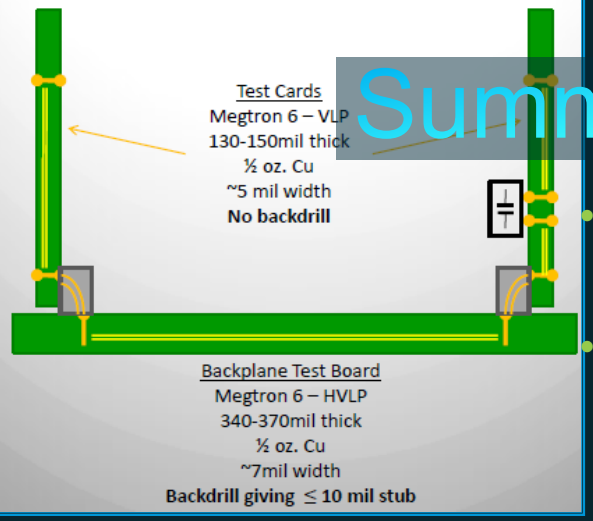
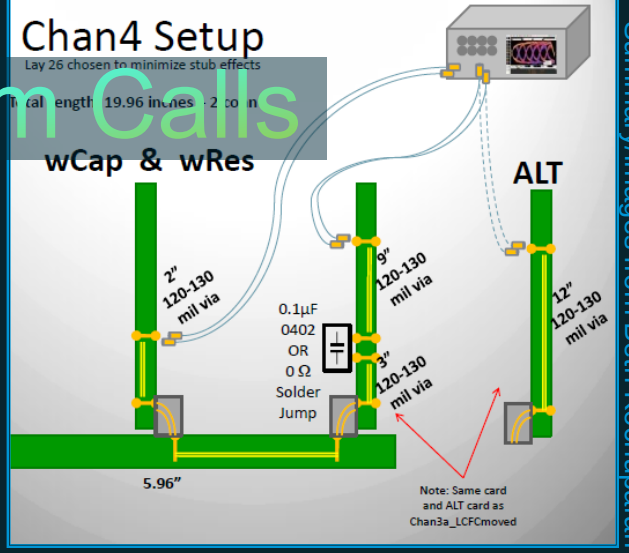
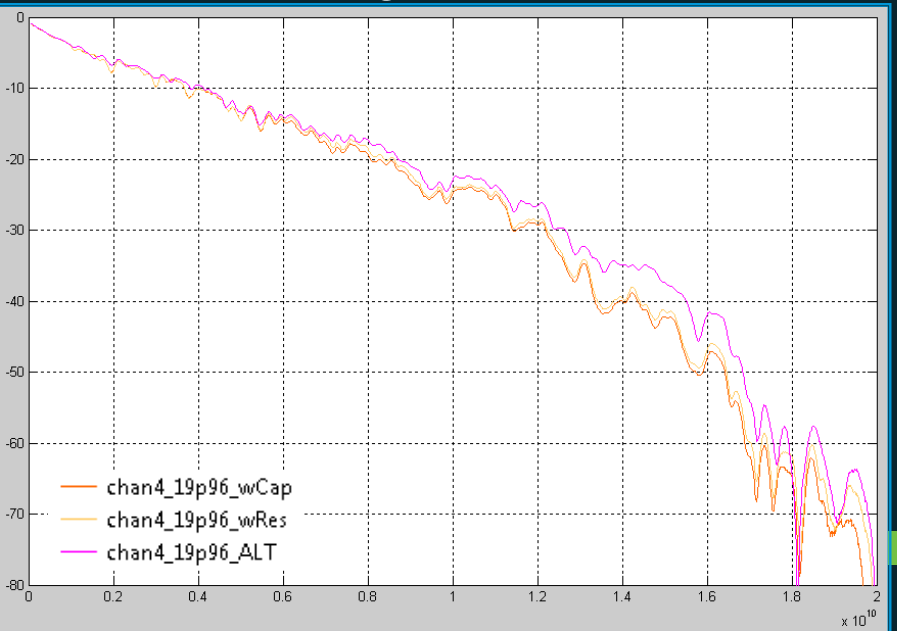
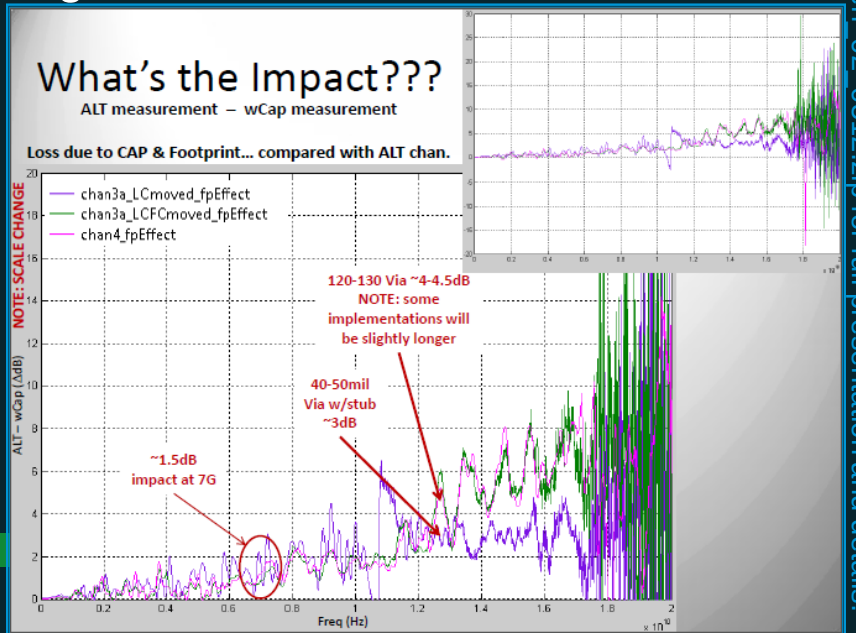




- Beth Kochuparambil (Cisco) – **Measurement**
- Measured channels with cap, without cap (solder jump), and without cap/footprint
  - 40-50mil w/long stub (no gnd via)
  - 120-130mil w/20mil stub (no gnd via)
- Cap-only penalty (solder jump→cap): **0.5-1dB IL** (@12.9G)
- Cap/footprint penalty: **~3dB or 4.5dB IL** (@12.9G)
- ILD is to be ignored due to lack of backdrilling on test cards.

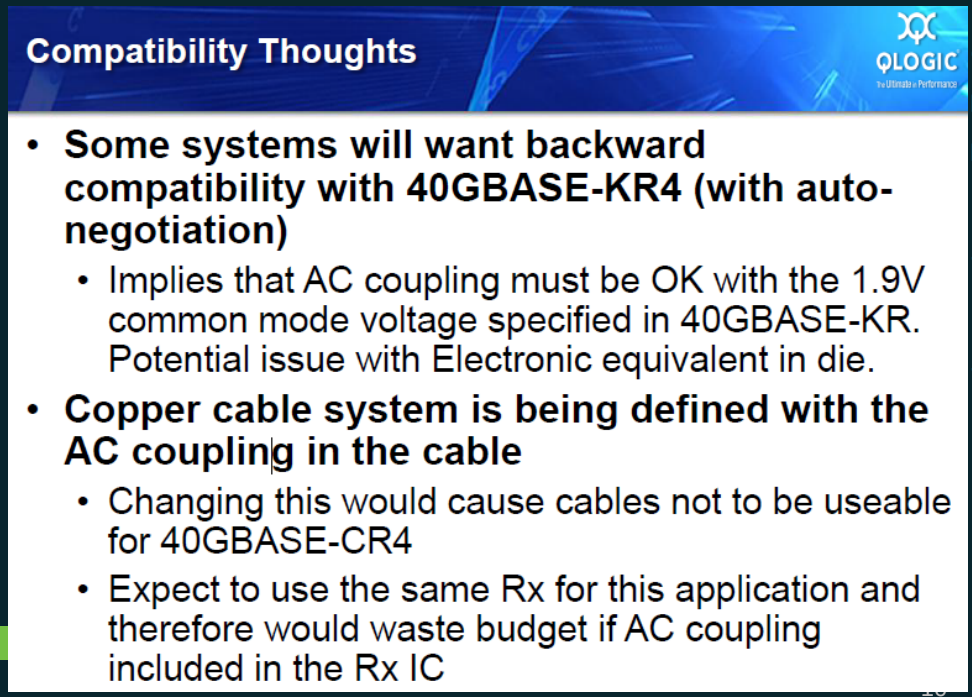




Summary/images from Beth Kochuparambil (…) See goergen_02_0512.zip for full presentation and details.

Summary of Data from Calls

- Mike Dudek (Qlogic) – Discussion points
- Backward compatibility – concerns of common-mode for on-die cap or equivalent circuitry
- Reuse of RX – concerns if one RX has cap and one doesn't
- Advantages and disadvantages discussed of 3 AC cap allocations
  - In channel (as in OIF-25G-LR)
  - In RX (as in KR – 10G backplane)
  - Write separate specification for cap



Summary/images from Mike Dudek (Qlogic) See goergen_02_0512.zip for full presentation and details.

Summary of Data from Calls: Implementation Limitations

- PCB board space & routing & manufacturability
- Package space & routing for high SerDes count
- Advanced PCB technologies for lower impact adds cost
- Backwards compatibility (ie: cap on B of A+B+C, on-die common mode)

Summary of Data from Calls: Possible Locations for Blocking Cap

Location	Comments
Embedded TX die/pkg	not advised
In connector	avoids PCB via footprint; no public data or massive volumes available
PCB, traditional footprint*, not optimized**	up to 5dB IL impact; placement/space limited
PCB, traditional footprint*, optimized**	IL impact; placement/space is additionally limited; PCB manufacturing limited
PCB, advanced technologies/techniques***	Lower impact of PCB implementations; high cost; manufacturing is not as repeatable
Physically on the package	No data of impact has been shown; placement/space limited, esp. for high SerDes count
Embedded on RX die (Equivalent circuitry, other)	IL impact decreases; common mode and compatibility concerns; does it have sufficient blocking capabilities

* traditional footprint refers to plated through hole (hole drilled through thickness of the board and plated with Cu to connect layers), PTH, to/from routing layer and surface mounted capacitor package

** optimization of traditional footprint includes, but is not limited to: backdrilling, spacing, grounding/isolation, pad structures, etc.

*** advanced technologies/techniques such as cap in via/barrel, embedded in board, microvia, etc.

Summary of Data from Calls: Additional Conclusions

- No data shown for impact of embedded cap in connector, package, or die
- RX vendors have little-to-no control of implementation of on-PCB AC cap implementation/footprint.
- Cap impact can no longer be handwaved/ignored; 1-5dB IL impact.
- Optimization can allow designers to have a controlled and limited penalty… Not all implementations can (or will) be optimized (ie: space & cost)
- IEEE specification will be used by public who may or may not have expertise or 3D simulations for optimization

Consensus Brings on Proposals…

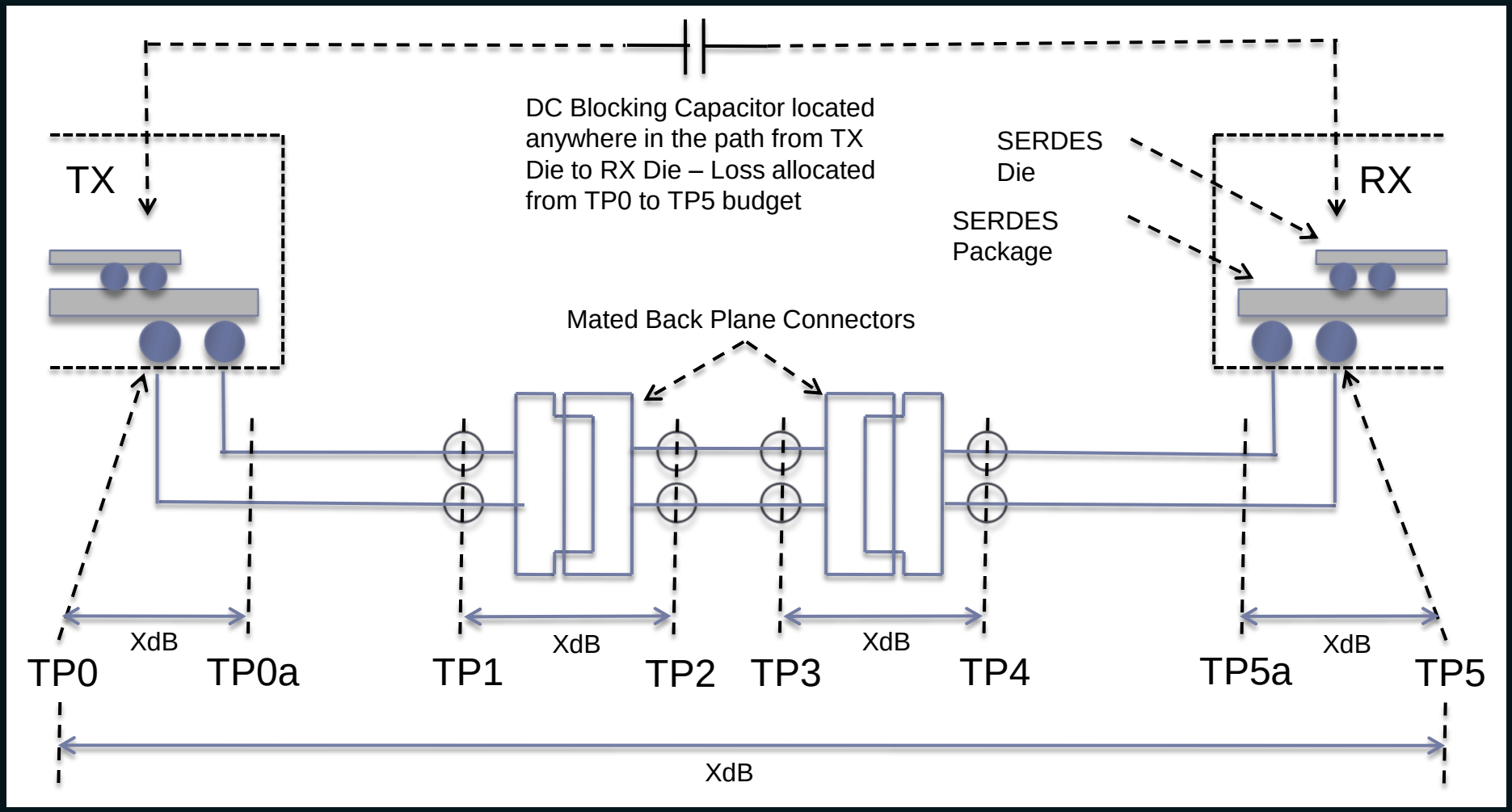
AC Cap Allocation Proposal

- Given limitations and design tradeoff of implementation…

  AC coupling cap impact is to be allocated to the channel budget.

- Considerations shall be made for
  - public use and approximate impact
  - allowing multiple implementation options (including cap-equivalent in RX)

Test Point Proposal



Test Point Proposal - Definitions

Test Point	Description
TX	Defines the transmitserdes die and package to the BGA
TP0	TX BGA attach to the circuit board pad
TP0a	TX De-Embedding Point for TX verification
TP1	Circuit board pad to connector pin connection
TP2	Circuit board pad to connector pin connection
TP3	Circuit board pad to connector pin connection
TP4	Circuit board pad to connector pin connection
TP5a	RX De-Embedding Point for RX verification
TP5	RX BGA attach to the circuit board pad
RX	Defines the receiver serdes die and package from the BGA

Test Point Proposal – Span Loss

TEST Point SPAN	Definition	Loss Budget in dB (PAM4 / NRZ)
TP0 – TP0a	TX De-Embedding Trace	
TP0 – TP1	Circuit Board Trace from the TX BGA to the first connector	
TP1 – TP2	First Mated Connector	
TP2 – TP3	Circuit Board Trace of the back plane / mid plane	
TP3 – TP4	Second Mated Connector	
TP4 – TP5	Circuit Board Trace from the second connector to the RX BGA	
TP0 – TP5	Complete Channel, TX BGA to RX BGA	(33 / 35)
TP5a – TP5	RX De-Embedding Trace	

In Addition to Adopting Test Points… Informative Impact Table Proposal

- Addressing public usability of specification
- Recommend providing informative ‘guidelines’ for IL, ILD, and ICR limitations for implementation types? (to be accounted for within the channel budget)
- Allows for simple understanding of loss budget “remaining” for PCB trace
- Impact table would give a ‘rule of thumb.’ Implementation could be better (or worse) than impact table, recognizing the full channel budget is the qualifier.

Motions and Straw Poll

- Move that the AC coupling cap is to be allocated to the channel budget
- Move to adopt baseline proposal for test point definition as per goergen_01a_0512 slides 16-18.
- Straw poll: To what level would you support the inclusion of an informative impact table as a part of the standard/appendix?
  - -Support and willing to contribute data
  - -Support the inclusion in the specification – not likely to contribute
  - -Support concept, but not in specification
  - -Do not support the impact table concept for AC cap implementation