Connector for IEEE802.3bj MDI and Future Multi-hundred Gb/s System

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Rev. B (Corrected page 9)

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Proposal Background

• QSFP28 has been adapted as a baseline proposal for a type of MDI for 100GBASE-CR4

• CFP-MSA is in process to finalize CFP2 CFP4 specification for 4x28G application

• Mechanical features and SI performance of CFP4 fit to MDI

• CFP2 and CFP4 are considered as a candidate of future generation of multi hundred Gb/s system

• CFP4 should be recognized as a MDI option on 802.3bj

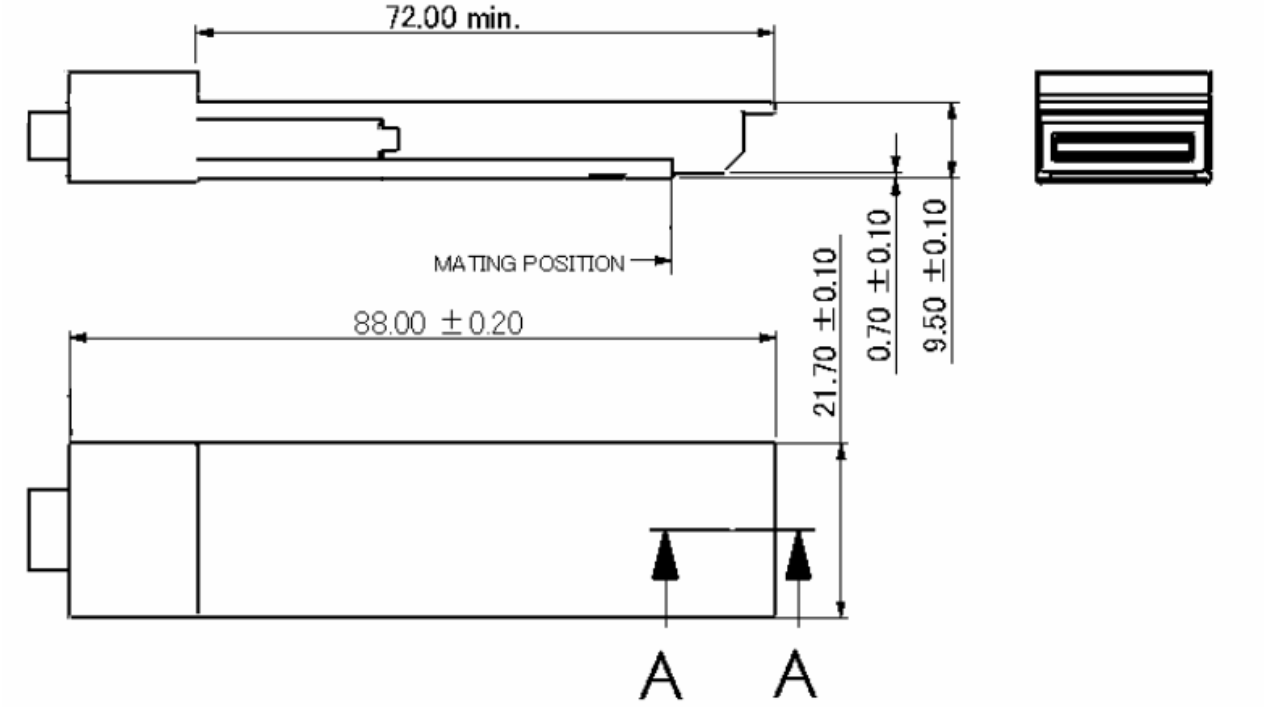
CFP4 Overview

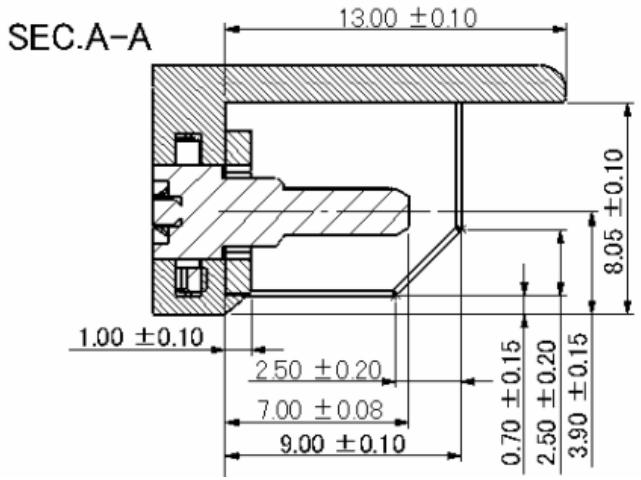
- Comparison between others

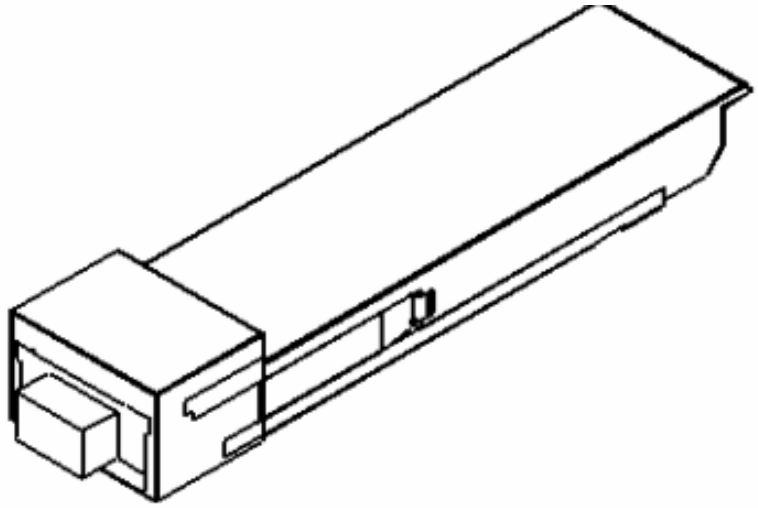
Category	CFP	CFP2	CFP4	QSFP28
Host rates max.	11.2G	28G	28G	28G
Total # of pins	148	104	56	38
TX + RX (Diff. Pairs)	10+10, 11+11, 12+12	4+4, 8+8, 10+10	4+4	4+4
REFCLK (Diff. Pairs)	1	1	1	0
Monitor Clocks (Diff. Pairs)	2	2	1	0
Ports in 364mm faceplate	4	8	16	18
module width (mm)	82 (76 main top)	41.5	21.7	18.3
module length (mm)	145	106	88	74
module main body height (mm)	13.6	12.4	9.5	8.5

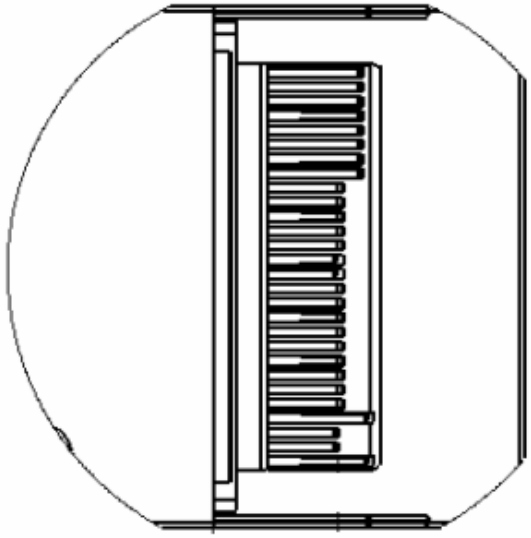
CFP4 Overview

• CFP4 has plug connector on its mating interface which provides mating accuracy and helps to achieve high speed performance



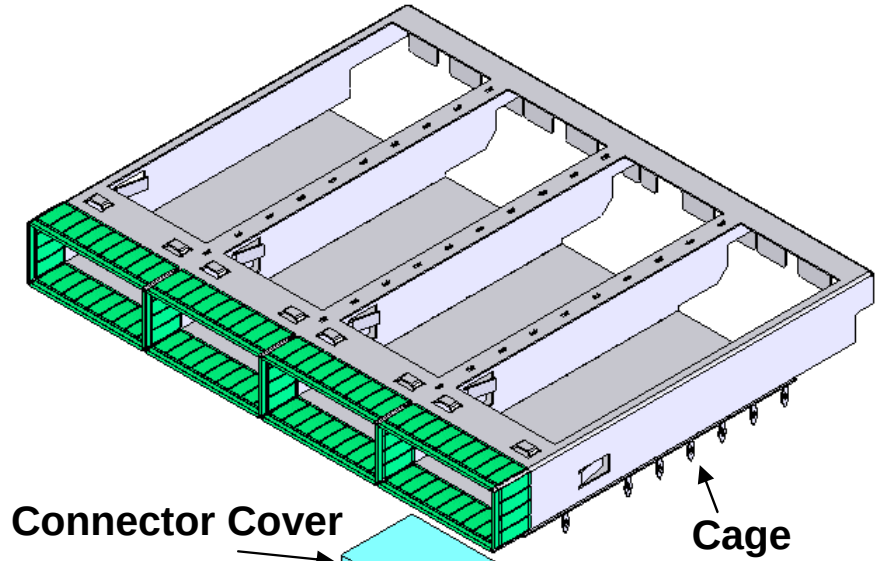


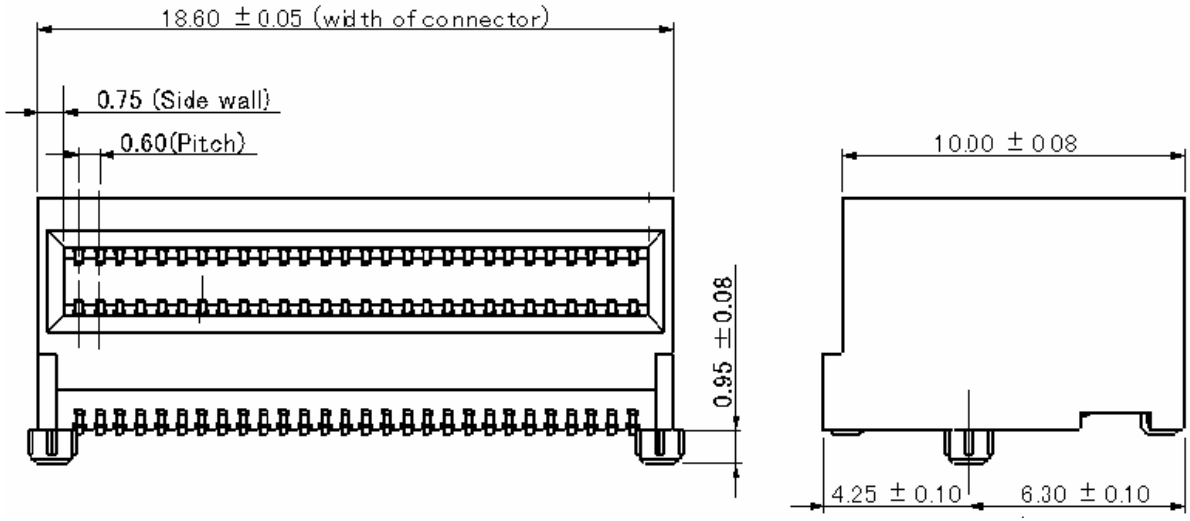


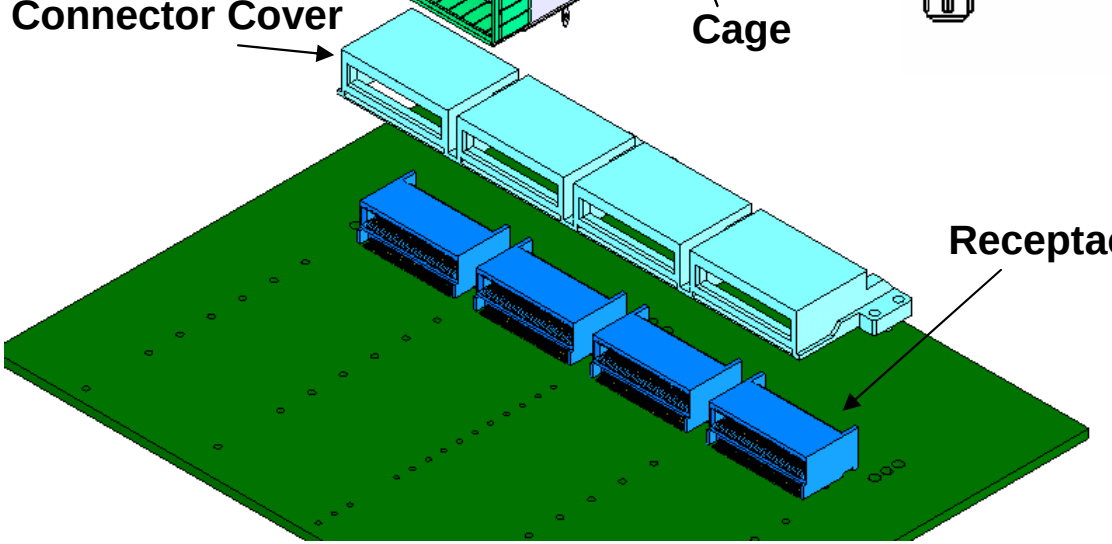


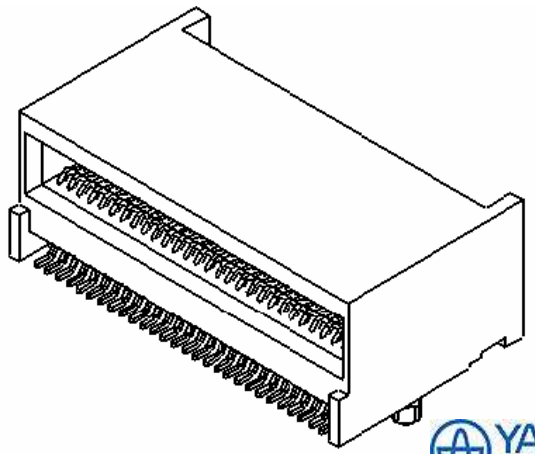
CFP4 Overview

- Surface mount receptacle connector
- Connector cover work for EMI noise shielding, and protects receptacle connector from mechanical stress



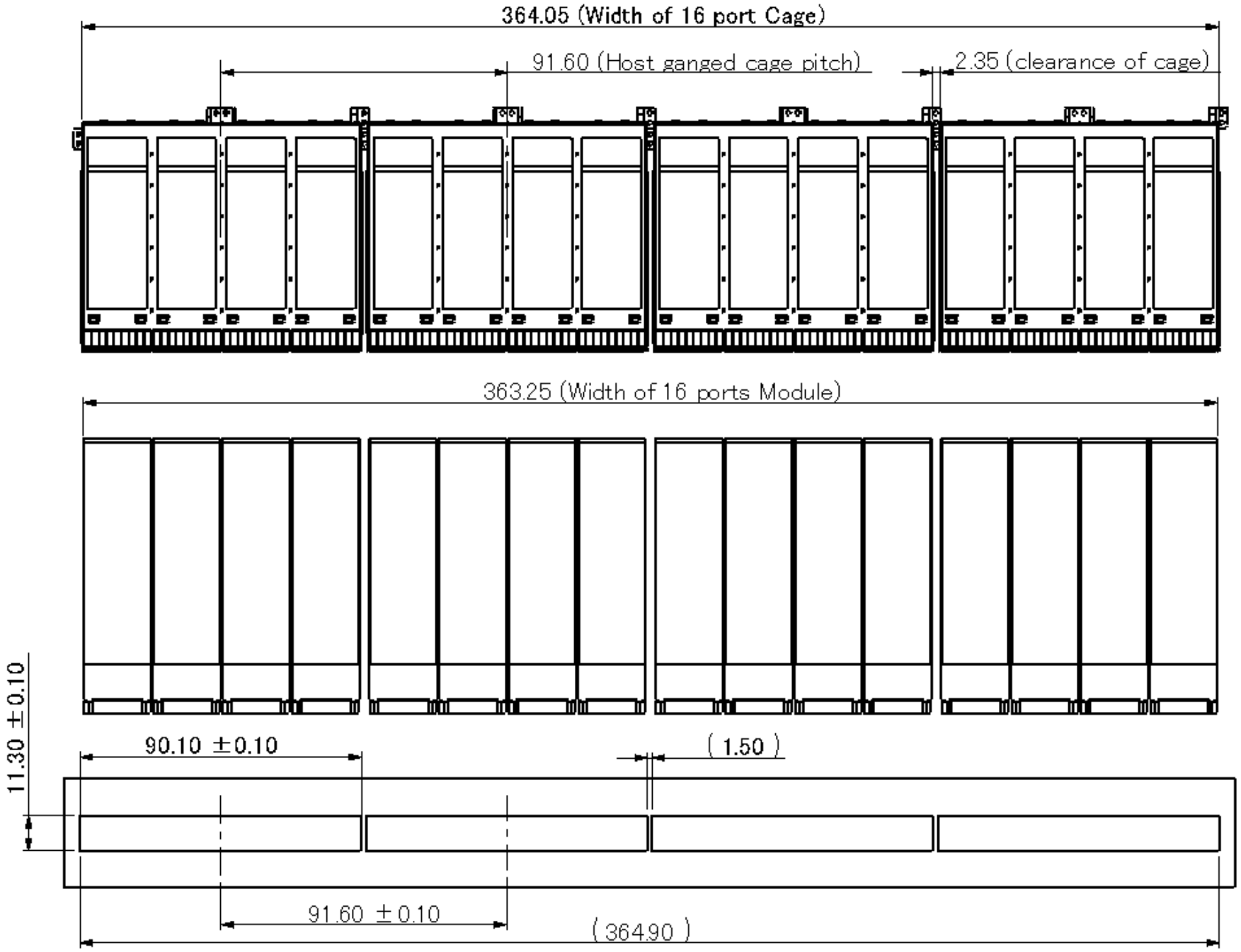






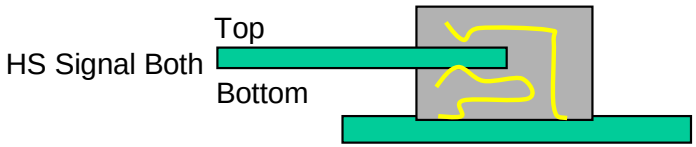
CFP4 Overview

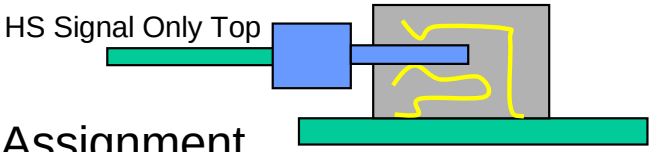
- 16 CFP4 fits in 365mm faceplate



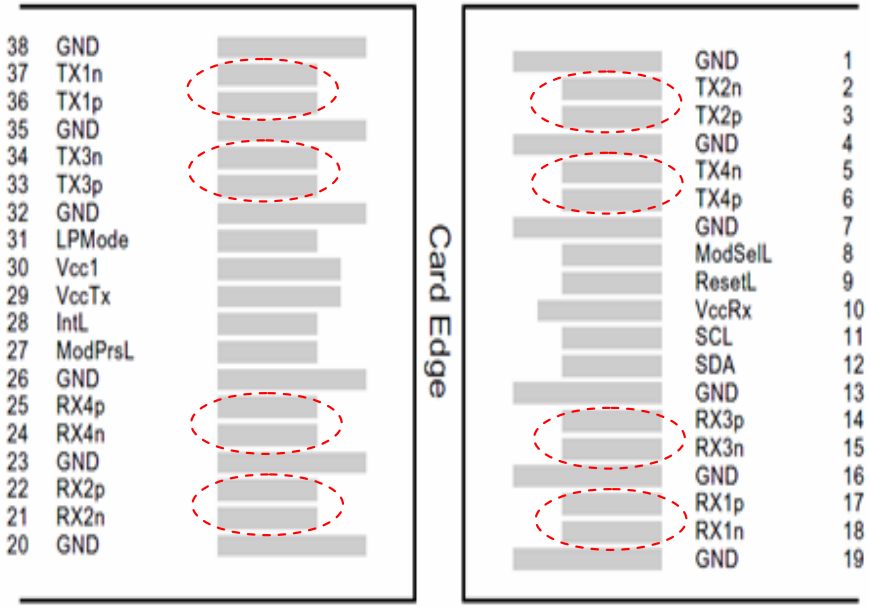
CFP4 Pin Assignment Advantage

- QSFP28: High speed signals are located on both top and bottom row (2 top + 2 bottom)
- CFP4: All 4 high speed signals are located on top row of the connector
  - Possible simple board layout to achieve best channel performance





QSFP28 Pin Assignment

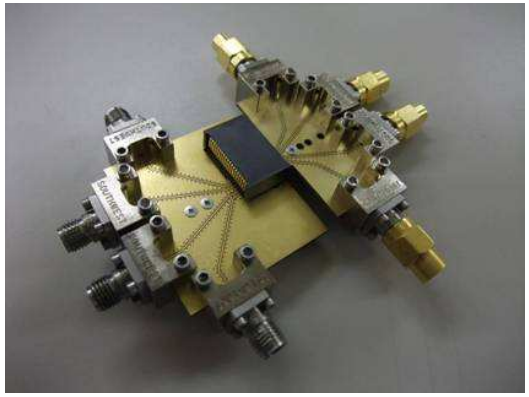


CFP4 Pin Assignment

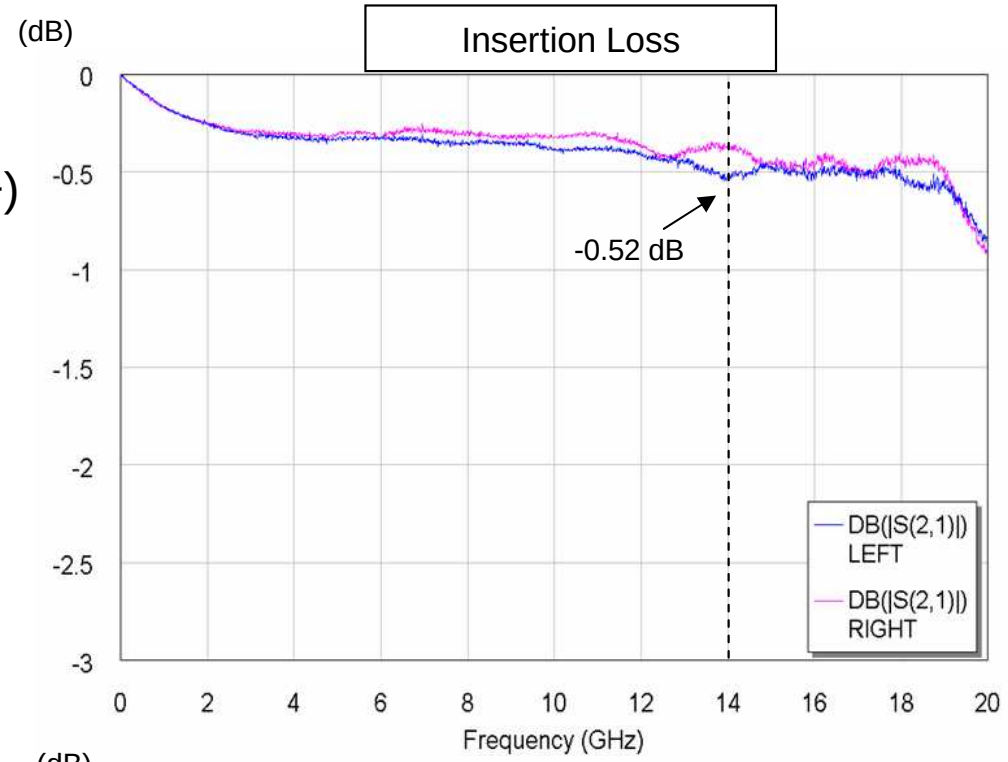
	Top			Bottom
56	GND		1	3.3V_GND
55	TX3n		2	3.3V_GND
54	TX3p		3	3.3V
53	GND		4	3.3V
52	TX2n		5	3.3V
51	TX2p		6	3.3V
50	GND		7	3.3V_GND
49	TX1n		8	3.3V_GND
48	TX1p		9	VND_IO_A
47	GND		10	VND_IO_B
46	TX0n		11	TX_DIS
45	TX0p		12	RX_LOS
44	GND		13	GLB_ALRMn
43	*(REFCLKn)*		14	MOD_LOPWR
42	*(REFCLKp)*		15	MOD_ABS
41	GND		16	MOD_RSTn
40	RX3n		17	MDC
39	RX3p		18	MDIO
38	GND		19	PRTADR0
37	RX2n		20	PRTADR1
36	RX2p		21	PRTADR2
35	GND		22	VND_IO_C
34	RX1n		23	VND_IO_D
33	RX1p		24	VND_IO_E
32	GND		25	GND
31	RX0n		26	*(MCLKn)*
30	RX0p		27	*(MCLKp)*
29	GND		28	GND

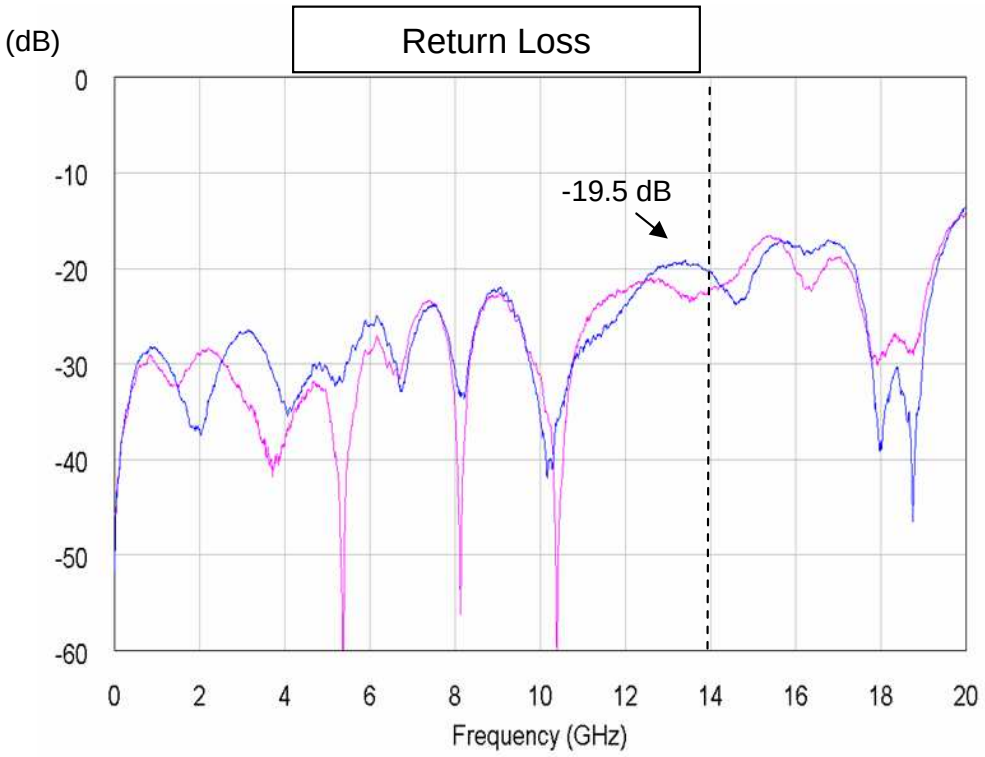
QSFP28 SI Performance

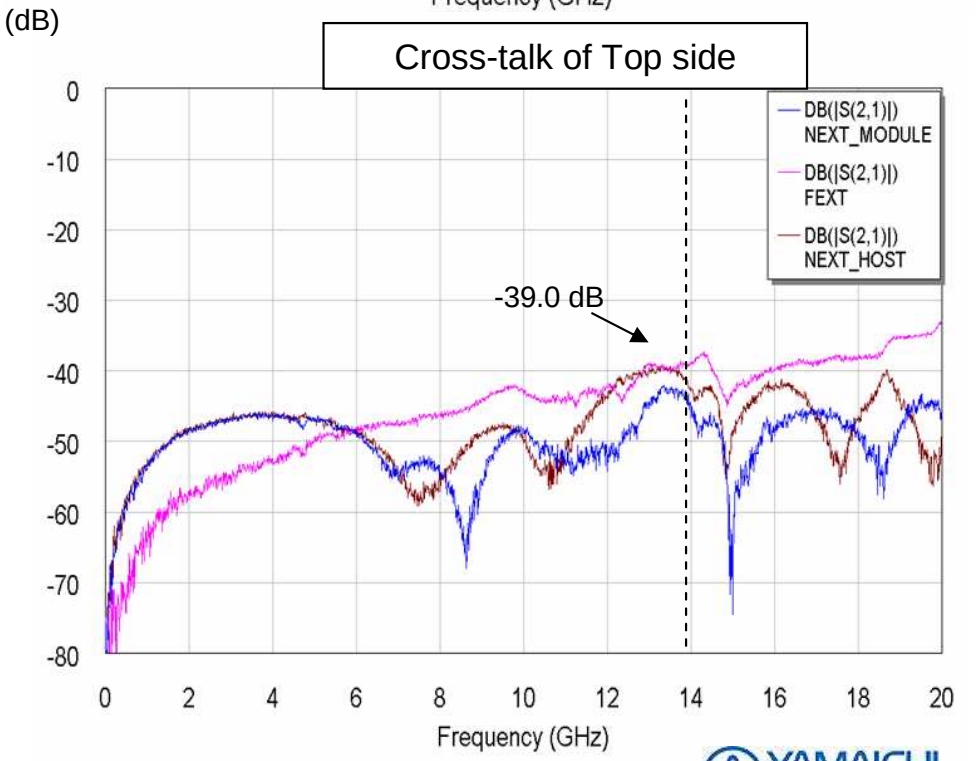
(Actual measurement data at Yamaichi eQSFP+)



Top side adjacent differential signals

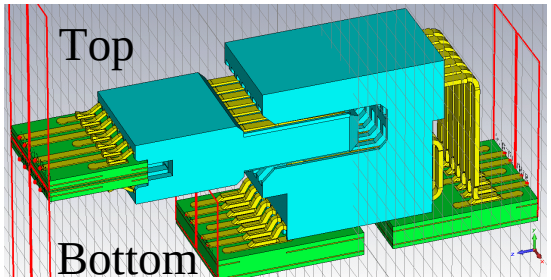




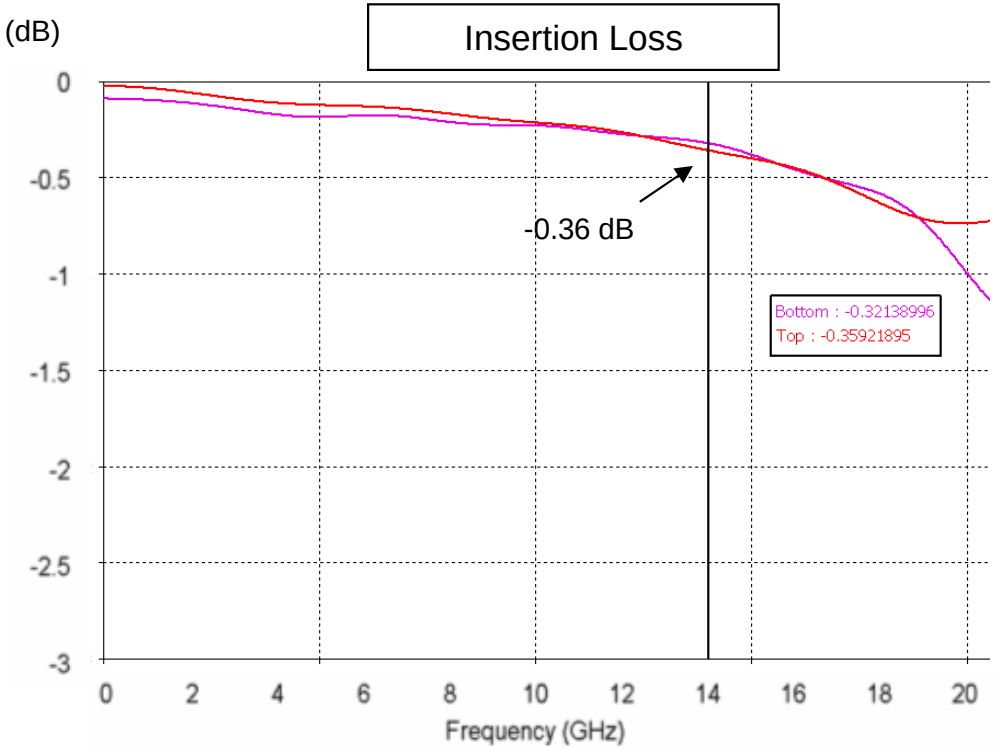


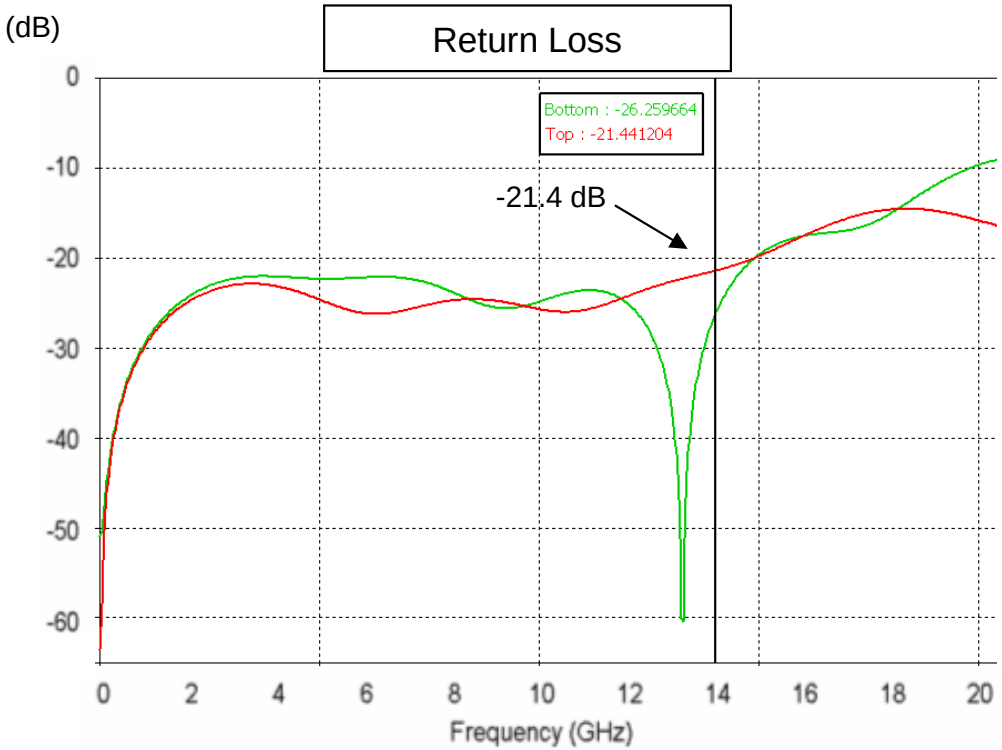
CFP2 CFP4 SI Performance

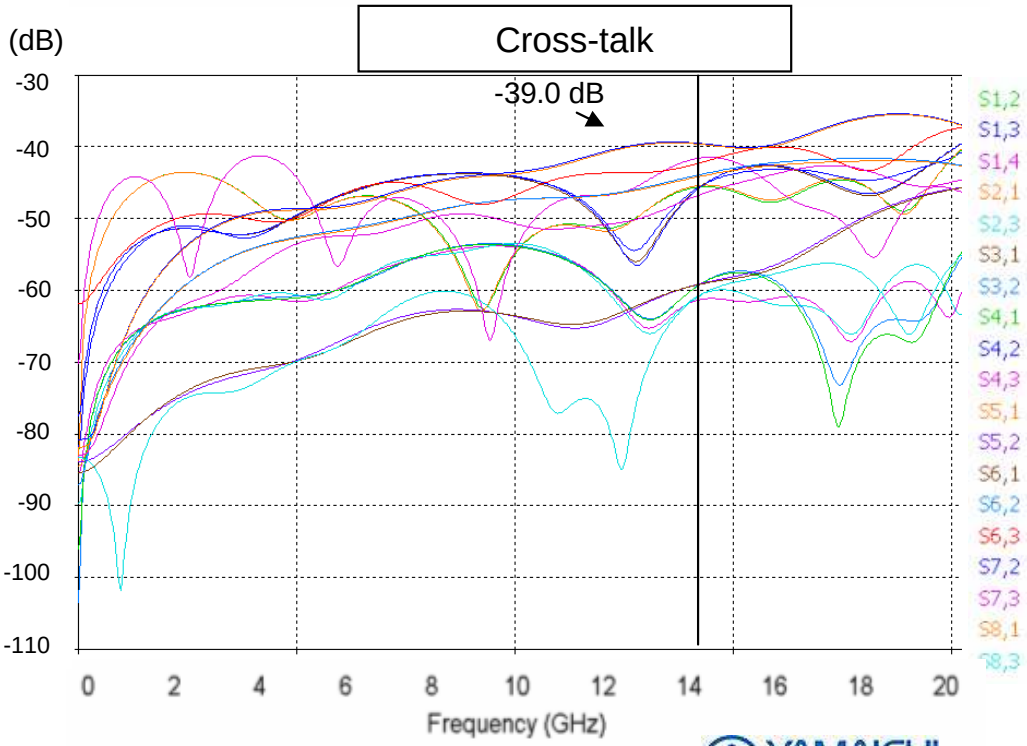
(Simulation data at latest Yamaichi design)



Adjacent differential signals on both top and bottom side







CFP2 / CFP4 Channel SI Performance Simulation Up To 50GHz

CFP2 CFP4 CONNECTOR

・2 adjacent high speed on top side

HOST BOARD

・Board material = N4000-13si(ε =3.2,tan δ =0.007)

・Trace length = **4”** and **7”**

・Trace geometry = Stripline

・Trace width = 5 mils

・Differential trace spacing = 6 mils

・2 signal layers

・Layer connection = layer 2 (near top)

・Counterbored (18mil stub)

・2 via (connector side and Device side)

PLUG BOARD

・Board material = N4000-13si(ε =3.2,tan δ =0.007)

・Trace length = **1.25”**

・Trace geometry = microstrip

・Trace width = 7 mils

・Differential trace spacing = 5 mils

・No via required on module PCB

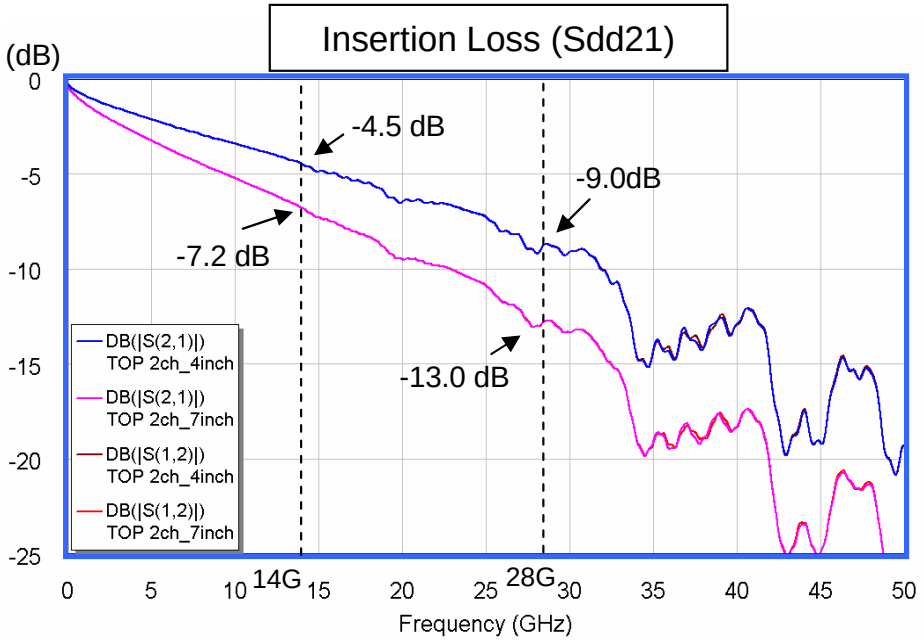
CFP2 CFP4 Channel SI Performance Simulation Result

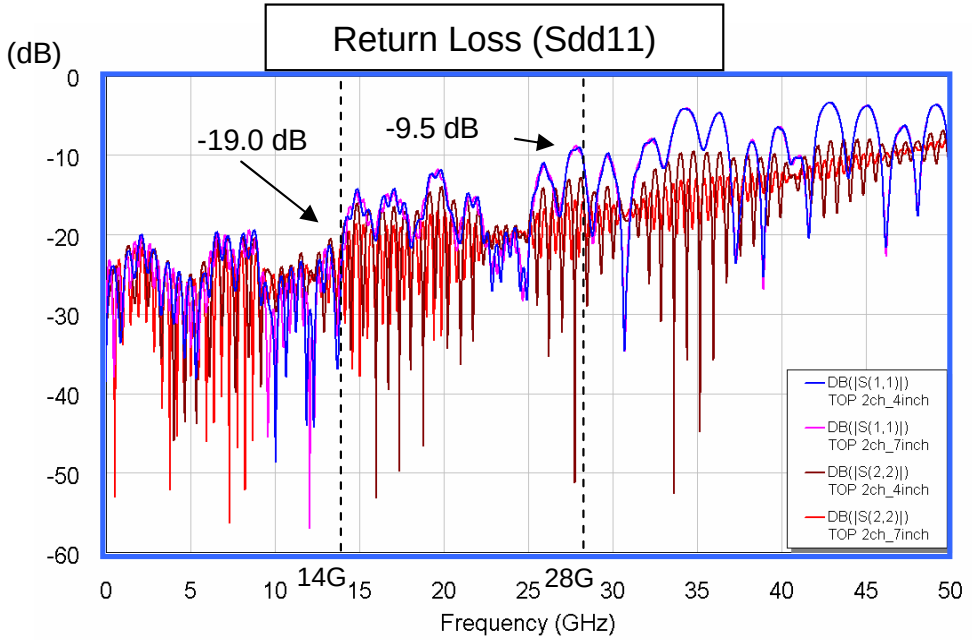
4inch Host, Driven from Host Side

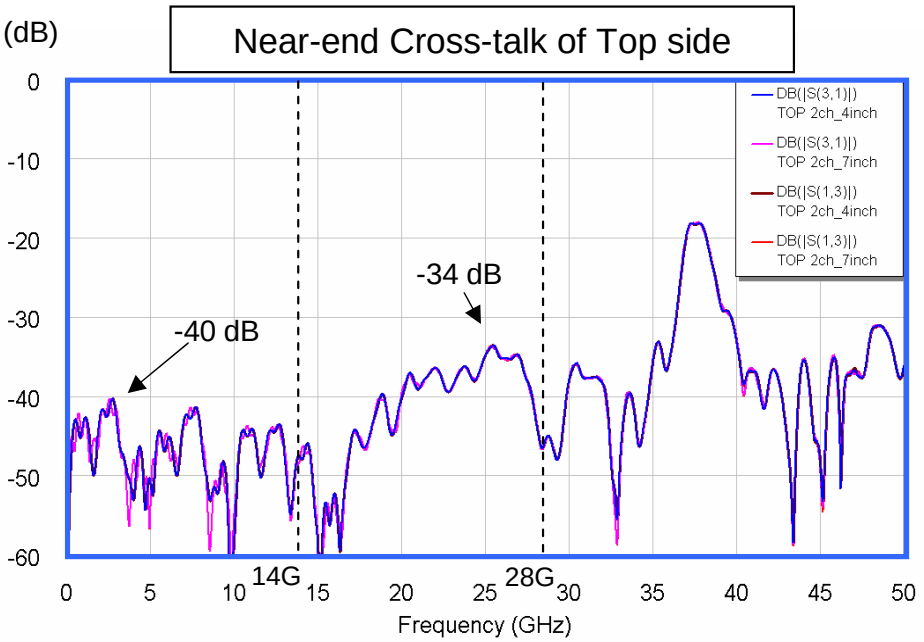
7inch Host, Driven from Host Side

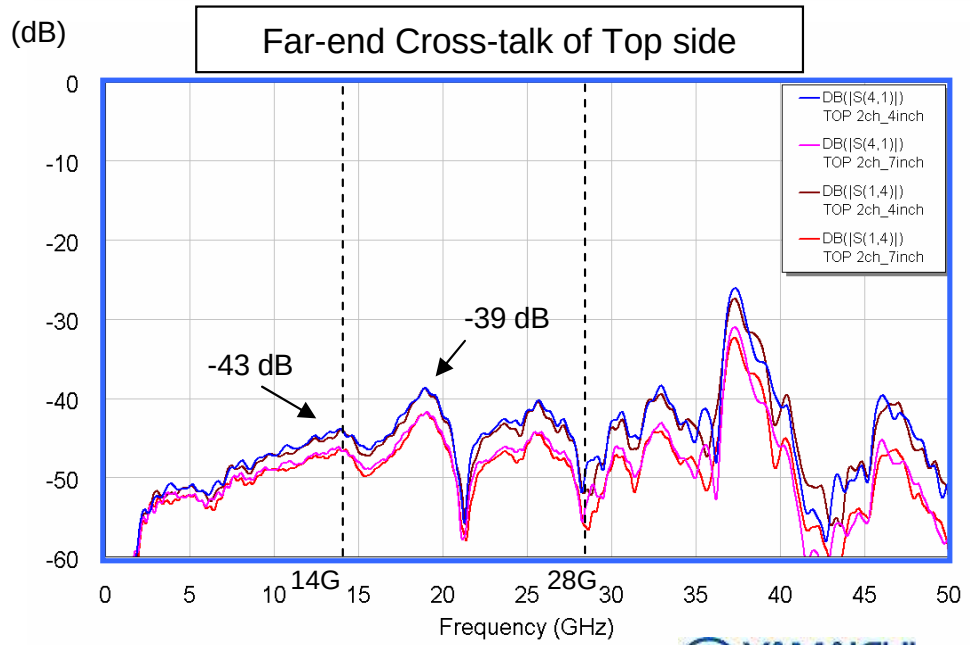
4inch Host, Driven from Module Side

7inch Host, Driven from Module Side









Summary

• IEEE 802.3bj should adopt both QSFP28 and CFP4 as baseline proposal for MDI