Simplified AM Sync Up

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Introduction

- Today the 802.3bj draft has the following AM format:

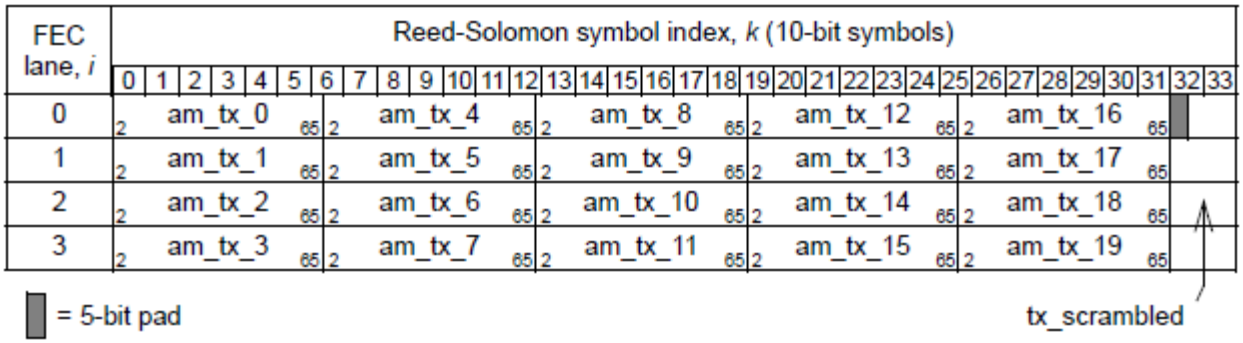

Figure 91–4—Alignment marker mapping to FEC lanes

- The draft also allows any logical lane to appear on any physical lane
- To sync up to the AMs quickly, a parallel search much take place on each lane, looking for any of the 4 lead AMs (0-3). EEE complicates this more.
- This is a significant amount of logic, which can dominate the non FEC portions of the FEC sublayer
- Is there a simpler way which will reduce the logic?
- This was not a problem for 802.3ba since there we obtain block lock before looking for AMs

Simpler Way?

- Repeat AM0, and AM16 across all 4 lanes
- That allows the receiver to do a parallel search for a single pattern instead of 4 different patterns across all lanes, then the logical lane number is identified by the other AMs
- In order to maintain BIP transparency, the BIP fields are not replaced, instead just M0-M3 and M4-M6
- AM0 is repeated for normal lock, and AM16 is repeated for EEE mode where you lock to both the first and fifth AM

FEC Lane #					
0	AM0	AM4	AM8	AM12	AM16
1	AM0	AM5	AM9	AM13	AM16
2	AM0	AM6	AM10	AM14	AM16
3	AM0	AM7	AM11	AM15	AM16

How Much Logic Can be Saved?

- **This depends on how you find lane lock**
- **If you scan serially, and are not too concerned with the lock time, then the logic saved is not that much**
- **If you scan in parallel, to find lock as quickly as you can, which is needed for EEE deep sleep mode, than the logic savings is significant**
  - Fast lock could be up to 30% or more of the block
  - This can be reduced by ~75% with this change

What needs to be changed?

- **91.5.2.6 Alignment marker mapping**
  - Change the mapping for the exceptions that would be for the first and last AMs per lane (repeating AM0 and AM16). Includes and update to figure 91-4
- **91.5.3.7 Alignment marker mapping and insertion**
  - Change the mapping for the exceptions that would be for the first and last AMs per lane (repeating AM0 and AM16)
  - Change to a replacement strategy for all AMs vs. mapping with errors to be consistent
  - Handle the delta for the EEE rapid AMs
  - BIP fields are mapped transparently
- **91.5.4.2.1 Variables**
  - Update amp_valid, no longer are all AMs unique on each lane
  - fec_lane, to be derived from the "alignment marker payload sequence" for lane x of the PMA service interface.
- **91.5.4.2.2**
  - AMP_COMPARE, update that this is always 0 and 16
- **91.5.4.2.3**
  - Amp_counter, update that it is always 0 and 16

A Note of BIP Transparency

- **With the replacement of some of the AMs as described in the previous slide, the BIPs are not completely transparent anymore since an error in some of the AMs would be overwritten.**

- **Options to deal with it:**
  - Replace markers as proposed, BIP is not completely transparent, is that a big concern? still mostly transparent, and errors in markers do not impact anything unless they are excessive, no packets dropped etc. Intermediate nodes can still keep track of BIP errors for debug purposes.
  - Corrupt bits in the new markers and copy these over as needed at the far end, it preserves the BIP transparency, but requires some extra circuitry for not much gain in value?
  - Not make the change.

Thanks!