Performance Evaluation of Transcoding and FEC Schemes for 100 Gb/s Backplane and Copper Cable

IEEE 802.3bj Task Force

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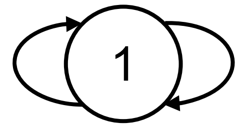
Outline

- Error models at RS decoder input
- Define coding gain
- Compute coding gain
- Compare error-rate performance for selected schemes
  - Post-decoding bit error rate vs. pre-decoding bit error rate
  - Post-decoding bit error rate vs. signal-to-noise ratio
- Error flooring

Independent Bit Error Model

(e = 0, 1 - p_b)  (e = 1, p_b)

- Very simple one-state bit error model for additive white Gaussian noise (AWGN)
  - Each state transition labeled by a pair: (error value, state transition probability)
  - Binary bit error values e, i.e., either e = 0 (no error) or e = 1 (error)
- Independent bit errors at Reed-Solomon (RS) decoder input
- Error model determined by only one parameter

p_b = bit error probability at RS decoder input

- Bit error probability p_b for antipodal binary signals as a function of signal-to-noise ratio (SNR)

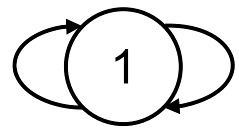
$$p_b = Q(\sqrt{\mathrm{SNR}}) \quad \text{where} \quad Q(x) = \int_x^{\infty} \frac{1}{\sqrt{2\pi}} e^{-y^2/2} dy \quad \text{and}$$

SNR = $d^2_{min}/(4\,\sigma^2)$,

d_{min} = distance between two signal levels

σ = noise standard deviation

Independent Symbol Error Model

(correct symbol, 1 - p_{sym}) 

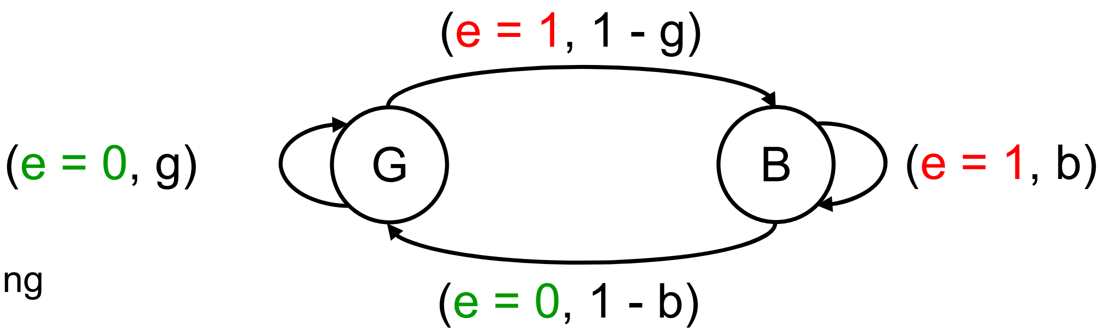
(erroneous symbol, p_{sym})

- Very simple one-state symbol error model
- m-bit symbols at decision-feedback equalizer output
- There are 2^m-1 possible symbol errors
- Independent symbol errors at RS decoder input
- In this work, symbol errors (not bit errors) at RS decoder input are assumed to be independent in order to compute random coding gain
- Error model determined by only one parameter

p_{sym} = symbol error probability at RS decoder input

Symbol errors at DFE output are modeled as independent errors to compute random coding gain

Gilbert Burst Error Model



No precoding

- A simple two-state Gilbert burst error model [1] accounting for DFE error propagation
  - Each state transition labeled by a pair: (error value, state transition probability)
  - Binary bit error values e, i.e., either e = 0 (no error) or e = 1 (error)
- Correlated bit errors at RS decoder input accounting for DFE error propagation
- Error model determined by two parameters

p_b = bit error probability at RS decoder input

b = probability of staying in bad state B (b = 0.5 assumed in this work)

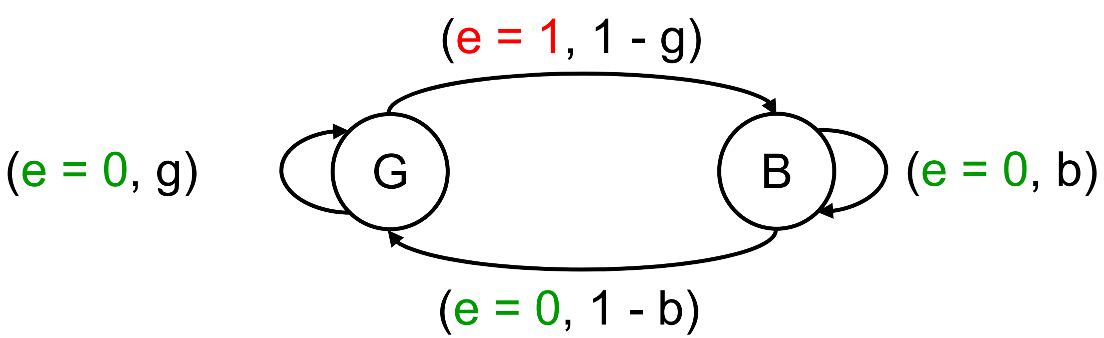
[1] E. N. Gilbert (1960), "Capacity of a burst-noise channel", Bell System Technical Journal 39: 1253–1265.

Gilbert Burst Error Model (cont.)

- Probability g of staying in good state G as a function of p_b and b

$$g = (1 - p_b) + p_b\,(b - p_b) / (1 - p_b)$$

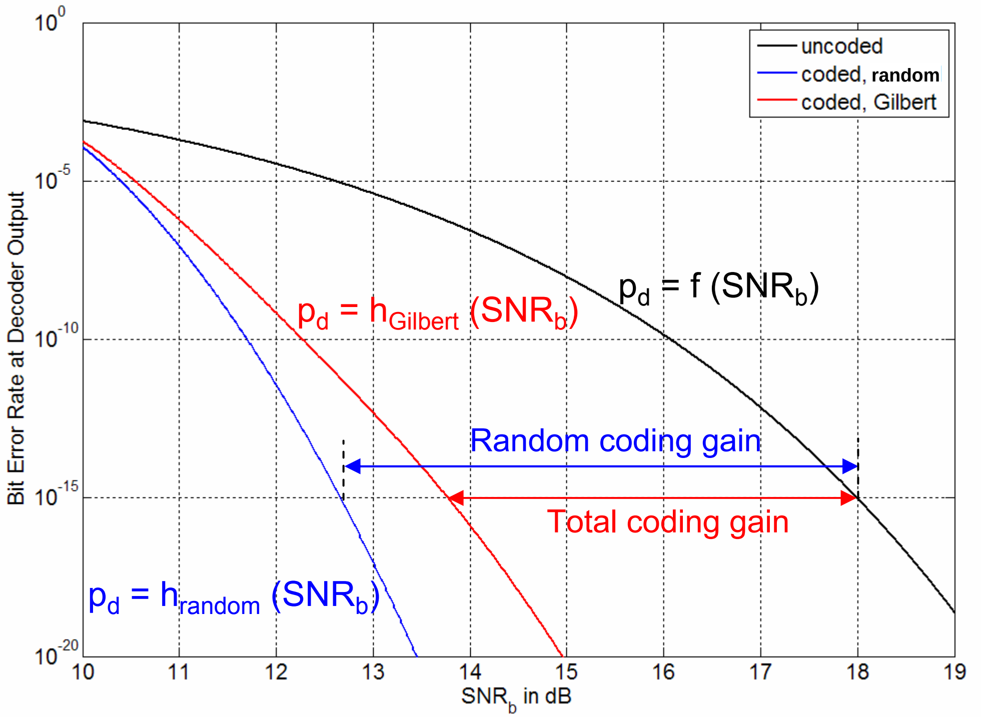
- Steady state
  - probability of being in good state G is (1-b) / (2-b-g)
  - probability of being in bad state B is (1-g) / (2-b-g)
- Model to determine bit error probability w/o DFE error propagation



- DFE slicer bit error probability w/o error propagation $p_{sl} = (1\text{-}b)\,p_b$

Definition of Coding Gain

- Uncoded case for 0% overclocking (s=0)
- SNR_b = SNR at DFE slicer input assuming previously detected bits are correct and 0% overclocking
- Coding gain depends on target BER, e.g. 1e-15
- Random coding gain in coded case with s% overclocking can be computed using independent symbol error model specified by p_{sym}
- Total coding gain in coded case with s% overclocking computed using Gilbert burst error model specified by the parameters p_b and state transition probability b



Computation of Coding Gain

p_d = Bit error rate (BER) at RS decoder output

Uncoded: SNR_b = SNR at DFE slicer input in uncoded case with 0% overclocking

1) $p_{sl} = Q\,(\mathrm{sqrt}(SNR_b))$, e.g., $p_{sl} = 0.5\,\mathrm{erfc}\,(\mathrm{sqrt}\,(SNR_b / 2))$ for NRZ signaling

2) $p_d = p_{sl} / (1\text{-}b) = f\,(SNR_b)$

Coded: SNR_c = SNR at DFE slicer input in coded case with s% overclocking

1) $p_d = g\,(p_b)$ from decoding with correlated bit errors at RS decoder input

2) $p_{sl} = (1\text{-}b)\, p_b$

3) $SNR_c = (Q^{-1}(p_{sl}))^2$, e.g., $SNR_c = 2\,(\mathrm{erfc}^{-1}(2\,p_{sl}))^2$ for NRZ signaling

4) SNR_c [dB] = SNR_b [dB] - s D [dB] as in bhoja_01_0911.pdf

D [dB] = SNR degradation in dB per 1% overclocking, D [dB] = 0.043 dB in AWGN channel

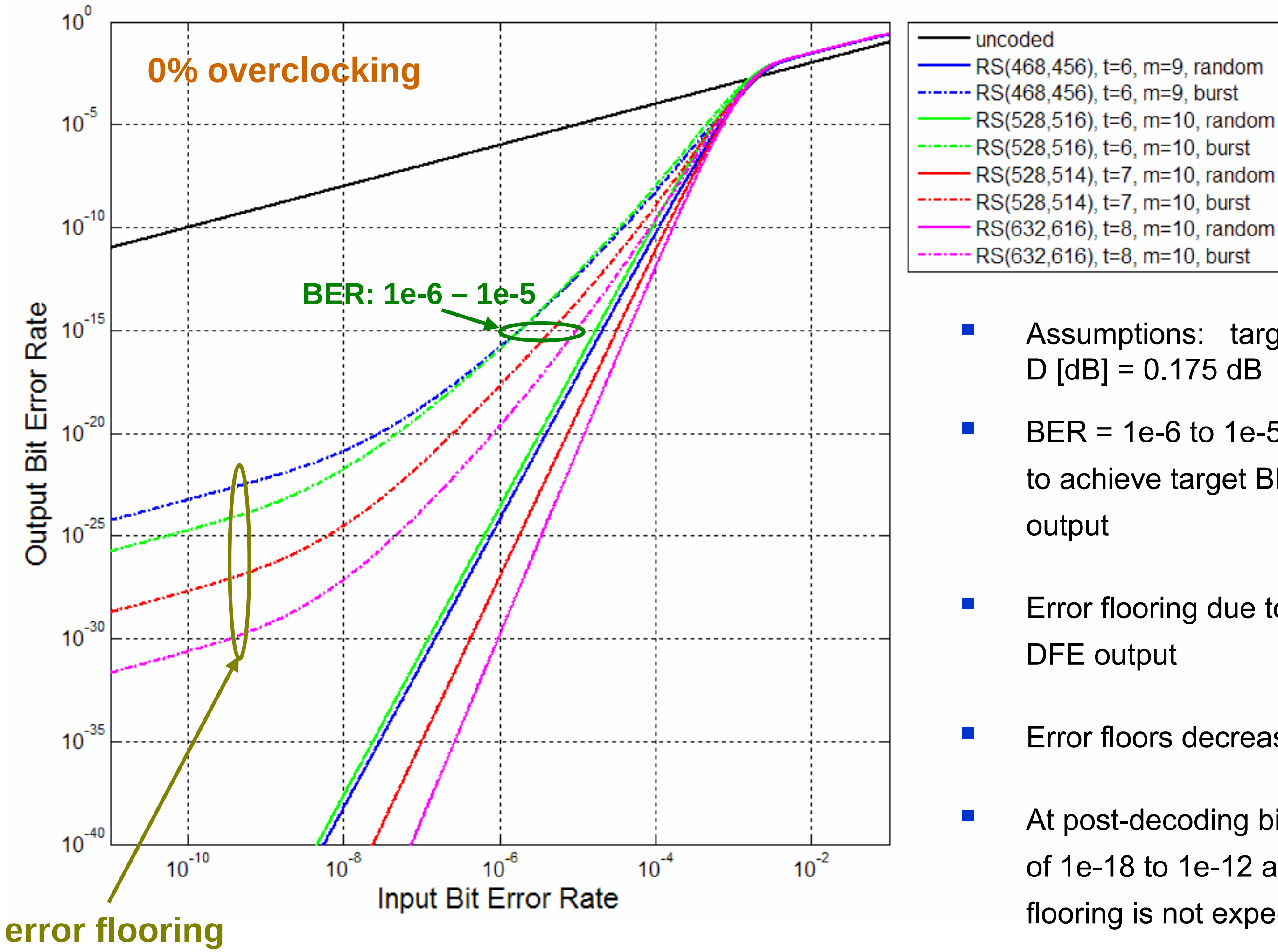
D [dB] ~ (increase in insertion loss for 1% overclocking) / 2 = 0.15 - 0.2 dB on channels w/ 30 – 40 dB loss

5) $p_d = h\,(SNR_b)$

Random coding gain: $p_d = g_{random}\,(p_b)$ is computed using independent symbol error model ➔ $p_d = h_{random}\,(SNR_b)$

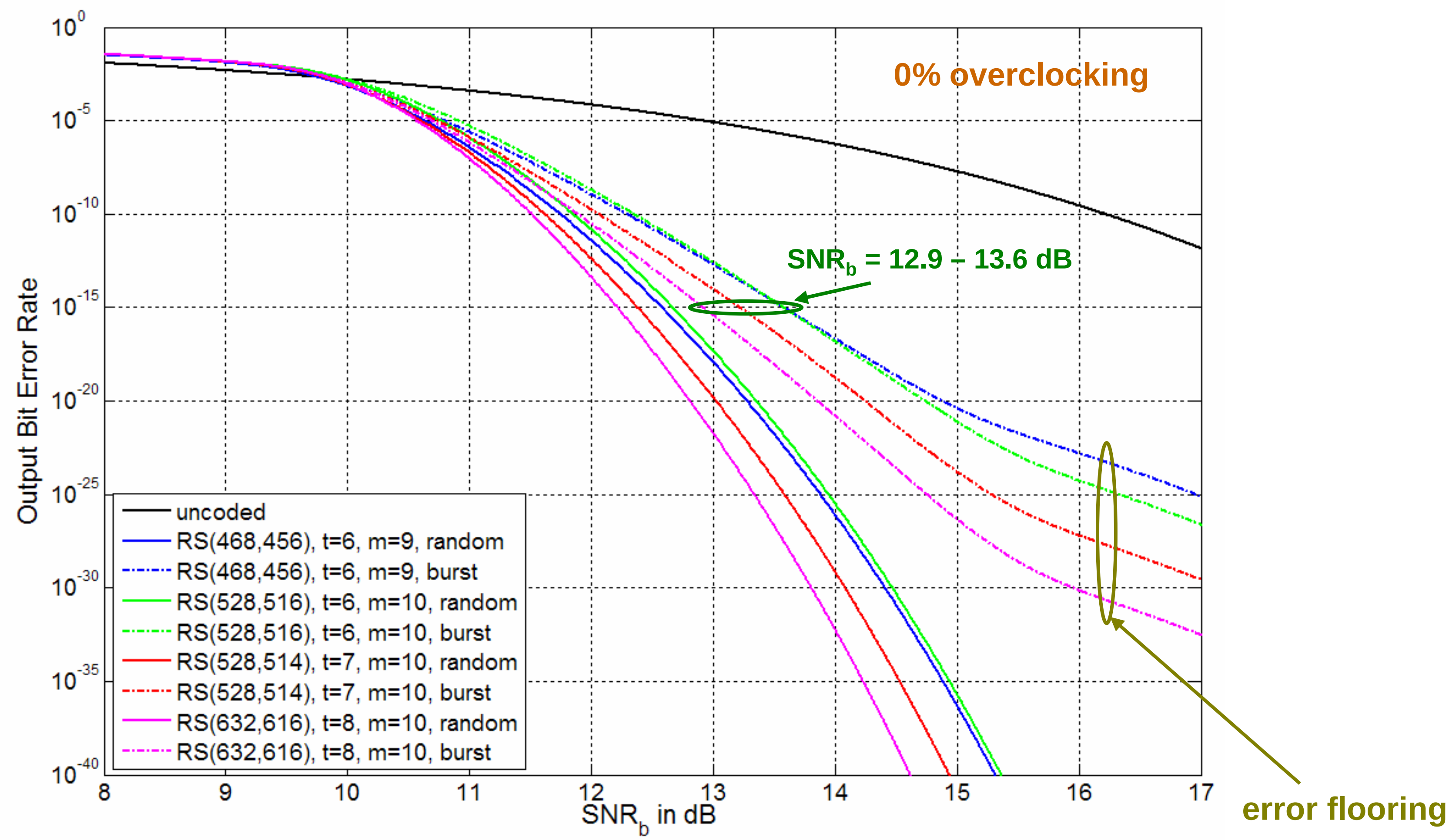
Total coding gain: $p_d = g_{Gilbert}\,(p_b)$ is computed using Gilbert burst error model ➔ $p_d = h_{Gilbert}\,(SNR_b)$

Post-Decoding Bit Error Rate vs. Pre-Decoding Bit Error Rate



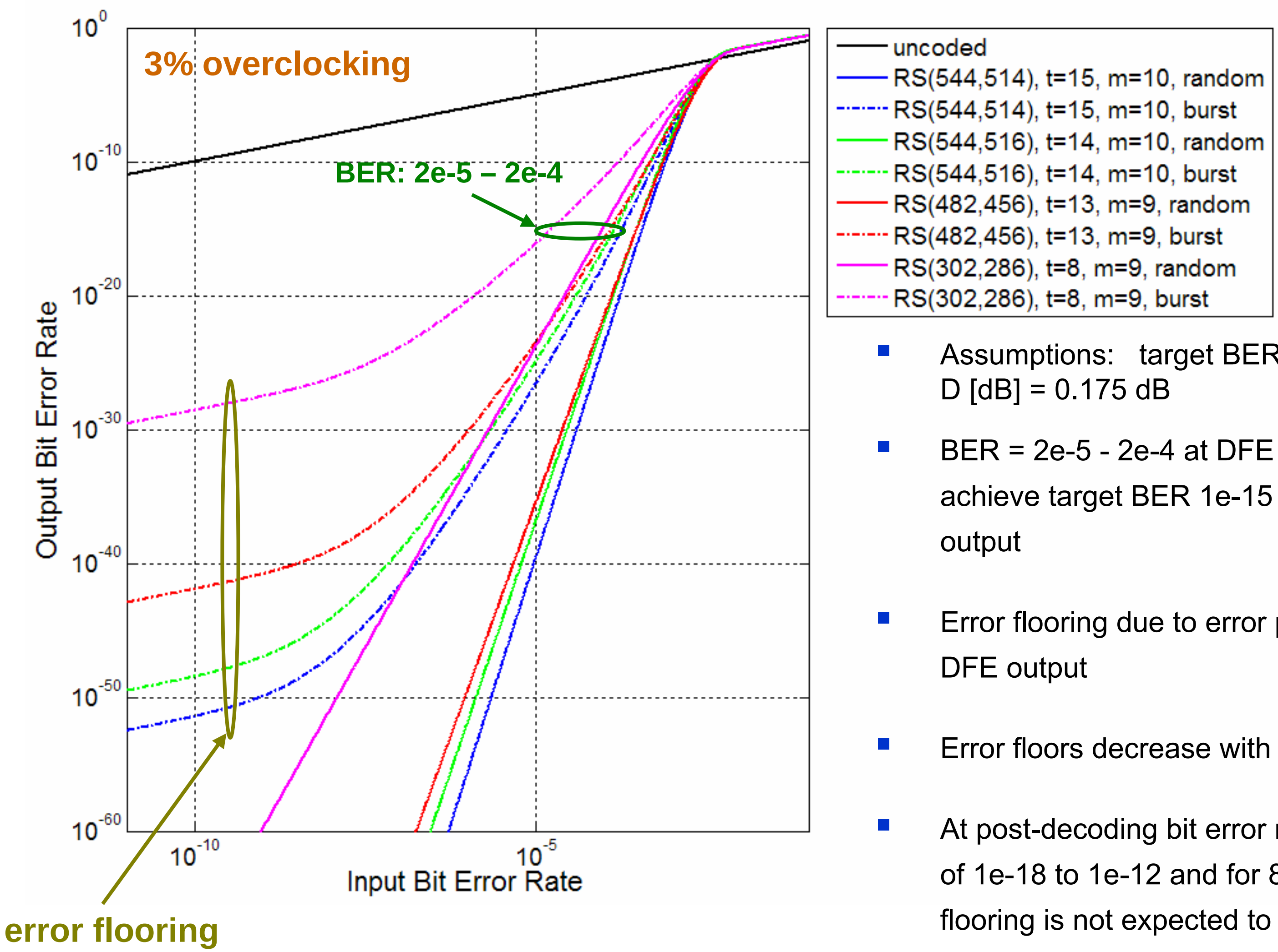
- Assumptions: target BER 1e-15, b=0.5, D [dB] = 0.175 dB
- BER = 1e-6 to 1e-5 at DFE output in order to achieve target BER 1e-15 at RS decoder output
- Error flooring due to error propagation at DFE output
- Error floors decrease with increasing t
- At post-decoding bit error rates in the range of 1e-18 to 1e-12 and for 6 ≤ t ≤ 8, error flooring is not expected to be a problem

Post-Decoding Bit Error Rate vs. SNR_b



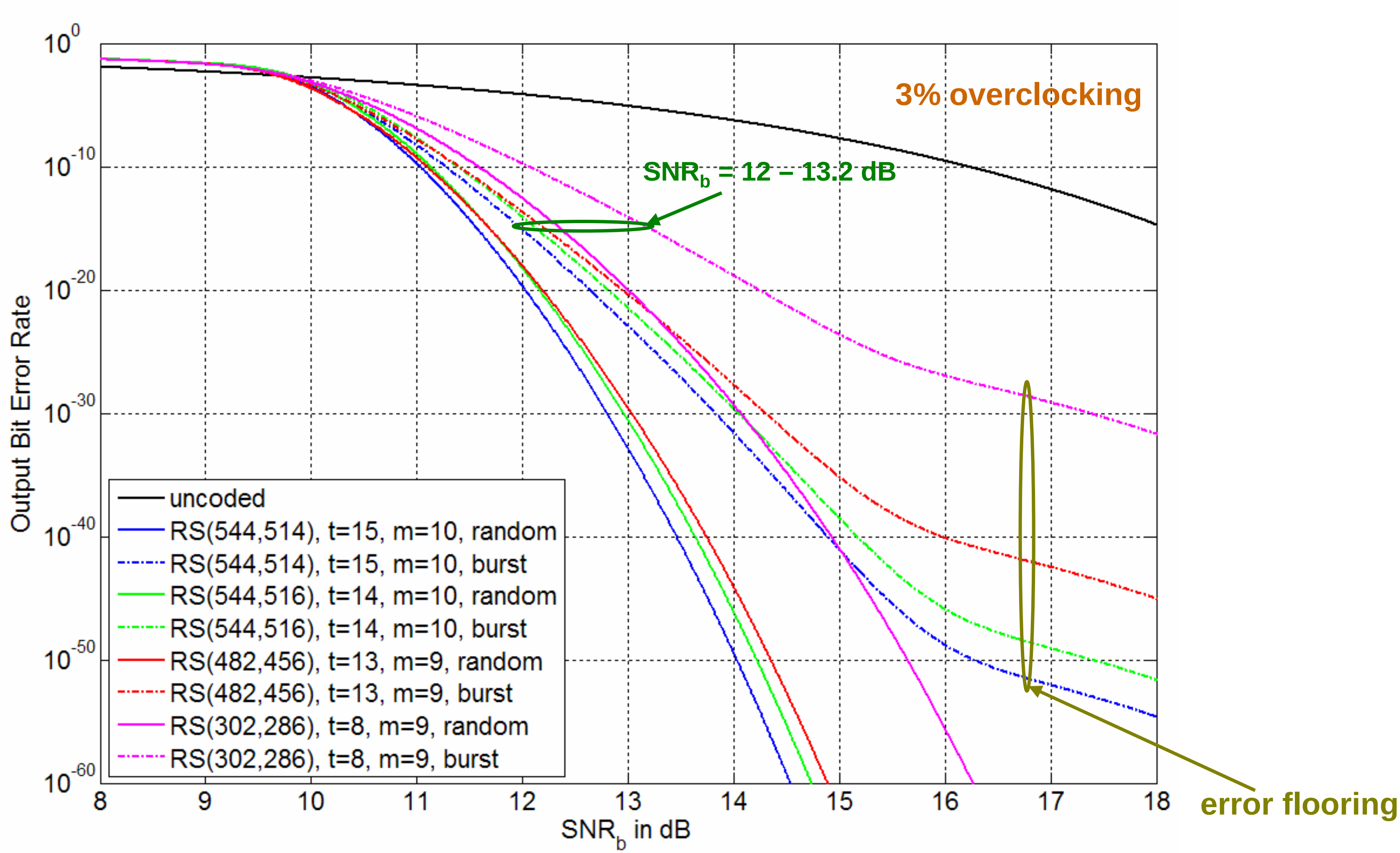
For 0% overclocking and $6 \leq t \leq 8$, SNR_b at DFE slicer input must be 12.9 – 13.6 dB to achieve target bit error rate 1e-15

Post-Decoding Bit Error Rate vs. Pre-Decoding Bit Error Rate



- Assumptions: target BER 1e-15, b=0.5, D [dB] = 0.175 dB
- BER = 2e-5 - 2e-4 at DFE output in order to achieve target BER 1e-15 at RS decoder output
- Error flooring due to error propagation at DFE output
- Error floors decrease with increasing t
- At post-decoding bit error rates in the range of 1e-18 to 1e-12 and for 8 ≤ t ≤ 15, error flooring is not expected to be a problem

Post-Decoding Bit Error Rate vs. SNR_b



For 3% overclocking and 8 ≤ t ≤ 15, SNR_b is in the range 12 – 13.2 dB to achieve target bit error rate 1e-15

Summary

- Introduced error models to evaluate RS decoder performance in the presence of DFE error propagation
- Defined random and total coding gain as a performance measure
- Parameters required to compute coding gain: n, t, m, b, s, D, target BER
- Presented methodology to compute random and total coding gain
- Compared performance of various transcoding and FEC schemes by computing
  - post-decoding bit error rate vs. pre-decoding bit error rate
  - post-decoding bit error rate vs. SNR_b
- Demonstrated existence of error floors which occur below 1e-20 if RS error correction capability $t \geq 6$

Backup

Comparison of Transcoding/FEC Schemes

Total Coding Gain [dB]	Random Coding Gain [dB]	Latency [ns]	TC block size [bit]	FEC	k	n	t	m	Line Rate [Gb/s]	Overclocking [%]	Multiplier of 156.25 MHz
4.51	5.51	87	513	RS	456	468	6	9	25.78125	0	165
4.52	5.42	108	516	RS	516	528	6	10	25.78125	0	165
4.87	5.71	108	514	RS*	514	528	7	10	25.78125	0	165
5.17	5.88	128	513	RS	616	632	8	10	25.78125	0	165
5.17	6.03	87	513	RS	456	472	8	9	25.92773	0.6	165 15/16
5.13	5.93	108	514	RS	514	530	8	10	25.93750	0.6	166
4.89	6.14	56	514	RS	286	302	8	9	26.56250	3	170
5.88	6.81	87	513	RS	456	482	13	9	26.56250	3	170
5.96	6.81	107	516	RS	516	544	14	10	26.56250	3	170
6.10	6.92	107	514	RS	514	544	15	10	26.56250	3	170

Assumptions: target BER 1e-15, b=0.5, D [dB] = 0.175 dB

* Z. Wang, H. Jiang and C. Chen, Oct. 2011