FEC Architectural Considerations

P802.3bj Interim
IEEE 802.3
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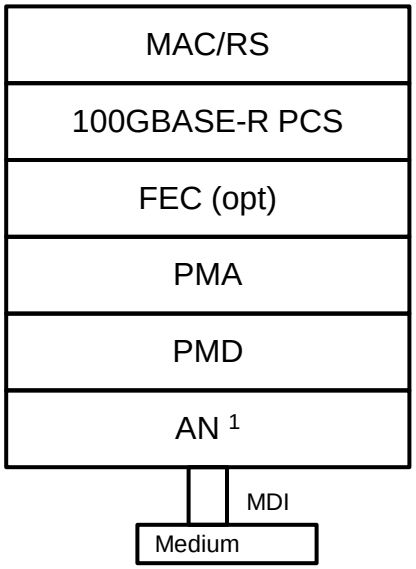
Introduction

- This slide set will explore the architectural impact of FEC in the 802.3ba architecture if a proposal with FEC is selected
- The presentation should not be seen as an endorsement for any proposals that include FEC

Today's 100 Gb/s Architecture

- Below is shown the generic architecture of 802.3ba interfaces, as depicted in Clause 80

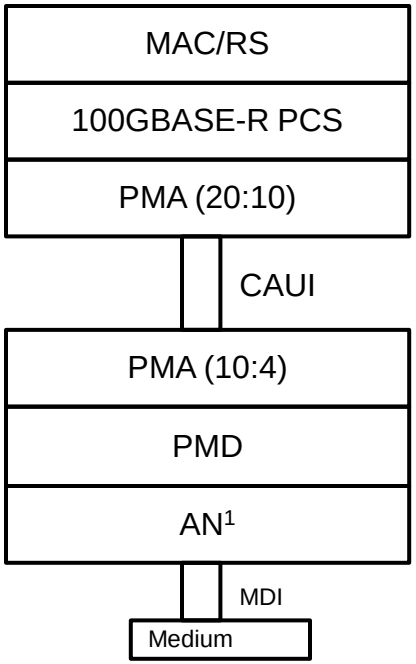


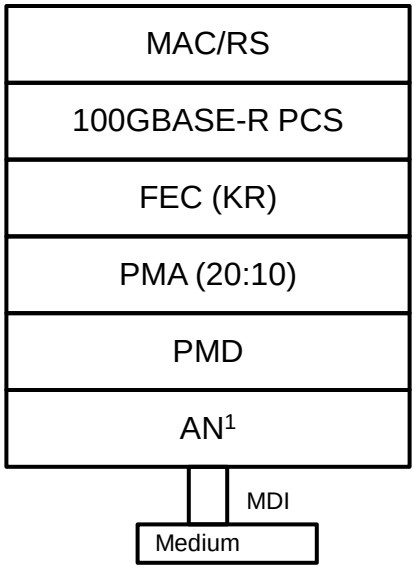
Note 1: Conditional on PMD type and solution chosen

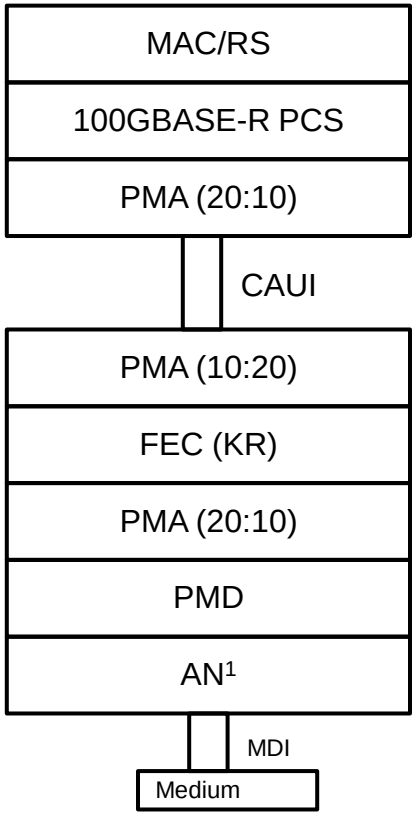
Note 2: FEC in this case is based on PCS Lanes (KR FEC)

Today's 100 Gb/s Architecture

- Many variations of this are possible and are shown in Annex 83C
- Note that the currently defined FEC is KR (Clause 74) based and operates on individual PCS Lanes, so 20 instances for 100 Gb/s



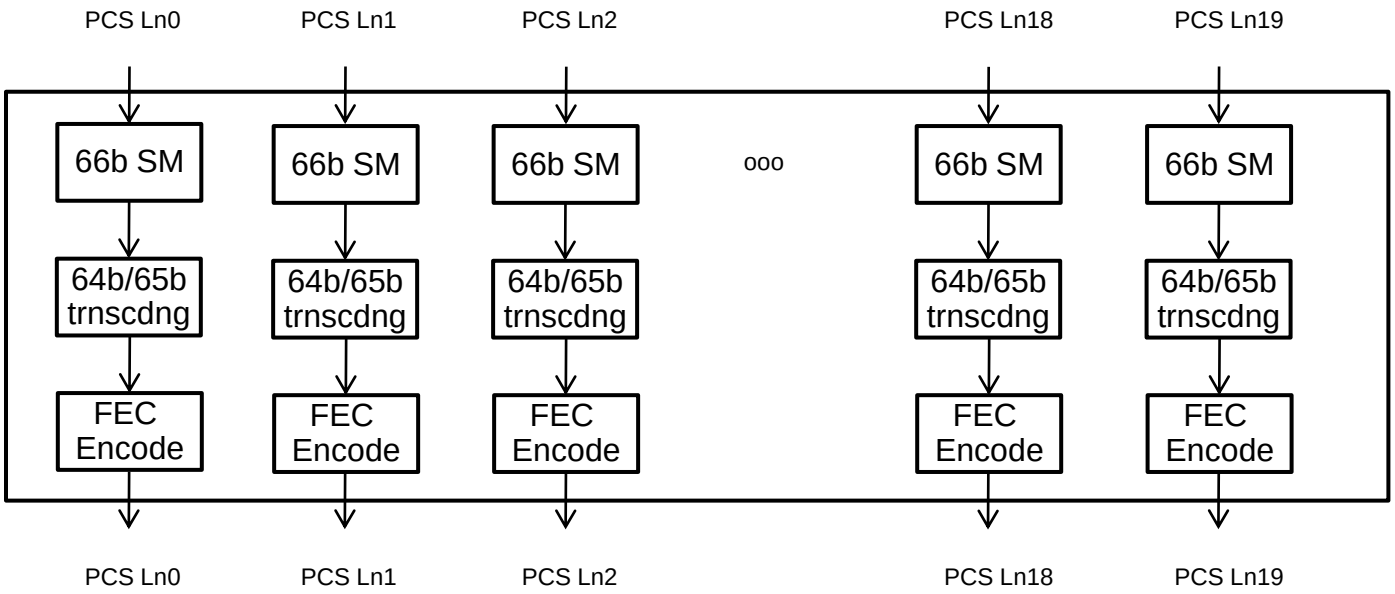




Note 1: Conditional on PMD type and solution chosen

KR FEC Processing

- Below shows the processing for the KR FEC that is part of 802.3ba (everything is done per PCS lane, TX processing is shown):



Low Latency FEC Investigations to Date

- Many different FEC options have been discussed so far within 802.3bj and the copper study group
- Most have looked at Reed Solomon codes in order to achieve good single bit and burst error correction capability
- Most have proposed striping FEC blocks across 4x25G lanes in order to achieve low latency (< 100ns), and re-use Alignment Markers for pre-FEC decode alignment of the 4 lanes

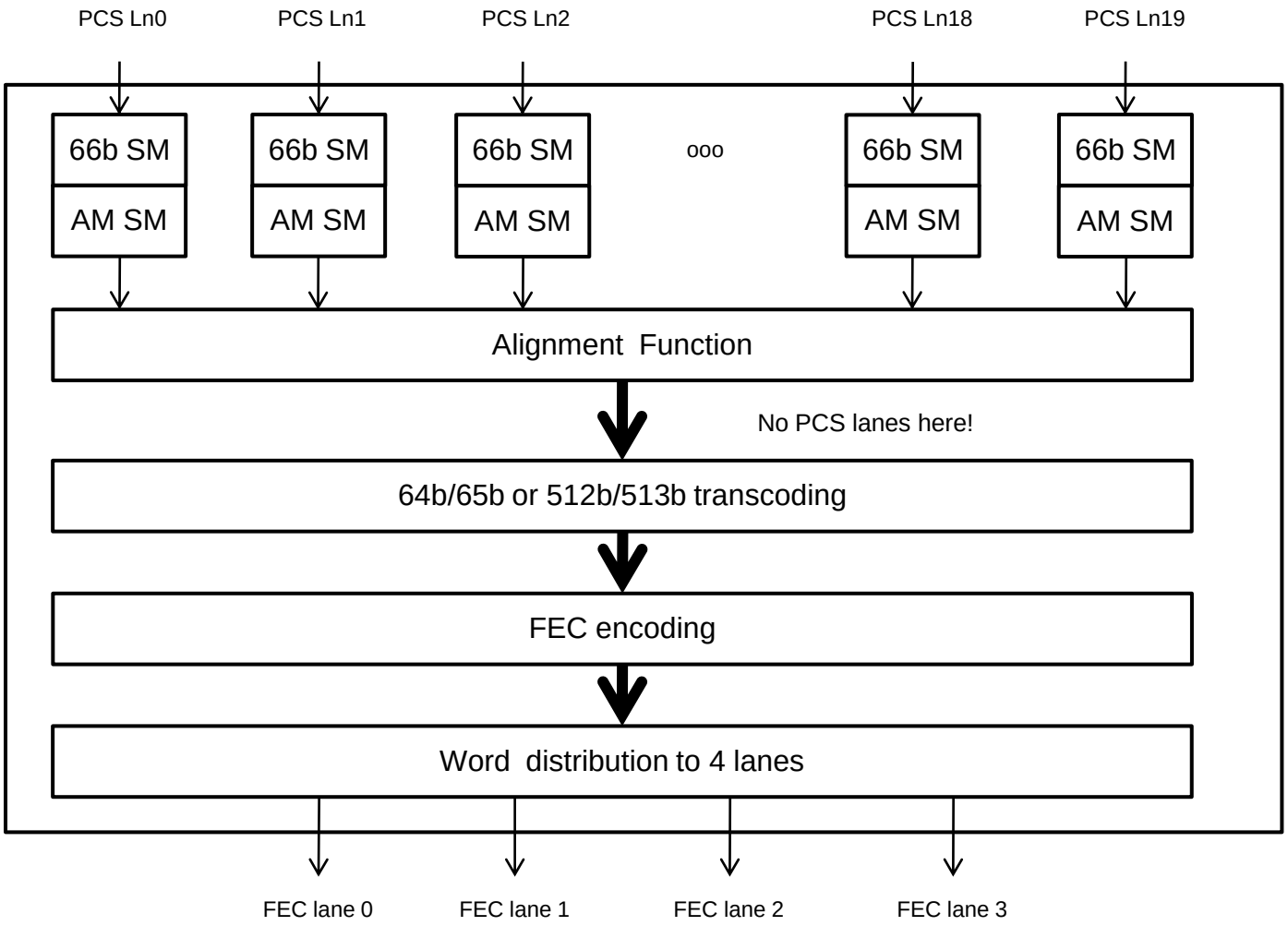
  Would be 4x higher latency if you run FEC per 25G lane
- Investigated proposals range from 0% over-clocking to 9%

  A possible sweet spot for backplanes seems to be around 6% (optimum triple tradeoff point)
- Proposals for 64B/65B and 512B/513B transcoding options so far to reduce the over-clocking

- Architecturally where does this possible new Low Latency FEC fit?

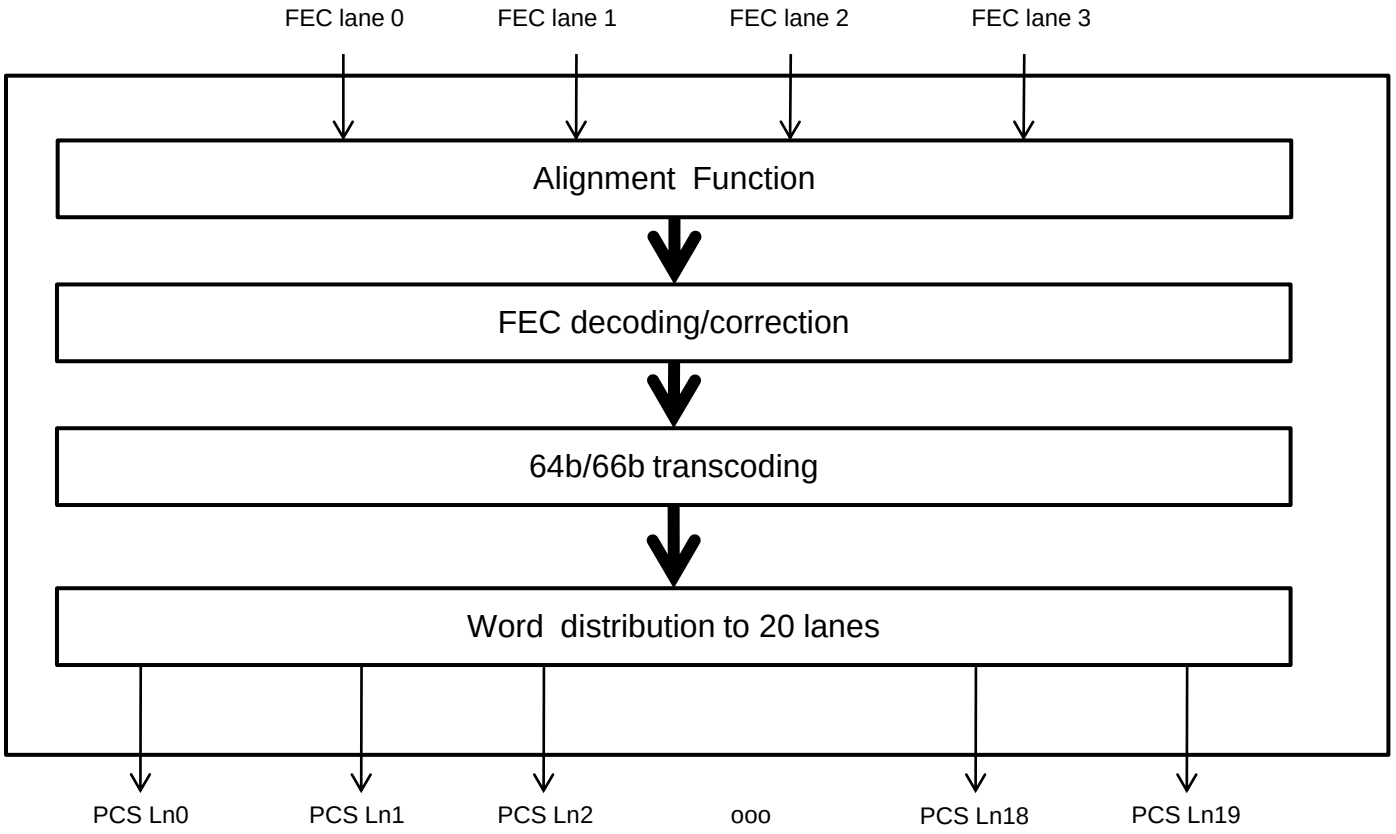
Low Latency FEC Architecture

- Below shows the processing for the FEC options that have been proposed so far (TX side processing):



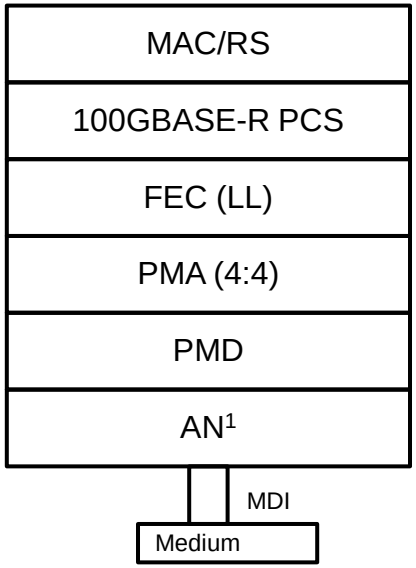
Low Latency FEC Architecture

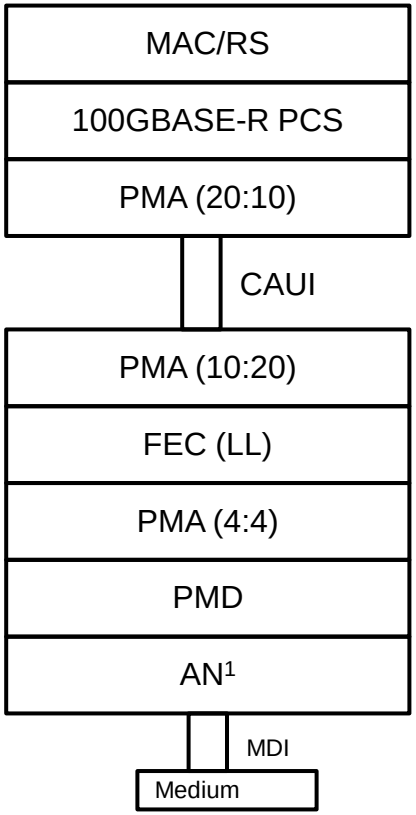
- Below shows the processing for the FEC options that have been proposed so far (RX side processing):

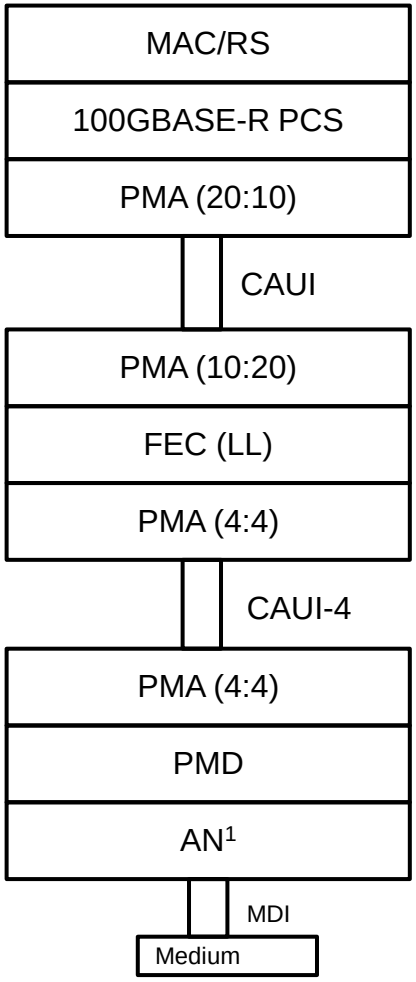


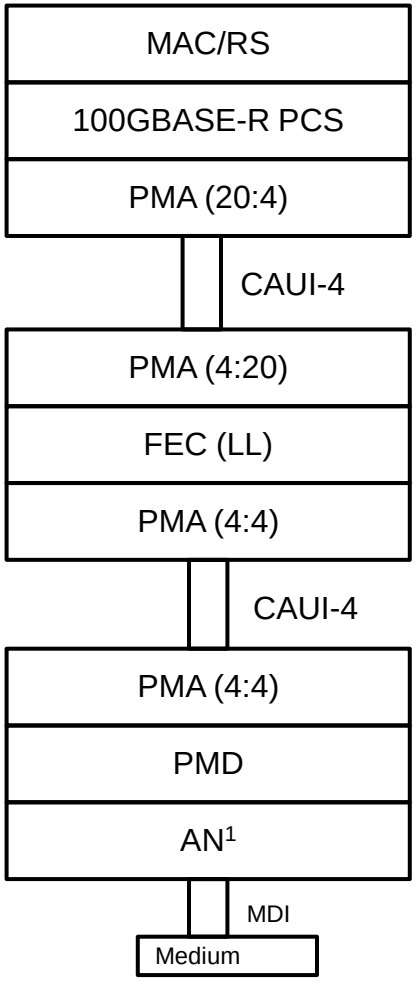
Low Latency FEC Architecture

- The figures below show possible striped (and therefore low latency) FEC architectures









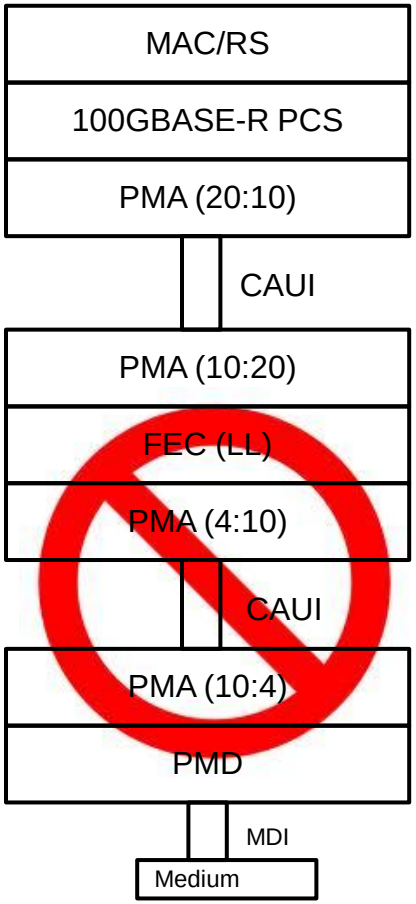
Note 1: Conditional on PMD type and solution chosen

Note: LL = Low Latency

CAUI-4 – assumed new 25G+ interface, might need multiple rates to support FEC

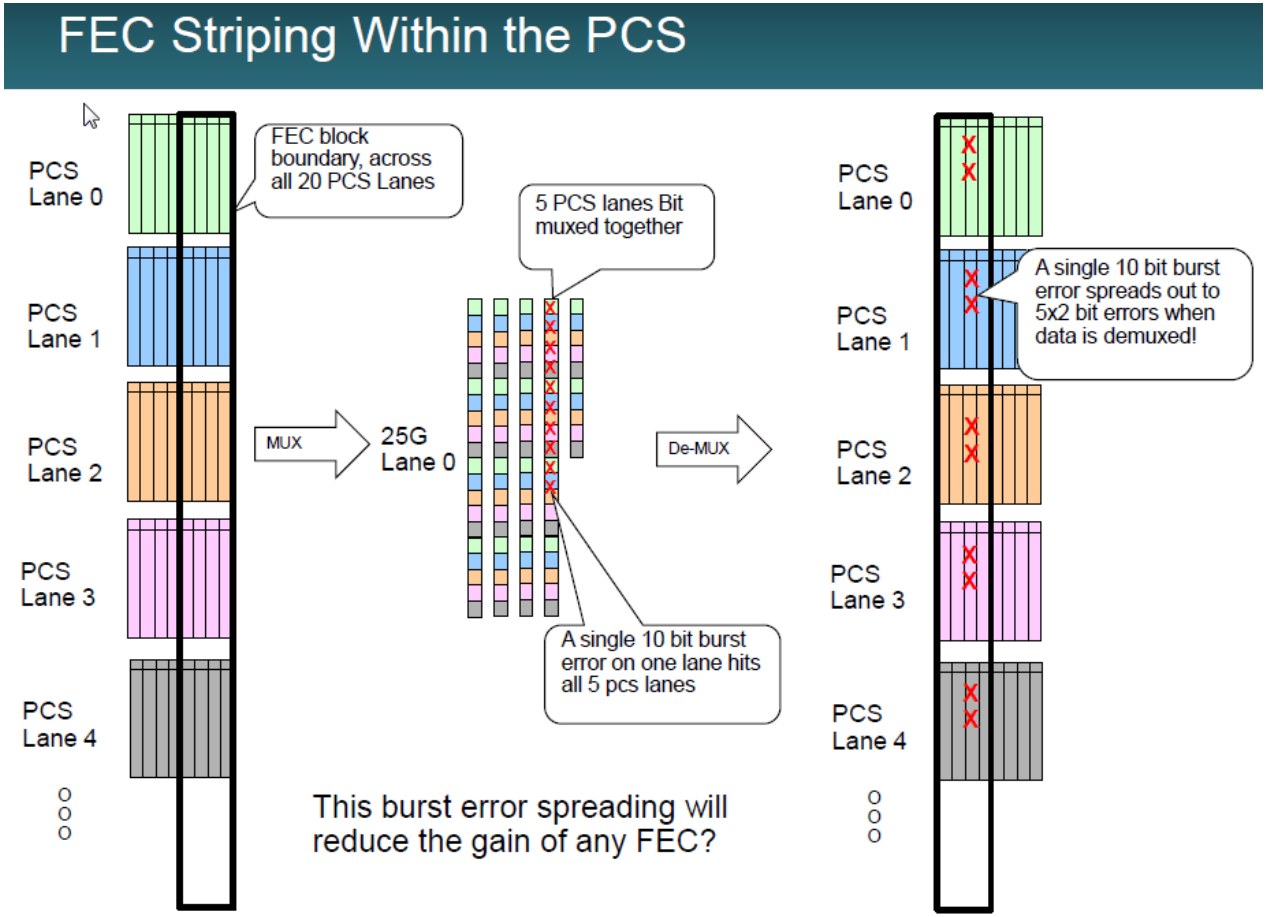
Low Latency FEC Architecture

- The figure below shows an incorrect architecture, once the Low Latency FEC is inserted, the number of lanes cannot change!
  - At least not with the standard 802.3ba PMAs
  - Exploring the possibility of supporting 4, 2 and 1 lane options. But we need to look at burst error behavior.



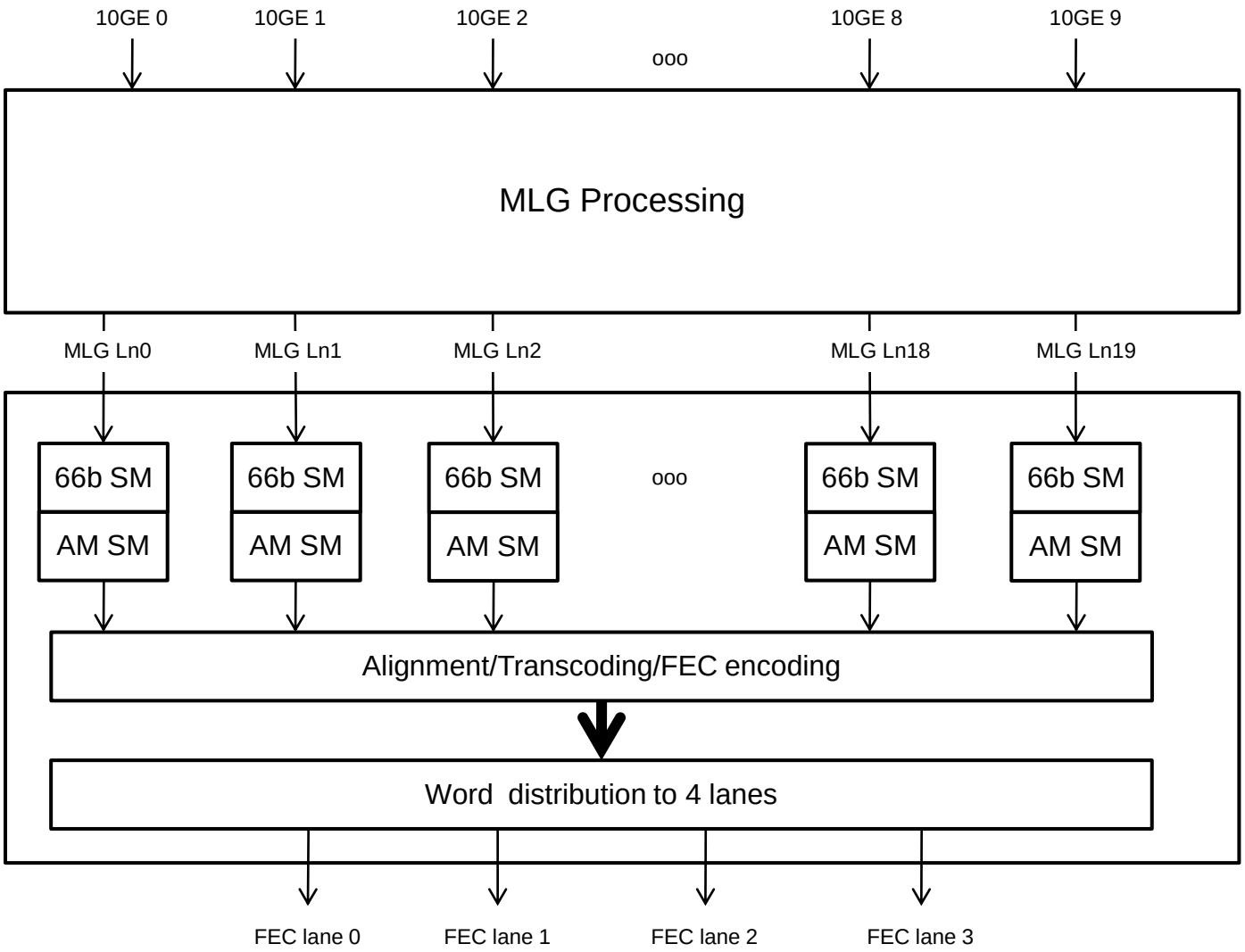
FEC within the PCS Layer

- Why not put FEC into the PCS layer and allow the normal PMA muxing that we do for 802.3ba?
- See gustlin_02_0911, doing this would cause any burst errors to be split up into multiple individual errors and weaken most FEC codes



LL FEC With MLG

- The architecture can support MLG payloads



Summary

- The Low Latency FEC codes that have been discussed so far within 802.3bj can fit cleanly into the 802.3 architecture
- However, the LL FEC codes are point to point codes across 4 lanes, and after the FEC code is inserted, normal 802.3ba bit manipulation cannot take place
- The FEC architecture as presented is flexible and can be modified to support various solutions (i.e. transcoding, FEC gain, lane counts or MLG)

Thanks!