



# **System OEM design guidelines for chip to module interfaces**

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IEEE 802.3bj TF and NG 100G Optical Ethernet SG  
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# Contributors and Supporters

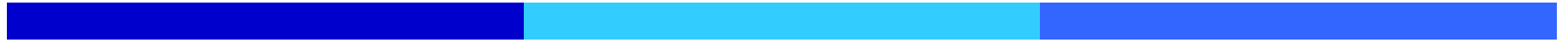
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- Mark Nowell, Cisco
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- Scott Kipp, Brocade
- Jeff Maki, Juniper
- John D'Ambrosia, Dell
- Dan Dove, Applied Micro
- David Warren, HP
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# Topics

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- 1) Reach considerations for chip-to-module electrical interfaces
- 2) Implications of reach considerations for both retimed and un-retimed module interfaces
- 3) Systems considerations related to the inclusion of FEC for NG PMDs



# **Reach Considerations for chip-to-module electrical interfaces**

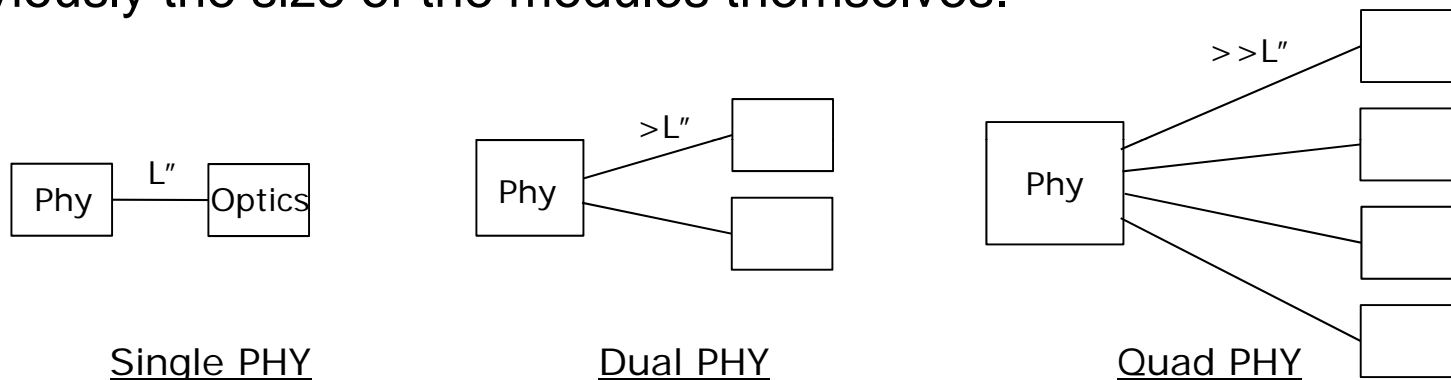
# Background

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- There have been discussions within the Next Generation 100Gb/s Optical Ethernet Study Group around two new 4 lane chip-to-module electrical interfaces and possible objectives:
  - CAUI-4 (4x25G retimed)
  - CPPI-4 (4x25G un-retimed)
- One of the key discussion points around any electrical interface is the (minimum) host reach requirements
- This presentation leverages previous IEEE and OIF contributions, to provide some basic system OEM guidelines for the host (PCB) reach requirements of any new chip-to-module electrical interface.

# Host Distance Requirements

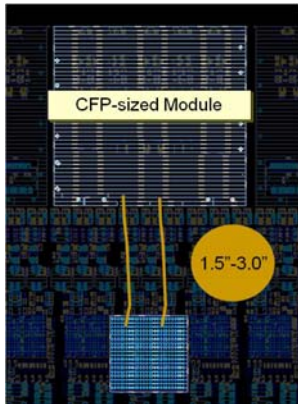
- A key consideration for chip-to-module distance requirements is related to the number of modules that need to be directly connected to a single host chip (be that a PHY, MAC, Framer, etc), and obviously the size of the modules themselves.



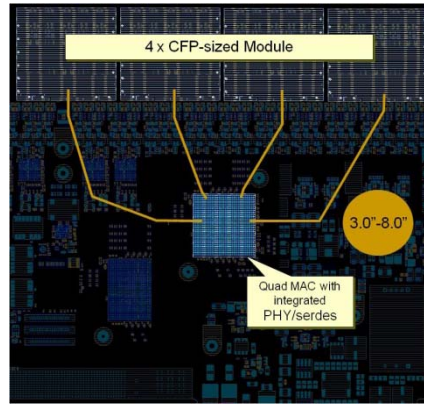
- Implementations tend to start with a single phy solution, but migrate to higher order PHYs over time, to meet density demands.
- Often to move to higher order PHYs is accompanied with a move to the next gen (smaller) module form factor
- As a general rule any new chip-to-module interface should support, as a minimum, evolution to a Quad PHY implementation

# 802.3ba – nAUI/nPPI recap

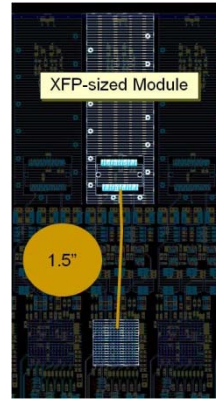
- Distances for nAUI/nPPI were primarily driven out of [nicholl\\_01\\_0708](#)



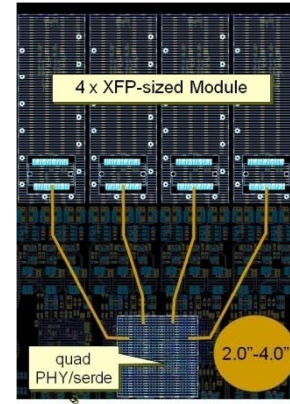
1 port CFP



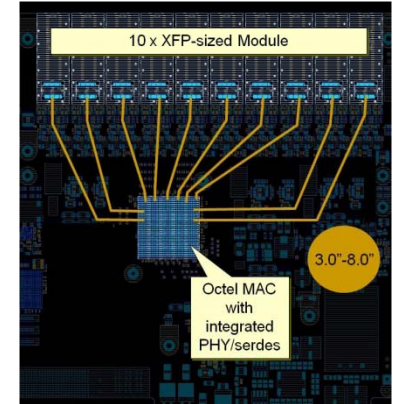
4 port CFP



1 port 'XFP'



4 port 'XFP'



8/10 port 'XFP'

## CFP sized module (Retimed)

1 port: 1.5" - 3"  
4 port: 3.0" - 8.0"

## CXP/QSFP sized module (Unretimed)

1 port: 1.5"  
4 port: 2.0" - 4.0"  
8 port: 3.0" - 8.0"

- In keeping with the 'Quad Phy' rule-of-thumb, 802.3ba targeted 8" for nAUI (retimed) and 4" for nPPI (unretimed)

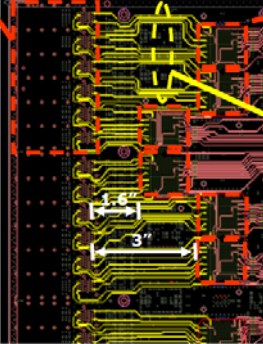
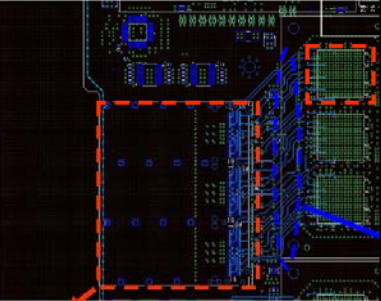

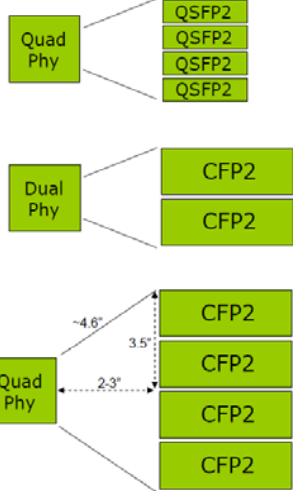
# OIF CEI-28G-VSR Activities

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- The OIF kicked off the CEI-28G-VSR project in Jan/10.
- The project was aimed at defining a 4 lane electrical interface for use with next generation 100G optical modules
- One of the underlying goals of the project, was that the work could (would) eventually be picked up by a future IEEE study group as the basis for a CAUI-4 chip-to-module interface.
- A lot of the same discussions arose as in 802.3ba, relating to the (minimum) host reach requirements
- The following slides (taken from OIF2010.132.01) were submitted to help the group define:
  - ❖ Host distance requirements (primarily driven by component placement and routing)
  - ❖ Channel loss requirements



# OIF2010.132.01 - Distance Analysis

SFP+ Example (n port)	QSFP Example (n port)	28G VSR Example (Gen 1)	28G VSR Example (Gen 2)
<p>Stacked (2x6), SFP+ cage</p>  <ul style="list-style-type: none"> <li>• Example of a high density</li> <li>• One Phy chip connected</li> <li>• The longest routed net is around a power block).</li> </ul>	<p>1 x 3, QSFP cage</p>  <ul style="list-style-type: none"> <li>• Example of a lower density line card</li> <li>• One Phy chip connected to one (no)</li> <li>• Longest trace is 2.2"</li> </ul>	 <ul style="list-style-type: none"> <li>• Preliminary placement analysis for</li> <li>• A single PHY (10:4 gearbox) con</li> <li>• Longest trace is estimated to be</li> <li>• Expected to represent the minimum</li> </ul>	 <ul style="list-style-type: none"> <li>• Quad Phy to 4 x QSFP2</li> <li>• Same as "nicholl_01_0708.pdf"</li> <li>• 4" should be sufficient</li> <li>• Dual Phy to 2 x CFP2</li> <li>• essentially the same as above</li> <li>• 4" should also be sufficient</li> <li>• Quad Phy to 4 x CFP2</li> <li>• trace length &gt; 4"</li> <li>• not supported by 28G-VSR ?</li> </ul>

## Channel Distance Recommendation

Based on:

1. A review of existing channel lengths on shipping product (all be it at lower rates)
2. A review of the nPPI objectives and associated analysis in .ba, and
3. A preliminary placement analysis on several 100G QSFP2 / CFP2 applications

We recommend the following target channel distances:

Min Channel distance = 0.8 "

Max Channel distance = 4 "

## Conclusion:

- Similar analysis to [nicholl\\_01\\_0708](#) performed, looking at both CFP2 and CFP4/QSFP2 form factors
- Again based on 'Quad Phy' rule a target distance of 4" was chosen


# Distance versus Loss

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- To define the electrical specification, the distance requirement must first be mapped to a channel loss requirement
- This mapping is obviously dependent on a number of parameters and assumptions, such as PCB material, stripline versus microstrip, connector loss, etc
- 😊😊 More debate and discussion 😊😊
- General philosophy is that the distance to loss mapping used in defining a standard, should be based on typical (mainstream) design approaches:
  - ❖ A poor design using higher loss board materials will likely not meet the distance requirement.
  - ❖ A state-of-the-art design, using state-of-the-art board materials and connector technologies, will likely exceed the minimum distance requirements by a significant margin

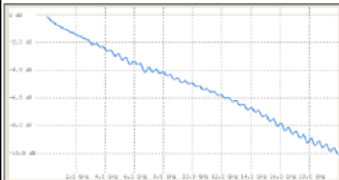
# OIF2010.132.01 – Loss Analysis

### PCB Material Loss Analysis




Real channel (with via)

- To evaluate the channel loss we considered real channel lengths taken over several different lengths (4", 6", 8", and 10") on Megtron4 and 6 material (some of the via effects too).
- A min-Max PCB frequency loss was then extracted (to account for via contribution where appropriate).



MEG4\_DIFF\_6INCH loss (no via)



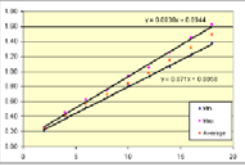
MEG6\_DIFF\_6INCH loss (no via)

### PCB Material Loss Summary

Channel PCB min-Max formulas directly extracted from channel measurements

Meg4: 4, 6, 8, 12 and 16 inches


Freq (GHz)	Megtron 4		Megtron 6	
	Min	Max	Min	Max
4	0.52	0.50	0.19	0.20
6	0.58	0.63	0.43	0.41
8	0.65	0.70	0.52	0.54
10	0.69	0.74	0.63	0.61
12	0.72	0.78	0.70	0.72
14	0.76	0.82	0.78	0.80
16	0.78	0.83	0.83	0.82



Extracted min-Max loss formula

Channel blocks: PCB formula and losses @14GHz (dB)	MEG4	MEG6
Loss/inch min	1.1	1.3
Loss/inch Max	1.1	1.3

### Channel Loss Budget Analysis



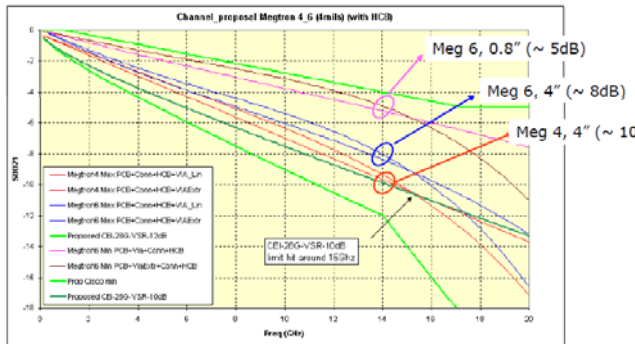
Emulated channel (2 via losses considered)

We then emulated the end-to-end channel loss for both a 0.8" (min) and a 4" (max) host trace length as follows:

- Host PCB loss based on extrapolation from measured data
- Two approaches considered to account for Via loss
  - Direct extrapolation (frequency) from measurements
  - Linear loss (1dB at 14GHz), taken from OIF2010.112.01
- Connector loss considered linear (1.5dB @14GHz), taken from OIF2010.112.01
- HCB loss (2.1dB @14GHz), also taken from OIF2010.112.01

Extrapolated channel loss from measured data on different board materials

### Loss Budget Summary



Channel proposal Megtron 4, 6 (trails) with HCB

Meg 6, 0.8" (~ 5dB)  
 Meg 6, 4" (~ 8dB)  
 Meg 4, 4" (~ 10dB)

- 10dB budget is close to meeting the requirements for a 4" host trace
  - ~ 2 dB margin when using Meg 6
  - ~ 0 dB margin when using Meg 4

### Conclusion:

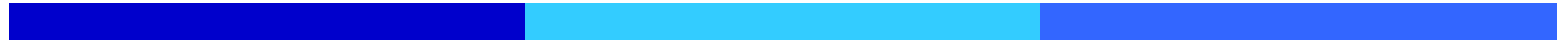
10dB (@14G) is a good candidate proposal to meet a 4" host channel:

- ~ 2dB margin for Meg 6
- ~ 0dB margin for Meg 4

# Summary – Host Reach Considerations

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- Recommend targeting a (minimum) distance of 4” for any next gen, 4 lane chip-to-module interface.
- Recommend that a loss budget of 10dB (@ Nyquist) is a good starting objective for a chip-module electrical channel targeting a host distance of 4” (note, this includes host PCB trace loss + connector loss + module PCB trace loss)..



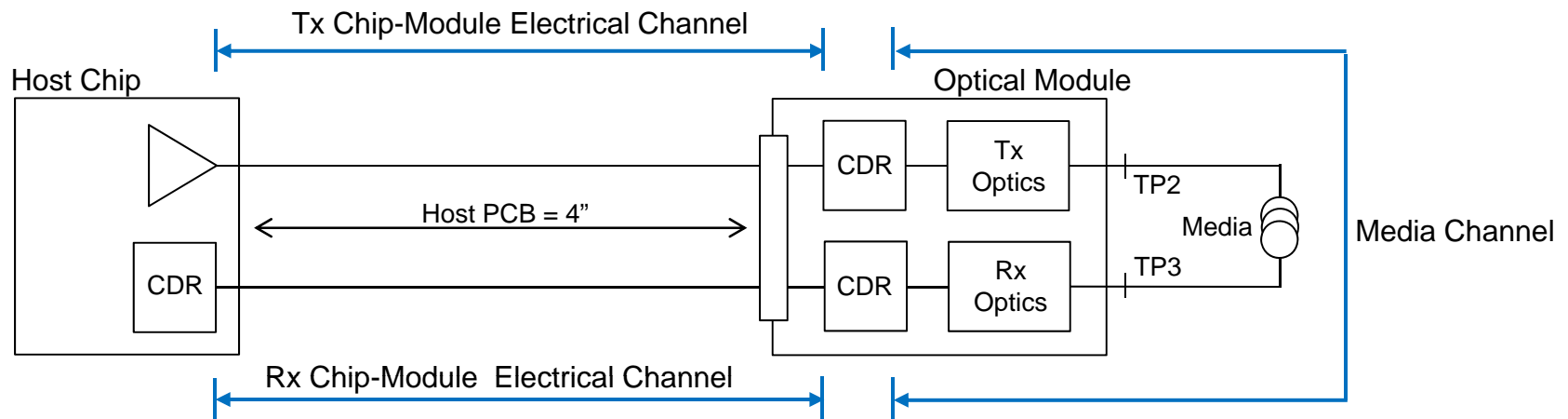
# **Implications of host reach for both Retimed and Un-retimed optical module interfaces**

# Background

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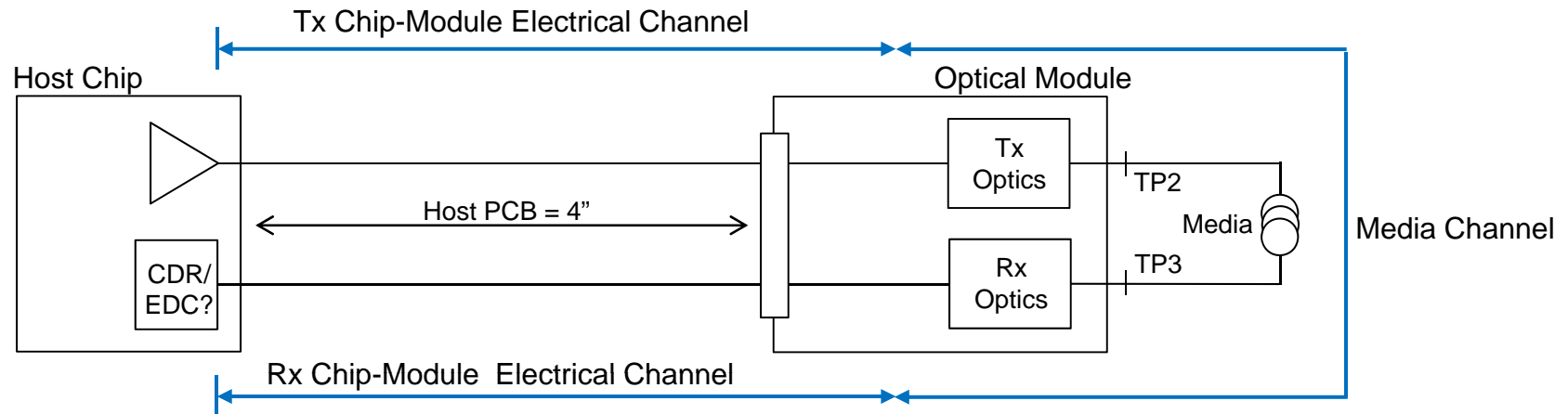
- If/once we agree to define a chip-to-module electrical interface, we need to separately consider the implications for:
  - 1) Retimed interface (CAUI-4 ?)
  - 2) Un-retimed interface (CPPI-4 ?)

# Retimed Module Interface



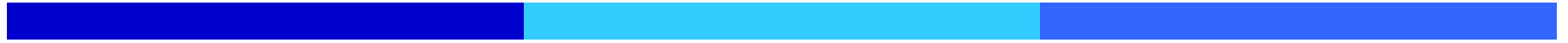
- Chip-Module electrical channel is symmetrical (Tx – Rx)
- Chip-Module electrical channel is essentially decoupled from media channel (can therefore be defined independently)
- Can leverage OIF-28G-VSR work, as evidence for technical and economic feasibility
- Recommend a 10dB (@ Nyquist) loss budget for a retimed chip-module electrical channel (CAUI-4)

# Un-retimed Module Interface



- No clear demark between chip-module electrical channel and media channel. Cannot define chip-module electrical channel in isolation from media channel (reach)
- Host chip must accommodate 2 x chip-module channel + media channel (e.g. 2 x 10dB + media channel loss)
- Need to define target PMD reach objectives(s), to assess a un-retimed module interface





# **FEC Considerations for next gen PMDs**

# Background

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- FEC is one option being considered to address reach requirements for some of the next gen PMDs (e.g. SR4)
- Some discussion about extending FEC to other PMDs, and potentially to legacy PMDs such as 100GBASE-LR4, etc (thereby potentially creating FEC and non-FEC versions)

# FEC Considerations

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- From a system vendor perspective FEC is not 'free'.
- A decision to introduce FEC should not be taken lightly.
- There are a number of system issues/implications to consider, not least of which is compatibility with 40GE/100GE ports already shipped (e.g. if a new PMD requires FEC how would it be supported on a 'legacy' platform which does not implement FEC?)

# FEC Recommendations

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If the group believes that FEC is ultimately required, then the following guidelines should be adhered to:

- If FEC is required for a new PMD, then it should not raise any (media) interop issues due to options.
- No proliferation of existing PMDs due to FEC variants.
- Solutions should be compatible with existing host designs supporting currently defined PMDs.

# Next steps

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- Recommend the development of a retimed chip-to-module interface (CAUI-4)
  - 10dB (@ Nyquist) loss budget
  - Leverage OIF CEI-28G-VSR
- Pending agreement on optical reach objectives, further contributions are required regarding technical and economic feasibility of an un-retimed chip-to-module interface.

# References

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- nicholl\_01\_0708: 'Distance Requirements for XLAUI/CAUI and PMD Service Interface'  
[http://www.ieee802.org/3/ba/public/jul08/nicholl\\_01\\_0708.pdf](http://www.ieee802.org/3/ba/public/jul08/nicholl_01_0708.pdf)
- OIF2010.132.01: 'VSR Channel Distance and Loss Budget'

Note: As the author for OIF2010.132.01, I will make it available upon request.