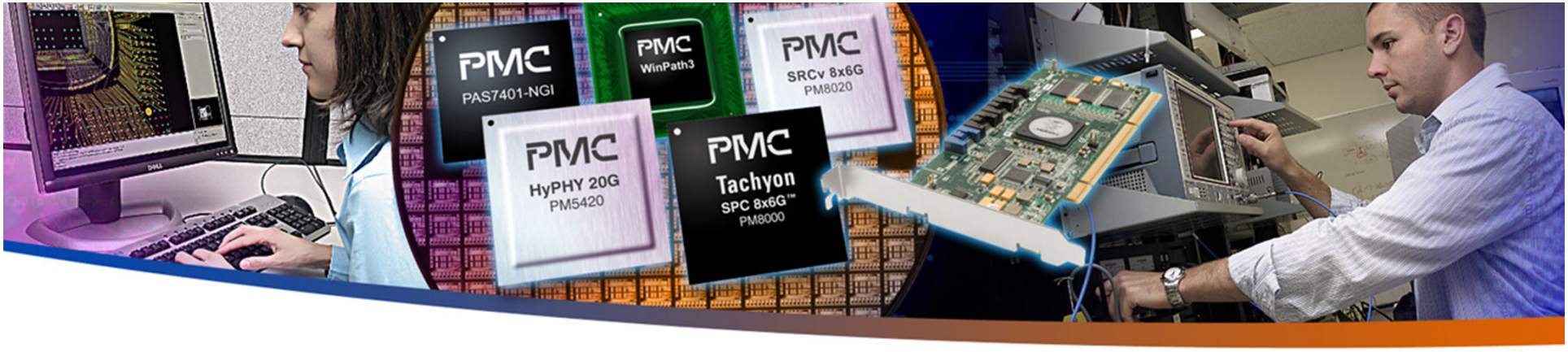

FEC Requirements for 100Gb/s Backplane and Copper Cable

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Supporters

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- Stephen Bates, RAD3 Communications
- Mark Gustlin, Cisco Systems

- THANK YOU to members of the 802.3bj FEC informal discussion group who provided valuable feedback.

Context

- The purpose of this exercise is to gather requirements information from the channel modelers, to drive the design of the FEC.
  - The actual FEC design will probably not be hard once we know what it has to do.

- The requirements may be met by a combination of FEC, precoding, synchronization, and scrambling

- These requirements are meant to draw a ‘box’ within which the team can explore. It does NOT preclude us specifying something better!
  - E.g. if we agree that Fmax = 28Gbps, but we find a workable solution with 26.5 Gbps, the final spec will be 26.5Gbps.

Draft Requirements for FEC + Line Code

	Requirement *(Implications)*	Proposed Value(s)	Status
1.1	Must not require more than **Lmax** latency at its full coding gain.	100 ns	Agreed
1.2	Should allow a latency adder less than **Lmax_NoFG** when no coding gain is required. *(Affects whether we can have just one Tx format, with Transcode & FEC bits, and only vary the Rx.)*	20ns	Does this need to be super-small?
2.1	Must not require a SERDES speed greater than **Dmax**. *(No greater than OTN)*	28 Gbps	Recommended
2.2	Must allow a SERDES speed equal to **Dmin** when no coding gain is required *(Affects whether we can have just one Tx format, with Transcode & FEC bits, and only vary the Rx.)*	"No req" or "25.78 Gbps"	Discuss.
2.3	Must carry a data rate not less than **Cmin** at its maximum coding gain	100Gpbs	Agreed

Draft Requirements for FEC + Line Code

	Requirement *(Implications)*	Proposed Value(s)	Status
3.1	Must reduce an AWGN input **BER_in** to a BER_out of 1E-12 or less. *(An important starting point. Detailed error models can be contentious, and will take time)*		**Request Input**
3.2	Must provide a Total Coding Gain of **TCG_A, TCG_B, TCG_C** under error models A,B,C at a BERout = 1E-12. *(Running sims vs. 20 channel models is not practical. We need to pick about 3-5. At least one should be Coax.)*		**Request 3 Error Models**
3.3	Must not have an appreciable error flare or floor above BERout = 1E-15 under AWGN, or under Error Models A, B, C. *(Many practical applications must be operated far below 1E-12. Analysis and emulation will be required to show a high likelihood that 3.3. is met)*	No Flare	**Request 3 Error Models**

Draft Requirements for FEC + Line Code

	Requirement	Proposed Value(s)	Action Sugg.
4.1	Must correct the worst burstiness event (bursts + ambient) that occurs with with **Pburst** likelihood on a single channel *(Burst error impact is Pburst * BurstLength, so Pburst < BERout/BurstLength is required)* *(Likely to be strongly driven by DFE error propagation. Differential coding may satisfy this.)*	1E-14 minimum. 1E-17 preferred.	**Derive from channel models.**
4.2	Must correct a burst of **Bml** bits on all lanes simultaneously, which is the maximum burst occurring with Pburst likelihood. *(Solution must be robust to card pull, power-supply, or correlated crosstalk events. This requirement strongly affects striping, and trades off against 4.1)*		**Consult board experts.**
5.1	Reasonable Power consumption (precise requirement needs more discussion)		Discuss

Request for Input

- Are these the right requirements?
- Are members willing to provide representative error models?