CEI-28G-VSR

Channel Distance and Loss Budget Requirements

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Acknowledgements

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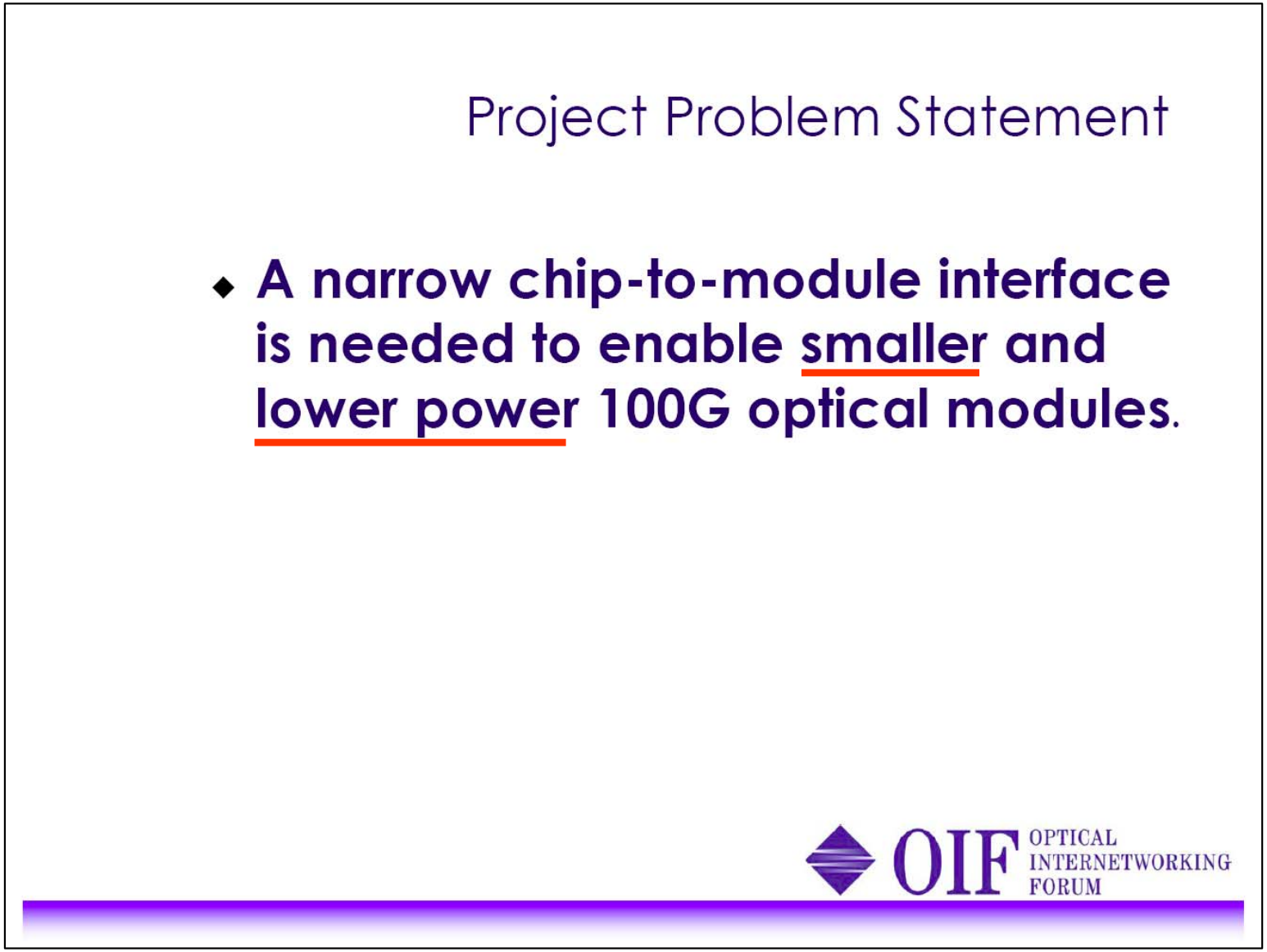
Topics

- Channel Distance Requirements
  - Review (confirm) VSR target channel distance(s)
  - Primarily driven by component placement and routing considerations
- Loss Budget Requirements
  - Review some measured PCB loss data for different board materials (Meg4 and Meg6)
  - Review current VSR loss budget proposal(s) (OIF2010-112.01), in conjunction with the measured PCB loss data

Background

Recapping the CEI-28G-VSR Project Proposal (OIF2010.068.01)

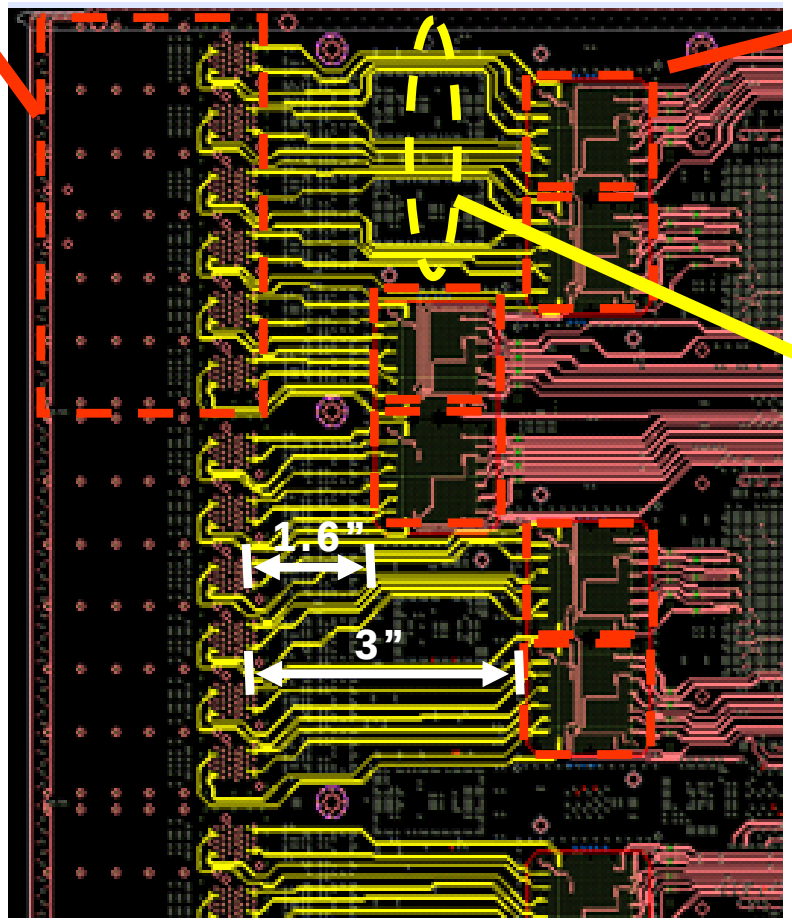


Channel Distance Requirements

SFP+ Example (n port SFP+ board)

Stacked (2x6), SFP+ cage

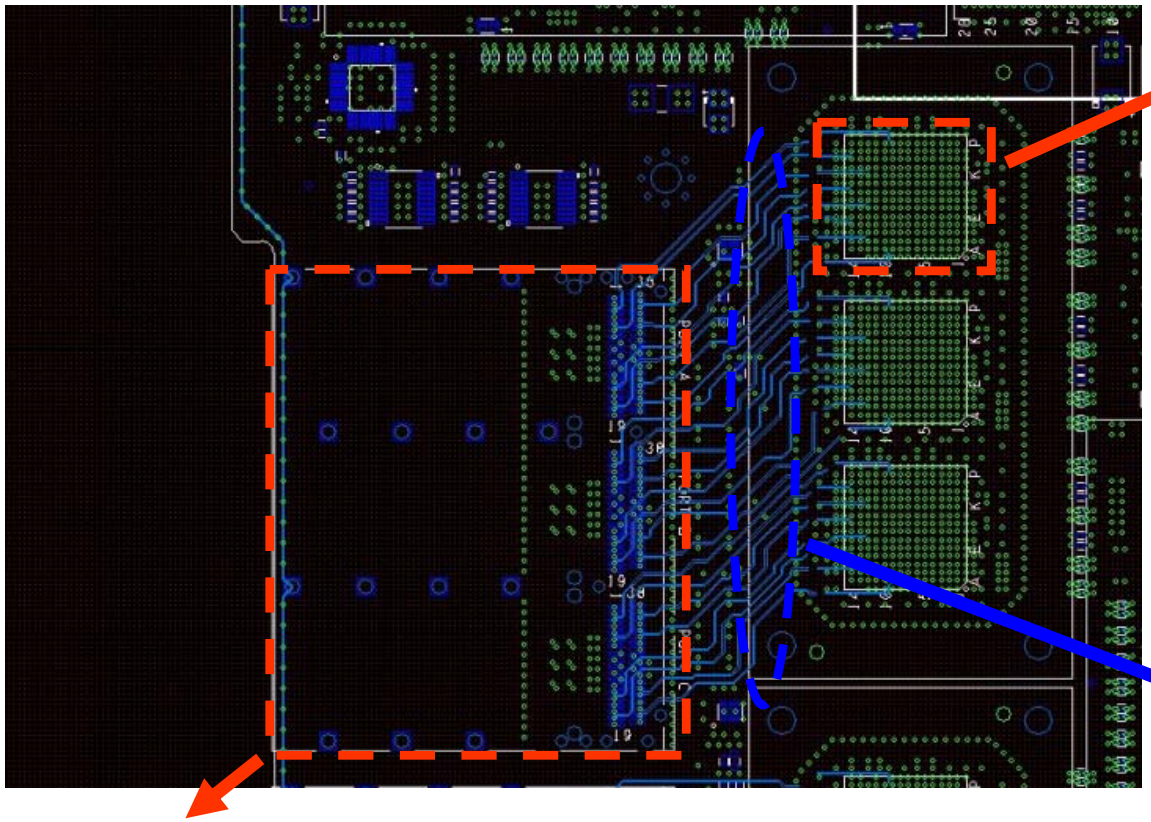
Quad 10G Phy (21mmx21mm)



Longest Trace = 4.4”

- Example of a high density (SFP+) line card design
- One Phy chip connected to 4 x (stacked) SFP+ modules
- The longest routed net is 4.4inches (in this case it is wiggled around a power block).

QSFP Example (n port QSFP board)



- Example of a lower density line card
- One Phy chip connected to one (non-stacked) optics module
- Longest trace is 2.2”

802.3ba nPPI Example

http://www.ieee802.org/3/ba/public/jul08/nicholl_01_0708.pdf

Results

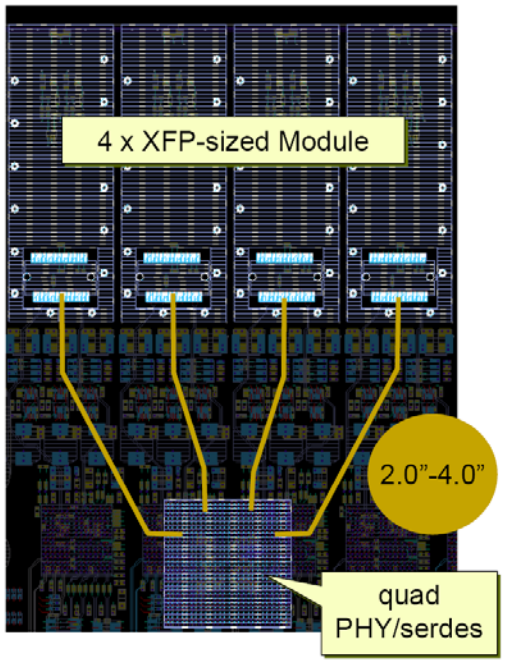
CFP sized optical modules (likely 1st gen)

- 1 port MAC/PHY chip: 1.5" - 3"
- 4 port MAC/PHY chip: 3" - 8"

XFP/QSFP/POD sized optical modules

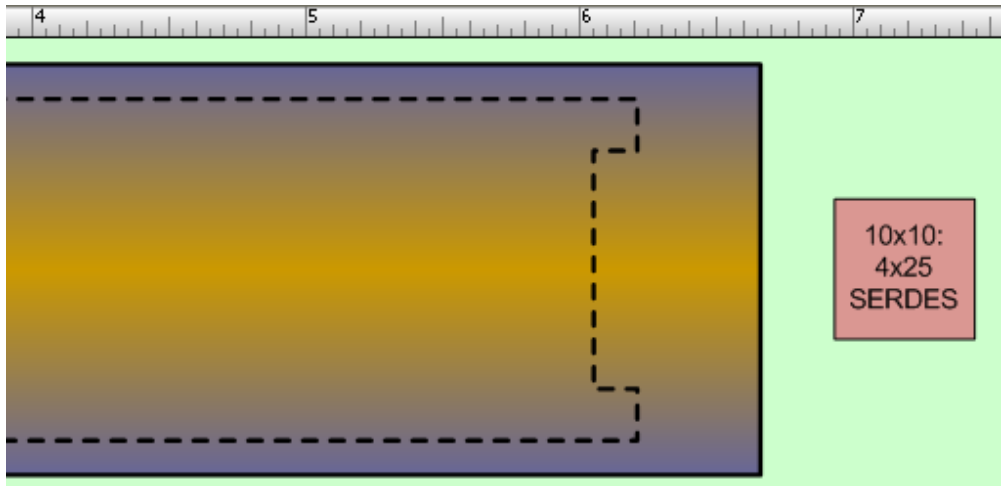
- 1 port MAC/PHY chip: 1.5"
- 4 port MAC/PHY chip: 2" - 4"
- 8 port MAC/PHY chip: 3" - 8"

3



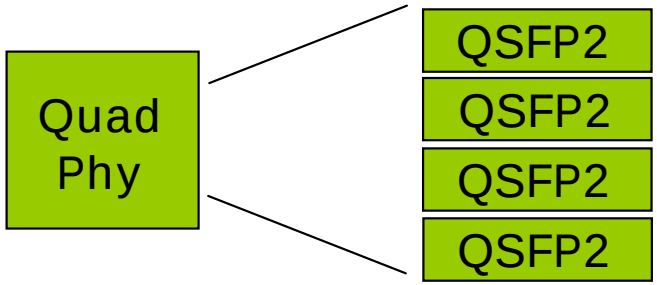
- nPPI target distance of 4" was based on a Quad Phy driving 4 x XFP/QSFP sized optical modules
- By direct analogy then 4" should be sufficient for a Quad Phy driving 4 x QSFP2 modules, and a Dual Phy driving 2 x CFP2 modules (CFP2 is ~ 2x width of QSFP2).

28G VSR Example (Gen 1)

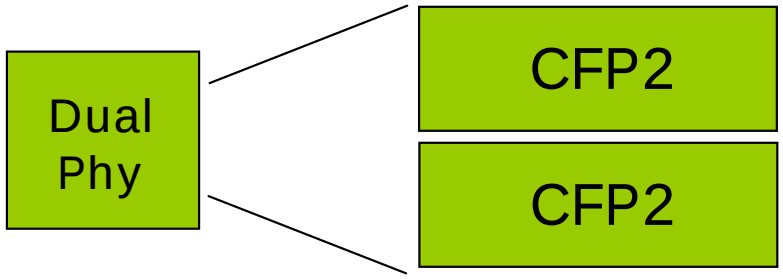


- Preliminary placement analysis for a next gen 100G application
- A single PHY (10:4 gearbox) connected to single “CFP2” optics
- Longest trace is estimated to be ~ 0.8”
- Expected to represent the minimum host trace length for 28G-VSR

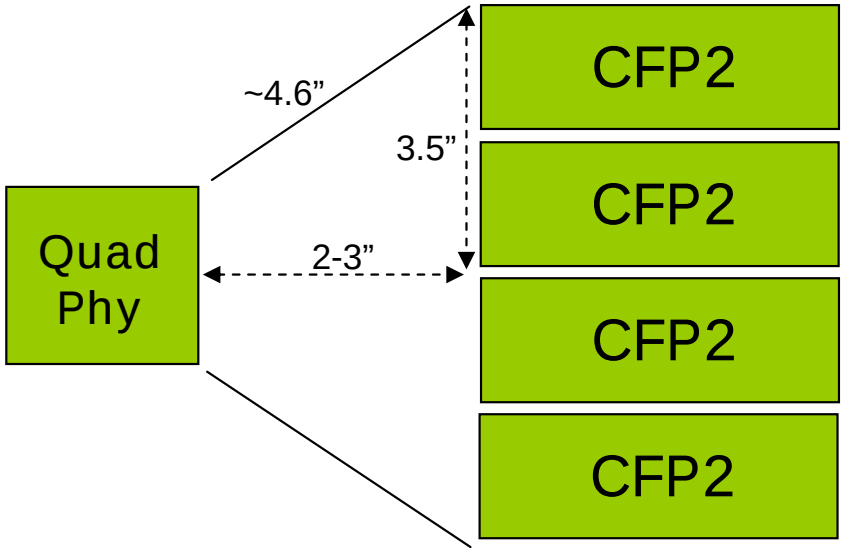
28G VSR Example (Gen 2)



- Quad Phy to 4 x QSFP2
- Same as “nicholl_01_0708.pdf”
- 4” should be sufficient



- Dual Phy to 2 x CFP2
- essentially the same as above
- 4” should also be sufficient



- Quad Phy to 4 x CFP2
- trace length > 4”
- not supported by 28G-VSR ?

Channel Distance Recommendation

Based on:

1. A review of existing channel lengths on shipping product (all be it at lower rates)
2. A review of the nPPI objectives and associated analysis in .ba, and
3. A preliminary placement analysis on several 100G QSFP2 / CFP2 applications

We recommend the following target channel distances:

Min Channel distance = 0.8 “

Max Channel distance = 4 “

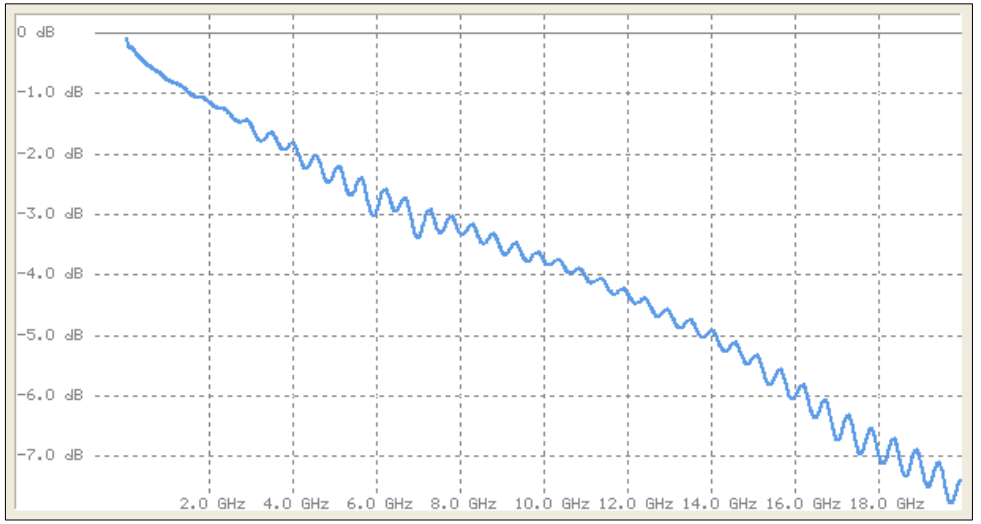
Loss Budget Requirements

PCB Material Loss Analysis

Real channel (with and without via)

- To evaluate the channel loss we considered real measurements taken over several different lengths (4”,6”,8”, etc) of 4mils/width traces on Megtron4 and 6 material (some of these traces including via effects too).
- A min-Max PCB frequency loss was then extrapolated (including via contribution where appropriate).

MEG4_DIFF_6INCH loss (no via)



MEG6_DIFF_6INCH loss (no via)

PCB Material Loss Summary

Channel PCB min-Max formulas directly extracted from channels measurements:

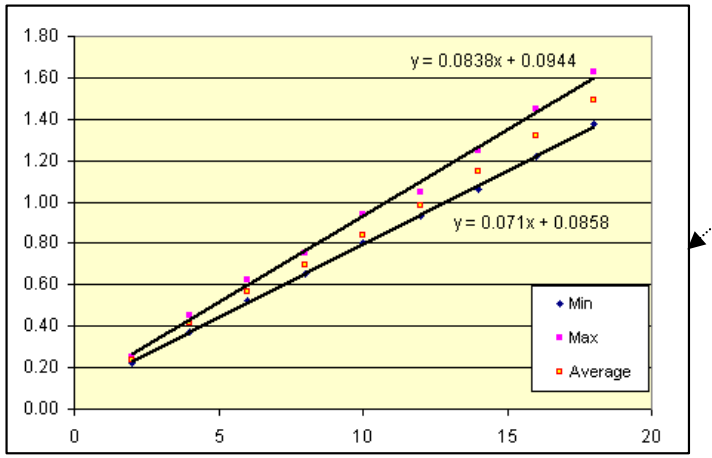
Meg4: 4,6,8,12 and 16 inches

Meg6: 4,6 and 8 inches

meas

meas

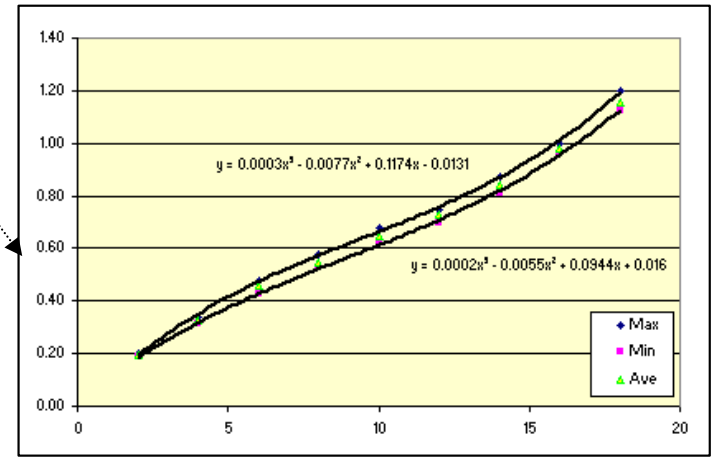
Freq (GHz)	Megtron 4		Megtron 6	
	Min	Max	Min	Max
2	0.22	0.25	0.19	0.20
4	0.38	0.45	0.31	0.34
6	0.53	0.63	0.43	0.48
8	0.65	0.75	0.53	0.58
10	0.80	0.94	0.63	0.68
12	0.93	1.05	0.70	0.75
14	1.06	1.25	0.81	0.88
16	1.22	1.45	0.96	1.00
18	1.38	1.63	1.13	1.20



plots

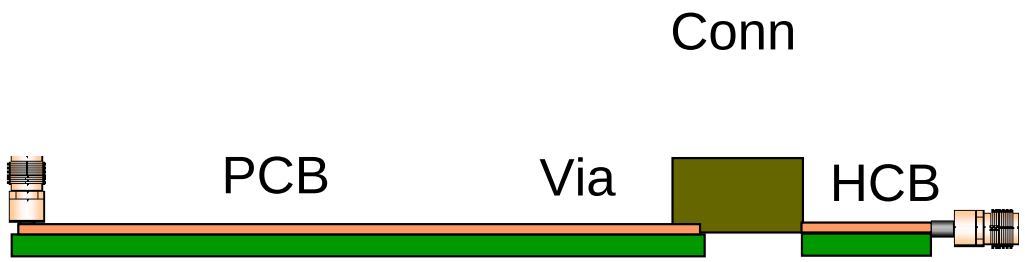
plots

Extracted min-Max loss formula



Channel blocks: PCB formula and losses @14GHz (dB)	MEG4	MEG6
Loss/inch min	1.1	0.8
Loss/inch Max	1.3	0.9

Channel Loss Budget Analysis

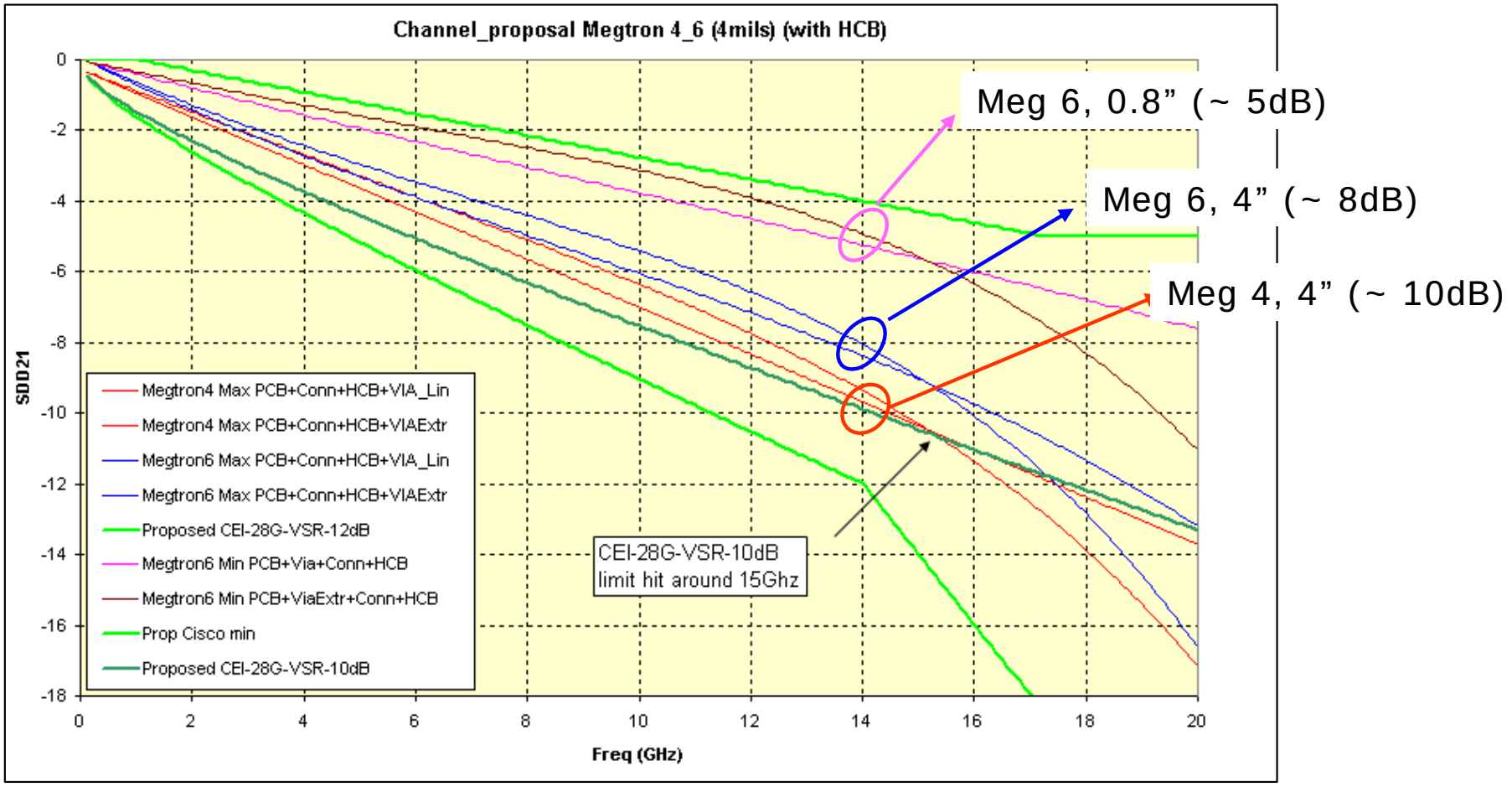


Emulated channel
(2 via losses considered)

We then emulated the end-to-end channel loss for both a 0.8” (min) and a 4” (max) host trace length as follows:

- Host PCB loss based on extrapolation from measured data
- Two approaches considered to account for Via loss
  1. Direct extrapolation (frequency) from measurements
  2. Linear loss (1dB at 14GHz), taken from OIF2010.112.01
- Connector loss considered linear (1.5dB @14Ghz), taken from OIF2010.112.01
- HCB loss (2.1dB @14GHz), also taken from OIF2010.112.01

Loss Budget Summary



- 10dB budget is close to meeting the requirements for a 4" host trace
  - ~ 2 dB margin when using Meg 6
  - ~ 0 dB margin when using Meg 4

Summary

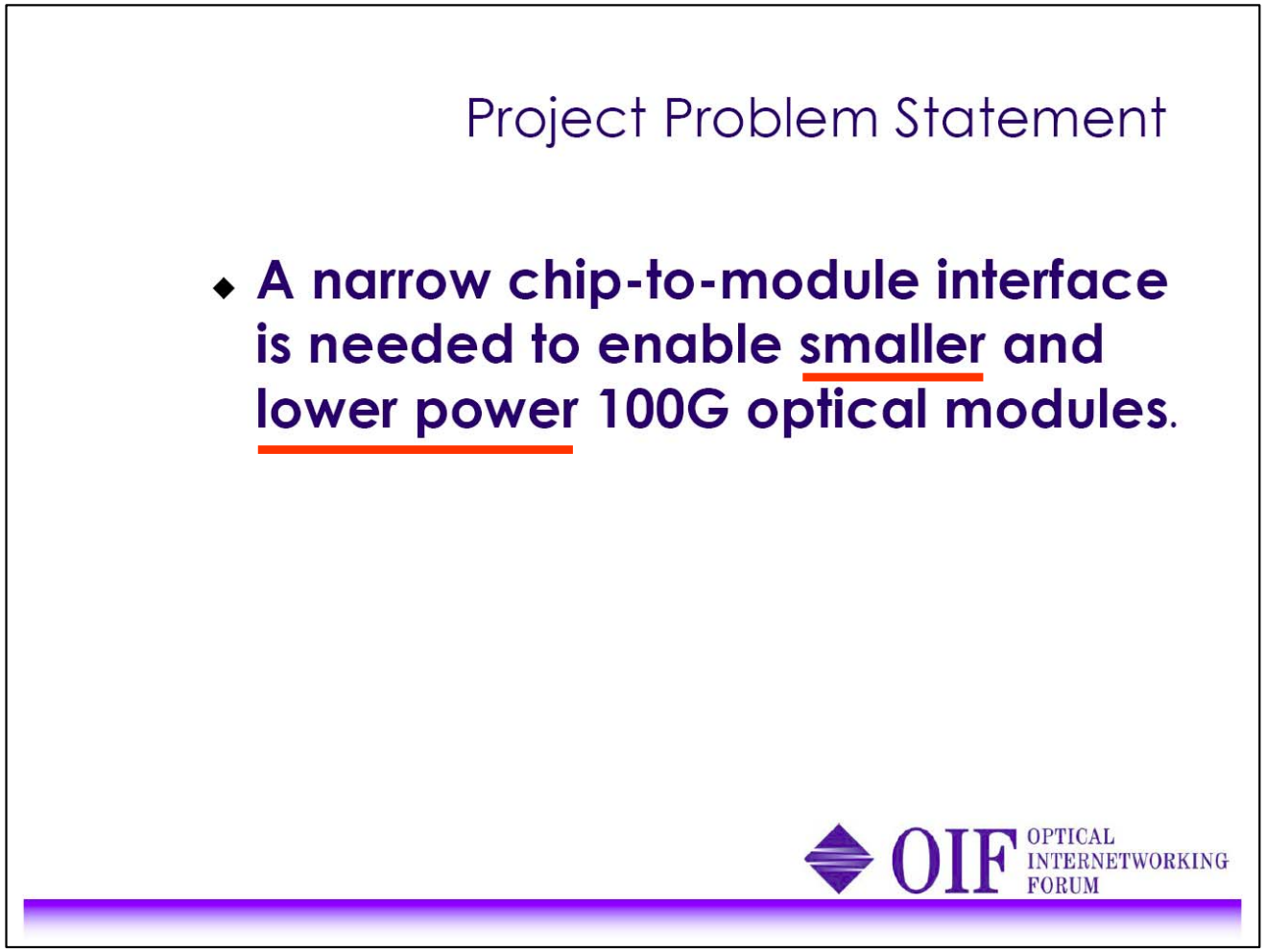
- We recommend that the OIF-28G-VSR project target a host PCB channel length of between 0.8” (min) and 4” (max)
- A 10dB loss budget would appear to be a good ‘starting’ proposal:
  - ~ 2dB margin when using “Meg6” material
  - ~ 0dB margin when using “Meg 4” material
- Further work is required to ensure that the following factors are accounted for as part of the final loss budget proposal:
  - Insertion loss ripple;
  - PCB impedance variation;
  - Routing layer used (this leads to stubs);
  - Connector pin design (depending on phy pinout);
  - Reflections/resonances and crosstalk between individual components.

Summary

- Further work is also required to ensure that adequate margin is included in the budget to account for manufacturing, process, environmental, etc variations, and that the margins for the individual components of the end-to-end link are ‘summed’ in a realistic manner (i.e. without being overly pessimistic)

Final Thought ....

- Beware ‘budget creep’ ....
- Remember the original problem statement ....



Backup

Module Form Factors