Further Studies of FEC Codes for 100G-KR

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Introduction

- Incoming data is coded with 64B/66B transcoding
- In 10G KR, first convert data to 64B/65B and then apply Fire code encoding.
- FEC codes based on 64B/65B transcoding (>5dB coding gain, <100ns latency) have been proposed in the past IEEE 100 GCU meetings [1][2]. They are mainly based on overclocking with single reference clock.
- 512B/513B transcoding was recently incorporated in FEC proposal for 100G KR systems [3]. Particularly, a FEC code with no overclocking was presented showing good coding gain.

[1] Z Wang and C. Chen, *"Feasibility of 100G KR FEC"*, IEEE 802.3 100GCu, May 2011.
[2] S. Bhoja, etc, "FEC Proposal for 100G KR," IEEE 802.3 100GCu, Sept. 2011.
[3] R. Cideciyan, "512B/513B Transcoding and FEC for 100G Backplane and Copper lLnk,", IEEE 802.3 100GCu, Sept. 2011.

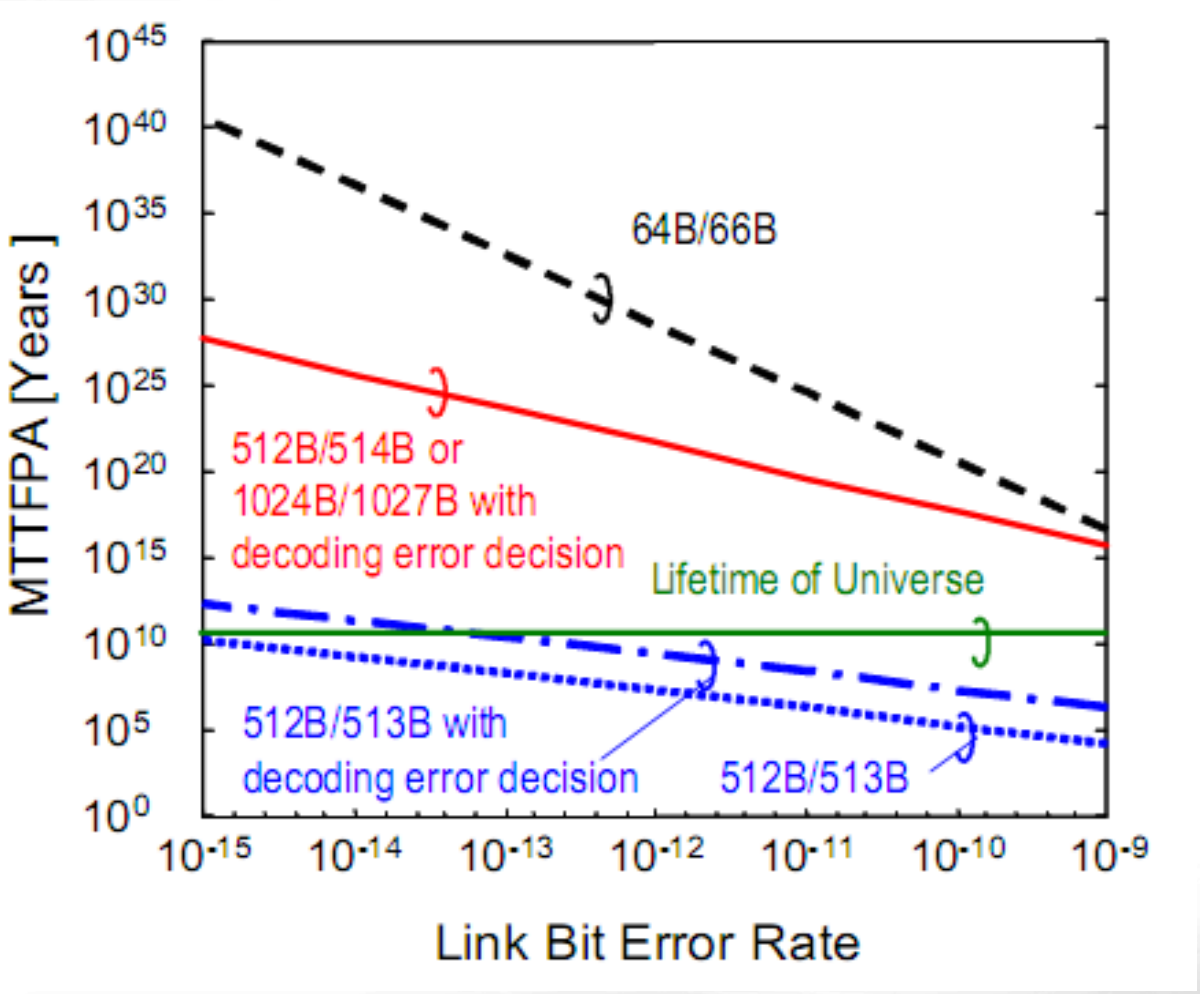
Analysis of Transcoding

- 512B/513B transcoding saves an extra redundancy of 1.3% compared to 64/65 transcoding while lowering protection for some control words.
- The analysis showed that 512B/513B trancoding has MTTFPA issue [4] [5] and self synchronization issue [6].
- The pros and cons for various transcoding methods were discussed in [6], (512*N)B/(513*N+1)B transcoding proposed by NTT was recognized as good options (see more in next page).

- 1024B/1027B (i.e., N=2) transcoding has been adopted by ITU-T for OTN.
- 512B/514B (i.e., N=1) transcoding is a good option for 100G KR.

[4] M. Teshima, etc, "Bit-Error-Tolerant (512*N)B/(513*N+1)B Code for 10Gb/s and 100Gb/s Ethernet Transport," IEEE Infocom Workshops 2008.
[5] NTT lab, "40GbE MTTFPA when using 512B/513B transcoding," ITU-T Q11/15, Feb. 2008, Geneva
[6] S. Trowbridge and O. Ishida, "40GbE MTTFPA when using transcoding," http://ieee802.org/3/ba/public/mar08/trowbridge_01_0308.pdf

Comparisons of Transcoding



* This figure is made by "cut and past" from Fig. 4 in [4].

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FEC without Overclocking (I)

- **Use 512B/514B transcoding**
- **Encode the transcoded data with RS(528, 514, t=7) over GF(2^10).**
  - Each physical lane (PL) provides source data of 20 X 66-bit blocks.
  - Combine 2x 66-b block from each PL to form a 512-b large block.
  - Use 512B /514B transcoding to generate 514-b data and send to FEC encoder
  - The encode may get 16 symbols (160bits) for the 1st 32 cycles and get 2 symbols for last cycle per frame. The encoder sends out 16 symbols per cycle with each PL transmits 4 symbols. It takes 33 cycles to transmit a frame.
  - The decoder may take 16 symbols per cycle to receive data of a FEC frame.

- **Performance comparison with (IBM) RS(352, 342, t=5) over GF(2^12) using 512B/513B transcoding:**
  - Total Latency: ~ (51+6+18+17 +6) 98ns vs. 88 ns
  - Net Coding Gain: 5.64dB vs. 5.09 dB (at 1e-15)
  - Burst error cap.: 70 bits vs. 60 bits
  - HW Complexity: ~ 1.05x vs. 1.0x
  - Available gain: ~ 4.8dB vs. 4.2dB

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FEC without Overclocking (II)

- **Use 1024B/1027B transcoding**
- **Encode the transcoded data with RS(528, 514, t=7) over GF(2^10).**
  - Each physical lane (PL) provides source data of 20 X 66-bit blocks.
  - Combine 4x 66-b block from each PL to form a 1024-b large block.
  - Use 1024B /1027B transcoding to generate 1027-b data and send to FEC encoder
  - We add 5 dummy bit for each frame to the encoder.

- **Performance comparison with the case using 512B/514B transconding**
  - Total Latency: slightly longer
  - Net Coding Gain: same
  - Burst error cap.: same
  - HW Complexity: slightly larger

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FEC Codes with Overclocking

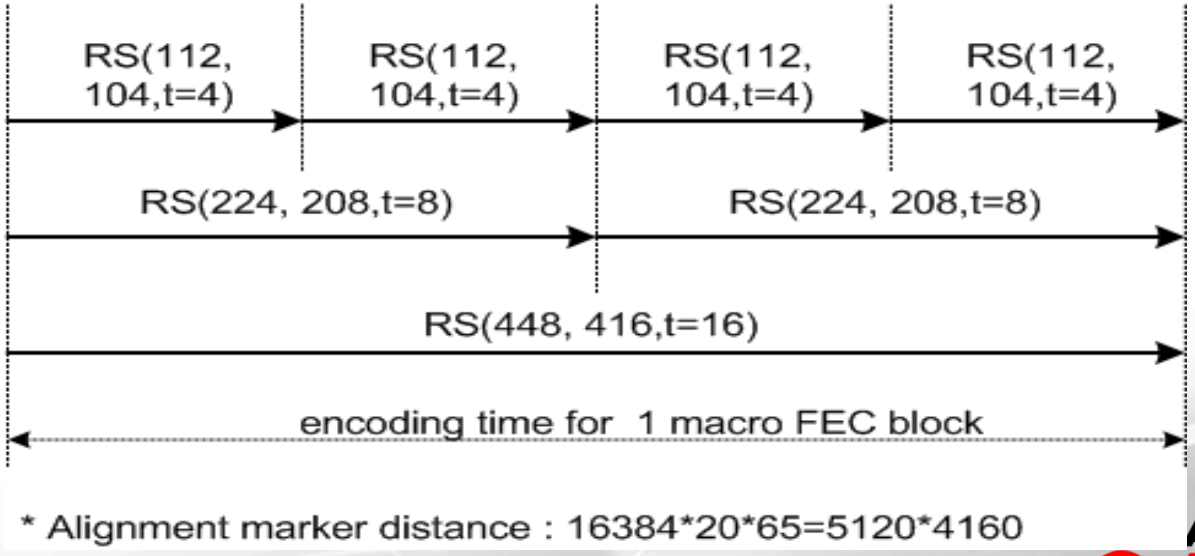
- **With 512B/514B transcoding, we can also construct RS codes under the condition of overcloking. The following lists some options:**
  - RS(536, 514, t=11) over GF(2^10), PLL: 67/66
  - RS(544, 514, t=15) over GF(2^10), PLL: 68/66
  - RS(402, 374, t=14), over GF(2^11), add 2 dummy bits, use fractional PLL
  - RS codes with t less than 11 is not considered in the ensuing comparison due to significantly less coding gain.

Comparisons for FEC Codes

Code	Coding gain (dB)	Over Clock Loss (dB)	Burst error correct cap. (bit)	Burst loss est. (dB)	Avail. Gain (dB)	latency (ns)
A: RS(448, 416, 16) TC=65/64, m=10	7.34	(6%) 1.09	160	~ 0.48	5.77	82+18 (32pCS)
B: RS(544, 514, t=15), TC=514/512, m=10	7.10	(3%) 0.545	150	~ 0.55	6.01	120+
C: RS(536, 514, t=11), TC=514/512, m=10	6.57	(1.5%) 0.272	110	~ 0.70	5.60	115+
D: RS(402, 374, t=14) TC=514/512, m=11 (2 dummy bits)	7.10	(5.2%) 0.844	154	~ 0.51	5.75	110++ (+frac PLL)
E: RS(528, 514, m=10)	5.76	0 (0%)	70	~0.98	4.8	98
F: RS(352, 342, m=12)	5.22	0 (0%)	60	~1.02	4.2	88

Analysis

- If no overclocking is highly preferred, we have 2 options.
- If high coding gain is desired, using larger size TC doesn't bring much benefit. Instead RS(448, 416) based on 64/65 TC has good tradeoff in coding again, latency and complexity.
- In addition, using RS(448, 416) code, we could give more options to system vendors in making tradeoff between coding gain and overall latency.



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Summary

- We have introduced a new FEC code based on 512B/514B transcoding for 100G KR systems without overclocking and showed good performance.
- We have made comparisons for several FEC codes under different transcoding with or without overclocking.
- We have shown that under overclocking, 64B/65B TC based RS(448, 416, t=16) code has some advantages compared to RS codes constructed based on larger size transconding.

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