Cl **00** *SC* **0** *P* *L* # 160

Lusted, Kent — Intel

Comment Type **ER** *Comment Status* **A**

The term "100GBASE-P" is now used in 13 separate instances the draft. However, it is not defined.

For example, Clause 30 uses the term in the PhyType and MAUType fields as valid syntax.

To make matters worse, Clause 80.1.4 Nomenclature now states "40GBASE-R or 100GBASE-R represents a family of Physical Layer devices using the Clause 82 Physical Coding Sublayer a physical coding sublayer...and a PMD implementing 2-level pulse amplitude modulation (PAM)." Then it states "100GBASE-P represents Physical Layer devices using the Clause 82 Physical Coding Sublayer for 100 Gb/s operation over multiple PCS lanes (see Clause 82) and a PMD implementing more than 2-level pulse amplitude modulation (PAM)."

Table 80-1 says that 100GBASE-KP4 is a "100 Gb/s PHY using 100GBASE-P encoding...." Why call it out as using BASE-P encoding? All of the other Table 80-1 entries in the base standard imply encoding to be the PCS.

Then the term sneaks into Table 82-5 and attempts to camoflages itself in the PCS column of all places! There is no 100GBASE-P PCS.

Furthermore, the IEEE 802.3bh Draft 3.1 standard defines "100GBASE-R" as "An IEEE 802.3 family of Physical Layer devices using the physical coding sublayer defined in Clause 82 for 100 Gb/s operation. (See IEEE Std 802.3, Clause 82.)"

SuggestedRemedy

Consider adding a "100GBASE-P" to the Definitions section or strike 100GBASE-P from the document.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add the following definition to 1.4:
"100GBASE-P: An IEEE 802.3 family of Physical Layer devices using the physical coding sublayer defined in Clause 82 and a physical medium dependent sublayer that employs pulse amplitude modulation with more than 2 levels for 100 Gb/s operation. (See IEEE Std 802.3, Clause 82 and Clause 84.)"

Also, modify the definition for 100GBASE-R to make the distinction between BASE-P and BASE-R.

Cl **00** *SC* **0** *P* *L* # 84

Sela, Oren — Mellanox Technologie

Comment Type **E** *Comment Status* **A**

Normal wake mode is not the best name for the "non-FW" mode. Should come up with better naming

SuggestedRemedy

some options: higher power save mode, full power save mode, deap power save mode, physical idle power save mode, full idle power save mode.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Use the term "Deep Sleep" mode to contrast with "Fast Wake" - the editor to search for and replace "normal mode" where the meaning is clear.

Cl **30** *SC* **30.1.1.15** *P* **23** *L* **19** # 93

Sela, Oren — Mellanox Technologie

Comment Type **T** *Comment Status* **A** *FEC mgmt*

aFECability - CL91 FEC is not optional

SuggestedRemedy

Change:
A read-only value that indicates if the PHY supports an optional FEC sublayer for forward error correction (see 65.2, and Clause 74, and Clause 91).
To:
A read-only value that indicates if the PHY supports an optional FEC sublayer for forward error correction (see 65.2, and Clause 74) or support of the Clause 91 mandatory FEC.

Response *Response Status* **C**

ACCEPT.

Cl **30** *SC* **30.1.1.16** *P* **23** *L* **25** # 94

Sela, Oren — Mellanox Technologie

Comment Type **T** *Comment Status* **A** *FEC mgmt*

aFECmode - Clause 91 FEC is mandatory so it shouldn't be enabled or disabled

SuggestedRemedy

There are 3 possible ways to handles this:
1. remove CL91 FEC from the text
2. Make the FEC 91 value as RO enabled
3. Use this verible to enable or disable the FEC correction at the receive side

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Option #1, also suggested by comment #367

Cl **30** *SC* **30.5.1.1.16** *P* **23** *L* **47** # 367

Anslow, Pete — Ciena

Comment Type **T** *Comment Status* **A** *FEC mgmt*

This text says "or FEC enable bit in RS-FEC control register (see 45.2.1.93a)". However, there isn't a FEC enable bit in the RS-FEC control register (Register 1.200) in 45.2.1.93a only "FEC enable error indication" which is quite different.

BASE-R FEC is optional, but I understood RS-FEC is not and hence a "FEC enable" isn't appropriate.

Am I missing something?

SuggestedRemedy

Make no change to 30.5.1.1.16 since RS-FEC cannot be disabled.

Response *Response Status* **C**

ACCEPT.

Cl **30** *SC* **30.5.1.1.17** *P* **24** *L* **5** # 300

Dudek, Mike — QLogic

Comment Type **T** *Comment Status* **A** *FEC mgmt*

We should have error counters for 100GBASE-KP4 as well

SuggestedRemedy

Add 100GBase-P Phys to this list. Also to 30.5.1.1.18

Response *Response Status* **C**

ACCEPT.

Cl **30** *SC* **30.5.1.1.17** *P* **24** *L* **7** # 301

Dudek, Mike — QLogic

Comment Type **T** *Comment Status* **A** *FEC mgmt*

Does it make sense to have this array of counters per PCS lane when the FEC is not operating on a per PCS lane basis?

SuggestedRemedy

Add after "do not use PCS lanes" "or use the RS-FEC described in clause 91.

Do the same for 30.5.1.1.18

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change "PCS lanes" to "PCS lanes or FEC lanes" throughout both subclauses.

Cl **30** *SC* **30.6.1.1.5** *P* **25** *L* **22** # 384

Dawe, Piers — IPtronics

Comment Type **ER** *Comment Status* **A** *PHY order*

Order of PHY types.

SuggestedRemedy

Use the order chosen for p48 line 42 73.6.4 Table 73-4-Technology Ability Field encoding or (reversed) in p50 73.7.6 Table 73-5-Priority Resolution. That is: slow to fast, wide to narrow, high power or short reach to low power or long reach. Also in 45.2.1.6 and 45.2.1.7.4

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The inserted items are in priority resolution order in 30.6.1.1.5.

Comment #90 changes 45.2.1.6 to be the same as 45.2.1.7.4 and 45.2.1.7.5 (i.e. also priority resolution order).

Cl **45** *SC* **45.2.1.6** *P* **28** *L* # 90

Sela, Oren — Mellanox Technologie

Comment Type **E** *Comment Status* **A** *PHY order*

For consistancy PHYs should be listed in the same order as they are in the Technology ability field and the priority resolution so 100GBASE-KP4 should be listed below 100GBASE-KR4

SuggestedRemedy

per comment

Response *Response Status* **C**

ACCEPT.

Table 45-7 - reverse KR4 & KP4

Cl **45** *SC* **45.2.1.8** *P* **29** *L* **44** # 297

Dudek, Mike — QLogic

Comment Type **E** *Comment Status* **A** *Style*

This is a very long list contained in Text it would be better to use a table

SuggestedRemedy

Create a table for Transmit disable description and point to it from here.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

There is no compelling reason to make such a change to the base text. However, the inserted text must be underlined.

Cl **45** *SC* **45.2.1.81** *P* **31** *L* **6** # 302

Dudek, Mike — QLogic

Comment Type **T** *Comment Status* **A** *Training mgmt*

Consider whether it would be useful for the 100GBASE-KP4 to provide equivalent information to that contained in 45.2.1.81 to 45.2.1.84

SuggestedRemedy

Either reword this to be BASE-R and Base-P or create equivalent additional registers for Base-P

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Registers 1.150 through 1.155 and similarly 1.1100-1.1103; 1.1200-1.1203; 1.1300-1.1303; 1.1400-1.1403 are all used by Clause 94.

Update the wording in these register descriptions. Make references clear in Clause 94.

Cl **45** *SC* **45.2.1.93** *P* **32** *L* **4** # 120

Sela, Oren — Mellanox Technologie

Comment Type **T** *Comment Status* **A** *FEC mgmt*

when FEC bypass is not supported the FEC bypass should be read only 0

SuggestedRemedy

add the folowing text:
Writes to this bit are ignored and reads return a zero if the RS-FEC does not have the ability to bypass correction (see 91.5.3.3).

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.1.93f** *P* **34** *L* **21** # 186

Slavick, Jeff — Avago Technologies

Comment Type **E** *Comment Status* **A** *Style*

"register bits 15:0" may cause confusion regarding the size of the error counter register.

SuggestedRemedy

Change "Errors detected in each FEC lane are counted and shown in register bits 15:0 in the corresponding register."
to
"Errors detected in each FEC lane are counted and shown in the corresponding register."

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.3.9** *P* **36** *L* **21** # 121

Sela, Oren — Mellanox Technologie

Comment Type **T** *Comment Status* **A** *FW mgmt*

As LPI FW is mandatory and normal mode is not this register should change to EEE both modes.

SuggestedRemedy

change in table 45-105 3.20.0 in the folwoing way:
Replave LPI_FW with LPI both mode supported.
in the description replace:
1 = Both Fast Wake and normal mode are supported
0 = only Fast Wake is supported
Replace in 45.2.3.9.6 the text with:
LPI normal mode (3.20.0)
If this bit is read as 1 the device support both modes for PHYs with the LPI FW and normal mode.
If this bit is set to 0 device support LPI FW only for those phys

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

This bit is a control bit not a status bit, it must select one or the other. However, a status bit is also required.

Add bit 3.20.9 - LPI modes supported:

1=FW only; 0 = both FW and DS.

(not valid for PHYs <40G, returns 0).

Cl **45** *SC* **45.2.7.13a** *P* **39** *L* **43** # 193

Slavick, Jeff — Avago Technologies

Comment Type **T** *Comment Status* **A** *FW mgmt*

Both is not the best term to use for descriping support of Normal and Fast Wake options.

SuggestedRemedy

Change "Both EEE modes" to be "Quiescent EEE mode support" for Tables 45-190, 45-191

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change the sense to match register 3.20.9 (proposed).

FW only - 1=FW only, 0= DS and FW modes (not valid for PHYs <40G, always reads 0).
Make appropriate changes in 45-190 & 45-191.

Cl **73** *SC* **6.10** *P* **49** *L* **15** # 194

Slavick, Jeff — Avago Technologies

Comment Type **T** *Comment Status* **A**

The transmit switch function is only applicable during Auto-Negotiation.

SuggestedRemedy

Change "Prior to entry into the AN_GOOD_CHECK state, the Transmit Switch function shall connect only the DME page generator controlled by the Transmit State Diagram to the MDI."
to:
"During Auto Negotiation and prior to entry into the AN_GOOD_CHECK state, the Transmit Switch function shall connect only the DME page generator controlled by the Transmit State Diagram to the MDI."

Response *Response Status* **C**

ACCEPT.

Cl **73** *SC* **7.2** *P* **50** *L* **1** # 195

Slavick, Jeff — Avago Technologies

Comment Type **T** *Comment Status* **A**

The recieve switch function is only applicable during auto-negotiation.

SuggestedRemedy

Change "Prior to entry into the AN_GOOD_CHECK state, the Receive Switch function shall connect the DME page receiver to the MDI."
to:
"During Auto Negotiation and prior to entry into the AN_GOOD_CHECK state, the Receive Switch function shall connect the DME page receiver to the MDI."

Response *Response Status* **C**

ACCEPT.

Cl **73** *SC* **73.10.7** *P* **51** *L* **25** # 83

Sela, Oren — Mellanox Technologie

Comment Type **E** *Comment Status* **A**

To be consistent we should have the PHY order in the same order as in the technology ability field and priority resolution - switch the order of the link status for KP4 and KR4

SuggestedRemedy

per comment

Response *Response Status* **C**

ACCEPT.

Cl **73** *SC* **73.3** *P* **48** *L* **17** # 82

Sela, Oren — Mellanox Technologie

Comment Type **E** *Comment Status* **A**

The PHYs are listed in the same order as they are in the Technology ability field and the priority resolution so 100GBASE-KP4 should be listed before 100GBASE-KR4

SuggestedRemedy

change:
include 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10, 100GBASE-KR4, 100GBASE-KP4, and 100GBASE-CR4
to:
include 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10, 100GBASE-KP4, 100GBASE-KR4, and 100GBASE-CR4

Response *Response Status* **C**

ACCEPT.

Also change order on:
Page 48, Line 52.
Page 49, Line 38.

Cl **78** *SC* **78.1** *P* **53** *L* **30** # 7

D'Ambrosia, John — Dell

Comment Type **E** *Comment Status* **A** *Style*

Avoid listings of PHYs

SuggestedRemedy

Table 78-1 specifies clauses for EEE operation over twisted-pair cabling systems, electrical backplanes, XGMII extension using the XGXS for 10 Gb/s PHYs and and inter-sub layer service interfaces using the XLAUI for 40 Gb/s PHYs and CAUI for 100 Gb/s PHYs
.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Some information is missing in the suggested remedy. Change paragraph to:

Table 78-1 specifies clauses for EEE operation over twisted-pair cabling systems, twinax cable, and electrical backplanes; for XGMII extension using the XGXS for 10 Gb/s PHYs; and for inter-sub layer service interfaces using the XLAUI for 40 Gb/s PHYs and CAUI for 100 Gb/s PHYs.

Cl **78** *SC* **78.5** *P* **54** *L* **47** # 250

Trowbridge, Steve — Alcatel-Lucent

Comment Type **T** *Comment Status* **A** *Terms*

"Fast Wake" is not a good or accurate term for the second mode of operation for EEE. It is more a different type of sleep which, by not turning off the transmitter, is able to wake faster. Figure 78-3 of the base document does not accurately show the way this new kind of sleep works.

SuggestedRemedy

Come up with a term to better characterize the type of sleep. Add a new figure (besides 78-3) to show the operation of this new type of EEE operation. See supporting presentation trowbridge_01

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add a figure that illustrates Fast Wake operation.

Change the nomenclature to refer to Deep Sleep operation in contrast to fast Wake (see comment #84)

Cl **78** *SC* **78.5** *P* **54** *L* **48** # 95

Sela, Oren — Mellanox Technologie

Comment Type **T** *Comment Status* **A** *Style*

The text is:Fast wake is mandatory for PHYs that implement EEE; normal wake is an additional optiont his statement is only true for the 40G and 100G PHYs that support EEE and not to all PHYs

SuggestedRemedy

options 1:
change the text to - Fast wake is mandatory for 40Gb/s and 100Gb/s PHYs that implement EEE; normal wake is an additional option for those PHYs
Option 2:
Fast wake is mandatory for PHYs that implement EEE and are connected to Clause 82 PCS; normal wake is an additional option for those PHYs

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Use suggested option #1

Fast wake is mandatory for 40Gb/s and 100Gb/s PHYs that implement EEE; deep sleep is an additional option for those PHYs

Cl **78** *SC* **78.5** *P* **55** *L* # 96

Sela, Oren — Mellanox Technologie

Comment Type **T** *Comment Status* **A** *Timing*

In table 78-4 PHYs with the CL74 FEC should have 2 rows under the normal mode - case 1 and case 2 when case 1 is without CL74 FEC and case 2 is with CL74 FEC

SuggestedRemedy

for the 40GBASE-CR4, 40GBASE-KR4 and 100GBASE-CR10 split the normal mode into 2 rows - case 1 and case 2.
in 78.5 change:
Case-1 of the 10GBASE-KR PHY applies to PHYs without FEC. Case-2 of the 10GBASE-KR PHY applies to PHYs with FEC.
To:
Case-1 of the 10GBASE-KR, 40GBASE-KR4, 40GBASE-CR4, and 100GBASE-CR10 PHYs
applies to PHYs without FEC. Case-2 of the 10GBASE-KR, 40GBASE-KR4, 40GBASE-CR4, and 100GBASE-CR10 PHYs applies to PHYs with FEC.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See also comment #40, #202

Cl **78** *SC* **78.5** *P* **55** *L* **32** # 42

Barrass, Hugh — Cisco

Comment Type **T** *Comment Status* **A** *Timing*

The values in Table 78-4 have been proposed and discussed, these can now be inserted.

SuggestedRemedy

change Tw_sys_rx as follows:

Normal wake - 1.2uS for 40G, 1.0uS for 100G
Fast Wake - 0.25uS for all PHYs

Response *Response Status* **C**

ACCEPT.

Cl **78** *SC* **78.5** *P* **55** *L* **32** # 40

Barrass, Hugh — Cisco

Comment Type **T** *Comment Status* **A** *Timing*

With the addition of scrambler bypass, rows need to be added to table 78-4.

SuggestedRemedy

Add rows for 40GBASE-CR4, 40GBASE-KP4 and 100GBASE-CR10 between Normal and Fast Wake with values of Tw_sys_tx, Tw_phy and Tphy_shrink_rx all 2uS larger than the corresponding values for "Normal."

Response *Response Status* **C**

ACCEPT.

Add the rows use timings from comment #202.

See also comment #96

Cl **78** *SC* **78.5** *P* **55** *L* **33** # 43

Barrass, Hugh — Cisco

Comment Type **T** *Comment Status* **A** *Timing*

The values in Table 78-4 have been proposed and discussed, these can now be inserted.

SuggestedRemedy

Change Tw_phy to 5.5uS Normal; 0.30uS Fast Wake

Response *Response Status* **C**

ACCEPT.

Tw_phy is 5.5uS for all of the rows in D1.2, comment #202 defines additional time for scrambler bypass cases.

Cl **78** *SC* **78.5** *P* **55** *L* **34** # 34

Barrass, Hugh — Cisco

Comment Type **T** *Comment Status* **A** *Timing*

The values in Table 78-4 have been proposed and discussed, these can now be inserted.

SuggestedRemedy

Change Tphy_shrink_tx to 2uS for Normal mode, all PHYs
Change Tphy_shrink_rx to 3uS for Normal mode, all PHYs
Change Tphy_shrink_tx to 0uS for Fast Wake mode, all PHYs
Change Tphy_shrink_rx to 0uS for Fast Wake mode, all PHYs

Response *Response Status* **C**

ACCEPT.

Cl **78** *SC* **78.5** *P* **55** *L* **35** # 35

Barrass, Hugh — Cisco

Comment Type **T** *Comment Status* **A** *Timing*

The values in Table 78-4 have been proposed and discussed, these can now be inserted.

SuggestedRemedy

Change Tw_sys_tx to 5.5uS for Normal mode, all PHYs; 0.34uS for Fast Wake, all PHYs.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Comment #202 defines the additional time for PHYs that include scrambler bypass.

Cl **78** *SC* **78.5** *P* **55** *L* **8** # 41

Barrass, Hugh — Cisco

Comment Type **T** *Comment Status* **A** *Timing*

The timing values for Table 78-2 have been presented and discussed (see separate presentation).

SuggestedRemedy

Insert the following values in every row:

Ts = 0.9/1.1 uS
Tq = 1700/1800 uS
Tr = 5.9/6.5 uS

Response *Response Status* **C**

ACCEPT.

Cl **79** *SC* **79.4** *P* **58** *L* **1** # 36

Barrass, Hugh — Cisco

Comment Type **T** *Comment Status* **A** *LLDP*

LLDP definitions are required for the exchange and negotiation of Fast Wake.

SuggestedRemedy

Bring Clause 79 into the draft & make the changes included in the separate submission.

Response *Response Status* **C**

ACCEPT.

See barrass_3bj_02_1112.pdf

Cl **80** *SC* **80.1.2** *P* **58** *L* **29** # 251

Trowbridge, Steve — Alcatel-Lucent

Comment Type **T** *Comment Status* **R** *OTN*

Concerning the deleted objective "Provide Appropriate Support for OTN", while P802.3bj does not have this objective, it touches three interfaces from the 802.3ba project which do, and the mechanism proposed for EEE does not preserve the OTN mapping.

SuggestedRemedy

Add, in an appropriate place, a warning note about the fact that "normal wake" operation should not be used for an interface that is transparently carried over an OTN network. Modify the operation of the "fast wake" mode so that LPI indication can be carried transparently through the OTN mapper. See supporting presentation trowbridge_01

Response *Response Status* **C**

REJECT.

See also #331, #249

The current draft does not pose any problems with appropriate support for OTN for copper interfaces. In order to connect to OTN transport, a device must be used that can act as an autonegotiation link partner and can control and terminate any functions that would not be supported over OTN (e.g. optional FEC as defined in 802.3ba). Such a device can decline the use of optional EEE if the capability is not adequately supported.

If, at some time in the future, an optical project should choose to define EEE it would need to make a number of choices regarding OTN. The operation of EEE Fast Wake might be redefined (in a number of different ways) if such choices were made.

Cl **80** *SC* **80.1.3** *P* **58** *L* **48** # 303

Dudek, Mike — QLogic

Comment Type **T** *Comment Status* **A** *MDI*

It states at the top of the next page that there is no electrical or mechanical specification of the MDI for bakplane Physical lanes

SuggestedRemedy

Delete "in Clause 84 for 40GBASE-KR4,"

Response *Response Status* **C**

ACCEPT.

Note that this is a change to the base standard.

Cl **80** *SC* **80.1.3** *P* **58** *L* **49** # 97

Sela, Oren — Mellanox Technologie

Comment Type **T** *Comment Status* **R** *MDI*

bullet g and h are wrong - 40GBASE-LR4, 100GBASE-LR4 and 100GBASE-ER4 are single lane MDI and not 4 lanes

SuggestedRemedy

g) The MDIs as specified in Clause 89 for 40GBASE-FR, in Clause 87 for 40GBASE-LR4, in Clause 88 for 100GBASE-LR4 and 100GBASE-ER4 all uses a single lane data path.
h) The MDIs as specified in Clause 84 for 40GBASE-KR4, in Clause 85 for 40GBASE-CR4, in Clause 86 for 40GBASE-SR4, and in Clause 92 for GBASE-CR4 all use a 4 lane data path.

Response *Response Status* **C**

REJECT.

Although they use 1 fiber, there are 4 lanes of data using 4 wavelengths.

Cl **80** *SC* **80.1.3** *P* **59** *L* **33** # 406

Dawe, Piers — IPtronics

Comment Type **T** *Comment Status* **R** *late, Style*

This says "CONDITIONAL BASED ON PHY TYPE" but for some PHY types it's not conditional: 74.1 "The 40GBASE-CR4 and 100GBASE-CR10 PHYs described in Clause 85 optionally use the FEC sublayer".

SuggestedRemedy

Change to"DEPENDING ON PHY TYPE". Also Figure 80-3b.

Response *Response Status* **C**

REJECT.

"CONDITIONAL BASED ON PHY TYPE" and "DEPENDING ON PHY TYPE" have identical meaning in the English language.

Cl **80** *SC* **80.1.4** *P* **59** *L* **50** # 98

Sela, Oren — Mellanox Technologie

Comment Type **T** *Comment Status* **A** *Style*

if we state that some 100GBASE-R PHYs use CL91 FEC we should also state that some 40GBASE-R and 100GBASE-R may use CL74 FEC

SuggestedRemedy

after - "...Layer devices also use the transcoding and FEC of Clause 91."
add "Some 40GBASE-R and 100GBASE-R also may use FEC of caluse 74"

Response *Response Status* **C**

ACCEPT.

Cl **80** *SC* **80.2.2** *P* **62** *L* **5** # 304

Dudek, Mike — QLogic

Comment Type **T** *Comment Status* **A** *Style*

Clause 94 does not belong in this section unless there is also some description of 100GBASE-P.

SuggestedRemedy

Add 100GBASE-P to the list of Phy types on line 5.

Do so also in Clause 80.2.5 on line 35

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change the beginning of the clause to:

"The terms 40GBASE-R, 100GBASE-R and 100GBASE-P refer ."

On line 7 change "40GBASE-R and 100GBASE-R PCSs" to "Clause 82 PCSs"

Change the beginning of 80.2.5 as 80.2.2

Cl **80** *SC* **80.2.6** *P* **62** *L* **43** # 85

Sela, Oren — Mellanox Technologie

Comment Type **E** *Comment Status* **A** *PHY order*

For consistancy PHYs should be listed in the same order as they are in the Technology ability field and the priority resolution so 100GBASE-KP4 should be listed before 100GBASE-KR4

SuggestedRemedy

per comment

Response *Response Status* **C**

ACCEPT.

Cl **80** *SC* **80.3.2** *P* **63** *L* **31** # 407

Dawe, Piers — IPtronics

Comment Type **T** *Comment Status* **R** *late, Style*

Draft proposes changing OPTIONAL OR OMITTED DEPENDING ON PHY TYPE to CONDITIONAL BASED ON PHY TYPE in Figure 80-3. Yet figure shows 10-lane PMAs below FEC. In general, these can mix up the lanes so are not allowed with Clause 91 FEC.

SuggestedRemedy

Don't do proposed change. I think the same applies to Figure 80-4, Figure 80-5. But if a change is appropriate, use just "DEPENDING ON PHY TYPE".

Response *Response Status* **C**

REJECT.

"CONDITIONAL BASED ON PHY TYPE" means the same as "DEPENDING ON PHY TYPE"

Cl **80** *SC* **80.3.2** *P* **63** *L* **32** # 329

Nicholl, Gary — Cisco

Comment Type **TR** *Comment Status* **A** *Style*

Comment against Fig 80-3b (physically located on page 65).

The figure shows a PMA (20:10) and a PMA (10:n) layer implemented below a RS-FEC layer. It is my understanding that the only PMA layer that is allowed to be implemented below a Clause 91 RS-FEC layer is a PMA (4:4), i.e. you are not allowed to do any lane bit muxing below the RS-FEC layer.

SuggestedRemedy

Please correct figure accordingly.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The figure is misleading, comment #87 (and comment #337) highlight issues that can be corrected to improve the understanding of the EEE primitives.

Cl **80** *SC* **80.3.2** *P* **63** *L* **32** # 335

Nicholl, Gary — Cisco

Comment Type **ER** *Comment Status* **A** *Style*

I would like to see another figure added similar to Fig 80-3a, but showing an example where the RS-FEC layer is separated from the 100GBASE-R PCS block by a PMA layer.

I think it is important to include this example, as it makes it very clear that applications where the RS-FEC is implemetned in a separate standalone PHY chip can be, and in fact must be, supported.

I am considered that if we do not include this example in the document we may overlook some subtle inter-layer communication that is required to support this critical application.

to shown an example where the FEC

SuggestedRemedy

Add figure added similar to Fig 80-3a, but showing an example where the RS-FEC layer is separated from the 100GBASE-R PCS block by a PMA layer.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The commenter probably missed the content of 83C-2a because two figures were given the same label.

Change the second figure 83C-2a to 83C-2b.

Cl **80** *SC* **80.3.3.4** *P* **63** *L* **51** # 100

Sela, Oren — Mellanox Technologie

Comment Type **T** *Comment Status* **A** *scr bypass*

Per changes to the LPI transnit state diagram (Figure 82-16) this should be changed

SuggestedRemedy

change:
The tx_mode parameter takes on one of up to eight values: DATA, SLEEP, QUIET, FW, ALERT, RF_ALERT, WAKE or RF_WAKE.
To:
The tx_mode parameter takes on one of up to six values: DATA, SLEEP, QUIET, FW, ALERT or BYPASS.

Response *Response Status* **C**

ACCEPT.

Cl **80** *SC* **80.3.3.4.1** *P* **63** *L* **52** # 198

Slavick, Jeff — Avago Technologies

Comment Type **T** *Comment Status* **A** *scr bypass*

WAKE, RF_ALERT and RF_WAKE no longer exist as tx_mode values.

SuggestedRemedy

Change "The tx_mode parameter takes on one of up to eight values: DATA, SLEEP, QUIET, FW, ALERT, RF_ALERT, WAKE or RF_WAKE."
to:
"The tx_mode parameter takes on one of up to five values: DATA, SLEEP, QUIET, FW or ALERT."

Response *Response Status* **C**

ACCEPT.

Cl **80** *SC* **80.3.3.6.1** *P* **66** *L* **15** # 337

Nicholl, Gary — Cisco

Comment Type **T** *Comment Status* **A** *Primitives*

How does this work if there is a intermediate PMA layer between the PCS layer and the FEC layer, i.e. how is the IS_RX_LPI_Active.request primitive transparently passed through the PMA layer than may reside between PCS and FEC layers ?

The description fo this primitive seems a little different than the others as the effect of receipt is defined specifically by the FEC sublayer whereas for the other primitives in this section the effect of receipt is defined by the sublayer which receives it (which in practive may not be the FEC layer)

SuggestedRemedy

Please add some further clarification around how this operates with an intermediate PMA layer between the PCS and the FEC, and whether the intent was in fact that IS_RX_LPI_Active.request primitive should be trated different to the other primitives in the surrounding section, IS_TX_MODE, IS_RX_MODE, etc

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

In the case where there is a PMA sublayer (or sublayers) between the PCS and the FEC IS_RX_LPI_Active.request must be passed through the PMA.

Add appropriate text in Clause 80.3.3.6 to describe this.

Add the following sentence after "communicates to the FEC that the PCS LPI receive function is active." -

"This primitive may be passed through a PMA sublayer but has no effect on that sublayer."

Cl **80** *SC* **80.3.3.7** *P* **66** *L* **34** # 338

Nicholl, Gary Cisco

Comment Type **T** *Comment Status* **A** *Primitives*

Does this primitive have to be invoked in the case of fast wake EEE ?

Do we need to clarify that the IS_ENERY_DETECT primitive is never invoked and has no effect when EEE fast wake mode is active ?

SuggestedRemedy

I think we should clarify that this primitive is never invoked and has no effect both for the case on no EEE cappability or fast wake EEE capability ? However this comment could be incorrect sa I still don't fully understand fast wake EEE :)

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

This is made clear in the PMD clauses, but needs to be clarified here.

For all of the EEE primitives, add "with the deep sleep mode option" after "optional Energy Efficient Ethernet (EEE) capability" (1 instance) and after "Without EEE capability" (4 instances)

Cl **80** *SC* **80.4** *P* **67** *L* **14** # 339

Nicholl, Gary Cisco

Comment Type **T** *Comment Status* **R** *Delays*

Does the first row of Table 80-3 have any aimplications for supporting a RS-FEC implementation on a 802.3ba host line card not originally designed for supporting RS-FEC.

An example here would be the inclusion of the RS-FEC into an optical module supporting the new 100GBASE-SR4 PMD being developed within 802.3bm, and plugged into an existing 802.3ba host line card. It is critical that this application can be supported so I am wondering if the additional delay of the RS-FEC layer would break anything on an existing 802.3ba host, for example with PAUSE buffering ?

SuggestedRemedy

More of a question for clarification, so no proposed remedy just yet.

Response *Response Status* **C**

REJECT.

The design of pause buffers (and the control of latency, generally) is a matter for system implementers. The delays in this table are intended to help interoperability.

It should be noted that the delay specified for RS-FEC is significantly less than that specified for BASE-R FEC in 802.3ba, so any system designed to tolerate the existing FEC will cope with the newly specified FEC. Furthermore, the delay of the RS-FEC sublayer is of a similar magnitude to the media delay from 100m of fiber.

Cl **80** *SC* **80.4** *P* **67** *L* **20** # 352

Anslow, Pete Ciena

Comment Type **E** *Comment Status* **A** *PHY order*

Comment #178 against D 1.1 was accepted but not fully implemented. Reach order has not been preserved.

SuggestedRemedy

Change the order of the additional rows shown in Table 80-3 to be:
100GBASE-R RS-FEC
100GBASE-KR4
100GBASE-KP4
100GBASE-CR4
In other words, move the CR4 row to the bottom.

Response *Response Status* **C**

ACCEPT.

Cl **80** *SC* **80.5** *P* **67** *L* **44** # 333

Nicholl, Gary Cisco

Comment Type **E** *Comment Status* **R** *Style*

Do we need to add an additional figure (say Figure 80-5b), showing an example with a CAUI4 interfacae between the 100GBASE-R PCS layer and RS-FEC layer ? Perhaps this is not required if the skew points and skew values would be identical to those shown in Figure 80-5a ?

SuggestedRemedy

If you agree with the comment then add a new figure as described above. If not then don't.

Response *Response Status* **C**

REJECT.

There is no CAUI-4 defined in this project, however the skew points defined (SP0/SP7) should remain the same for either CAUI-10 or CAUI-4. If a future project should see fit to define an interface for CAUI-4 then it will be the responsibility of that project to update the diagram to include the appropriate labeling for both PMA SERVICE INTERFACE instances (and adjacent PMAs).

Cl **80** *SC* **80.5** *P* **70** *L* **11** # 385

Dawe, Piers IPtronics

Comment Type **T** *Comment Status* **R** *Delay*

The Skew and particularly, Skew Variation allocations were developed for 10 lanes. When there can be no more than 4 lanes, trace length mismatch will be reduced, so these limits are probably higher than needed for 4 lanes, costing buffers that will never be used.

SuggestedRemedy

Review the Skew and Skew Variation allocations, bearing in mind the difference between 10 lanes and 4.

Response *Response Status* **C**

REJECT.

In project .3ba it was concluded that 4 lane and 10 lane implementations could suffer from the same skew (in terms of time). There has been no evidence presented in this project to overturn that conclusion.

Cl **80** *SC* **80.5** *P* **70** *L* **23** # 199

Slavick, Jeff Avago Technologies

Comment Type **T** *Comment Status* **A** *Timing*

Table 80-5 states that SP6 is N/A for 25G rates, but Figure 80-5a shows it coming out of a PMA(4:4) for a 100GBASE-R PHY stackup which would be a 25G signaling location.

SuggestedRemedy

Change the N/A for SP6 in Table 80-5 to~98

Response *Response Status* **C**

ACCEPT.

Cl **80** *SC* **80-3b** *P* **65** *L* # 87

Sela, Oren Mellanox Technologie

Comment Type **E** *Comment Status* **A** *Style*

Figure 80-3b Optional inter-sublayer service interface for EEE support is confusing need to calrify and split into 2 figures

SuggestedRemedy

1) add a comment that this figure only has the additional signals on top of those in Figrue 80-3a.
2) the PMA attached below an RS-FEC sublayer can only be a 4:4, because the figure has both the RS-FEC and CL74 FEC in the same figure it looks like a 4:n or a 10:n or a 20:10 PMA can be attached to the RS-FEC sublayer.
splitning this into 2 Figures - one with the optional CL74 FEC and one with the madatory RS-FEC will make this more clear

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

To reduce confusion:

Add text to the diagram stating that this is only the additional signals for optional EEE.

Delete the specifics for the PMA sublayers (20:10 etc.) and add a PMA between the PCS & the FEC (issue highlighted by comment #337)

Cl **80** *SC* **80-4** *P* **69** *L* # 111

Sela, Oren — Mellanox Technologie

Comment Type **T** *Comment Status* **R** *Delay*

Table 80-4
The PCS lane to lane skew should not be applicable for the 100GBASE-CR4/KR4/KP4. Those number include significant skew components that are not relevent - optical PMD skew - SP3 and SP4, it also has siginifcant PMA skew that is too high for a 4:4 PMA

SuggestedRemedy

Split the table into 2 table. Table 1 should remain the same as table 80-4 in 802.3-2012.
the second table should only have the 100G skew and should be applicable to the new PHYs.
For the new table SP0 should remain 29ns, SP1 can be 29ns, SP2 should be ~36ns. SP3 should be~41ns, SP4 should be~60ns (copper MDI only), SP5 should be~65ns and SP6 should be~73ns. SP7 should still be 29ns.
as a result the latency at the FEC receive should change from 180ns to~90ns
this should also effect 91.5.3.1 on page 124 line 41.

Response *Response Status* **C**

REJECT.

The skew budgeting mechanism in 40/100G Ethernet is based around interchangeable usage of sublayers. It is likely that future projects will continue to use sublayers in that manner. A system implementer who configures sublayers in a fixed manner may take advantage of reduced skew budgets according to the specific configuration.

Cl **81** *SC* **81.1.7** *P* **72** *L* **43** # 14

D'Ambrosia, John — Dell

Comment Type **TR** *Comment Status* **R** *PICS*

Following sentence
"EEE capability requires the use of the MAC defined in Annex 4A for simplified full duplex operation (with..."

states a requirement, but there is associated SHALL statement

SuggestedRemedy

Change sentence to
"EEE capability shall use the MAC defined in Annex 4A for simplified full duplex operation (with...."

Add corresponding PIC

Response *Response Status* **C**

REJECT.

Adding a "shall" and associated PIC would create a requirement in one clause that could only be satisfied in a different clause. The statement as written matches those used in other RS clauses.

Cl **81** *SC* **81.3.1.5** *P* **73** *L* **40** # 334

Nicholl, Gary — Cisco

Comment Type **E** *Comment Status* **R** *Style*

This line states that LPI is requested by the RS aasserting TXC and setting TXD to 0x06 (in all lanes). However Fig 81-6a at the top of page 74, gives the impression that 0x06 is only sent on lane 0 , i.e. TXD <7:0>.

SuggestedRemedy

Modify Fig 81-6a to show that LPI is signalled as 0x06 on all lanes and not just on lane 0 (TXD<7:0>).

Response *Response Status* **C**

REJECT.

The note in this figure states:

Note: TXC and TXD are shown for one lane, all 8 lanes behave identically during LPI

Cl **81** *SC* **81.3.1.5** *P* **73** *L* **45** # 101

Sela, Oren — Mellanox Technologie

Comment Type **T** *Comment Status* **A** *Timing*

Might be good to calrify that the time in this statement is Tw_sys_tx

SuggestedRemedy

change to:
The RS should not present a start code for valid transmit data until after the wake up time specified for the PHY (Tw_sys_tx). The wake times are shown in Table 78-4

Response *Response Status* **C**

ACCEPT.

Cl **81** *SC* **81.3.2.4** *P* **74** *L* **41** # 340

Nicholl, Gary — Cisco

Comment Type **T** *Comment Status* **R** *Style*

This section indicates that the PHY signals LPI to the RS by asserting RXC and setting RXD to 0x06 (on all lanes). However Figure 81-8a gives the impression that only lane 0 , i.e. RXD<7:0> is set to 0x06.

SuggestedRemedy

Propose modfiying the table to show that all RXD lanes are set to 0x06, or at least make it clear that all lanes are set and that only lane 0 is shown in the diagram for clarity.

Response *Response Status* **C**

REJECT.

The note in this figure states:

Note: RXC and RXD are shown for one lane, all 8 lanes behave identically during LPI

Cl **81** *SC* **81.3.4** *P* **75** *L* **31** # 341

Nicholl, Gary — Cisco

Comment Type **T** *Comment Status* **R** *Style*

This section states:

"Sublayers within the PHY are capable of detecting faults that render a link unreliable for communication. Upon recognition of a fault condition, a PHY sublayer indicates Local Fault status on the data path."

The term "unreliable for communication" is very vague and not clearly defined.

Now that were are moving to these higher speed ethernet links customers are starting to take link fault signalling more seriously (and see more value in it), I am getting increasing questions from the field where a customer see a LF condition and wants to know what caused it This is always a difficult question to answer as it is not clearly defined in the stadnard.

SuggestedRemedy

I tihnk we should clearly define in the standard as to which alarm conditions generate a Local Fault (LF). I don't think this is that difficult and the list would be something like PMD:LOS, PMA:LOL, PCS:Loss-of-block-lock: PCS: HI-BER .. basically the basic PHY alarms reported in the MDIO section.

I think standrdizing this would be a great service to the industry.

This is really no different to what has been done in the past for SONET and OTN equipment where the alarm conditions which generate AIS (SONET/OTN equivalent of LF) are clearly defined and implemented consistently across equipment from multiple vendors.

Response *Response Status* **C**

REJECT.

This is the text that was agreed during 802.3ba. This is simple descriptive text, it is unnecessary to go into details regarding other clauses.

Cl **81** *SC* **81.3a** *P* **76** *L* **1** # 327

Nicholl, Gary Cisco

Comment Type **T** *Comment Status* **R** *Style*

What appears to be missing in this section (and in Figure 91-9a) is a description of whether this LPI assertion and detection functional block and associated state machines is implemeted upstream or downstream from the link fault singaling functional block (described in section 81.3.4).

I believe it must be implemented upstream (above) the link fault signalling block as when a Local Fault is received by the RS from the PHY layer, then the trasnmit RS stops sending either MAC date or LPI and instead sends continuous Remote Fault towards the PHY.

SuggestedRemedy

Please clarify where in the data path this function is to be included, with respect to link fault signalling. If the convention is that this is implicitely defined by the fact that this section(81.3a) occurs before the link fault signalling section (81.4) then you can ignore this comment.

Response *Response Status* **C**

REJECT.

The position of the LPI assertion and detection mechanism is immaterial. The behavioral definition of the link fault signaling makes it clear that link fault overrides LPI.

Cl **81** *SC* **81.3a** *P* **76** *L* **35** # 330

Nicholl, Gary Cisco

Comment Type **TR** *Comment Status* **A** *Style*

"The definition of TXC<7:0> and TXD<63:0> is derived from the state of PLS_DATA.request (81.1.7), except when it is overridden by an assertion of LP_IDLE.request."

Is this actually ture ?

In the case of a Remote Fault condtion aren't both the state of PLS_DATA.request and LP_IDLE.request ultimately overwritten by the assertion of Remote Fault.

The definition of TXC<7:0> and TXD<63:0> is derived from the state of the follwoing in priority order:

1. Remote Fault
2. LP_IDLE.request
3. PLS_DATA.request

SuggestedRemedy

If my comment is correct then I suggest updating the text to reflect this.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change: "an assertion of LP_IDLE.request" to "an assertion of Remote Fault or LP_IDLE.request"

Cl **82** *SC* **82.1.3** *P* **80** *L* **27** # 188

Slavick, Jeff Avago Technologies

Comment Type **E** *Comment Status* **R** *Style*

Note 1 & 2 now state the same thing.

SuggestedRemedy

Remove NOTE 2 from Figure 82-1 and change all references in the diagram for NOTE 2 (the two instances of AN2) to reference NOTE 1.

Response *Response Status* **C**

REJECT.

This was addressed by comment #337 on draft 1.1.

Although the comment is correct, the consolidation of the 2 notes may be more easily achieved during the revision.

Cl **82** *SC* **82.1.4** *P* **80** *L* **36** # 328

Nicholl, Gary — Cisco

Comment Type **T** *Comment Status* **R** *Style*

"For Physical Layers that use Clause 91 RS-FEC, if an optional physical instantiation, i.e. CAUI, is not implemented directly below the PCS sublayer, then the lower interface connects to the FEC sublayer."

I want to make sure that this text does not preclude a CAUI-4 (i.e. optionaly 4 lane electrical interface) being implemented between the PCS sublayer and the RS-FEC sublayer.

Perhaps this is something that should be punted until we add an optional CAUI4 interface in 802.3bm. I do see applcations however where a standalone backplane PHY chip (FR4,KP4) would be connected to an existing 8023.ba MAC ASIC via a 4x25G (CAUI4) electrical interface.

SuggestedRemedy

More of a question for clarification. Remedy if required may be punted to a comment against a future 802.3bm draft.

Response *Response Status* **C**

REJECT.

This sentence describes the simple fact that the PCS may or may not be connected directly to the FEC. The existence, or otherwise of a 4-lane CAUI would make no difference to the sense of this section.

Cl **82** *SC* **82.2.18.2** *P* **87** *L* **9** # 103

Sela, Oren — Mellanox Technologie

Comment Type **T** *Comment Status* **A** *Control*

LPI should not be transmitted or received when EEE is not supported or when it is not enabled.

SuggestedRemedy

change:
Note: A PCS that does not support EEE classifies vectors containing one or more /LI/ control characters as type E
To:
Note: A PCS that does not support EEE or a PCS that does support EEE but EEE is disableed classifies vectors containing one or more /LI/ control characters as type E

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Note: If EEE has not been negotiated or if the PCS that does not support EEE vectors containing one or more /LI/ control characters are classified as type /E/

Cl **82** *SC* **82.2.18.2.5** *P* **88** *L* **41** # 201

Slavick, Jeff — Avago Technologies

Comment Type **T** *Comment Status* **A** *scr bypass*

The state TX_RF_WAKE has been removed.

SuggestedRemedy

Remove the "or TX_RF_WAKE" from the tx_tw_timer definition.

Response *Response Status* **C**

ACCEPT.

Cl **82** *SC* **82.2.18.3.1** *P* **88** *L* **33** # 39

Barrass, Hugh — Cisco

Comment Type **T** *Comment Status* **A** *Timing*

Scrambler bypass will require extra time for the wake.

SuggestedRemedy

Change Table 82-5b:

Add a row:

Twr | Time the receiver waits in the RX_WAKE state before indicating a wake time fault, LPI_FW = FALSE & scr_bypass = TRUE | - | 6.5 | uS

Add "& scr_bypass = TRUE" to other row with LPI_FW = FALSE

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Timing values defined in comment #202

Cl **82** *SC* **82.2.18.3.1** *P* **89** *L* **12** # 202

Slavick, Jeff — Avago Technologies

Comment Type **T** *Comment Status* **A** *Timing*

Tx LPI Transmit state machine needs update to support scrambler bypass modes and such. Changes for Table 82-5a and 82-5b are also needed to support the changes to state machine diagram.

SuggestedRemedy

See slavick_3bj_01_1112.pdf

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Use the timings from option #2 (slide 16) & the diagram from slide 5. The editor has license to change the form of the diagram to fit the draft without changing the function.

See also comment #39, 201, 283, 284

Cl **82** *SC* **82.2.18.3.1** *P* **89** *L* **18** # 283

Barrass, Hugh — Cisco

Comment Type **T** *Comment Status* **A** *scr bypass*

LPI Tx state diagram needs to change to support scrambler bypass. State TX_RF_ALERT is being deleted.

SuggestedRemedy

Delete references to state TX_RF_ALERT.

Response *Response Status* **C**

ACCEPT.

Cl **82** *SC* **82.2.18.3.1** *P* **89** *L* **20** # 282

Barrass, Hugh — Cisco

Comment Type **T** *Comment Status* **A** *Timing*

LPI Tx state diagram needs to change to support scrambler bypass. In support of this Twl needs to be set for the cases of scr_bypass_enable = TRUE or FALSE.

SuggestedRemedy

Duplicate the row with Twl & LPI_FW = FALSE, the two rows consisting of:

Twl | Time spent in the TX_WAKE states, LPI_FW = FALSE & scr_bypass = FALSE | 3.9 | 4.1 | uS

Twl | Time spent in the TX_WAKE states, LPI_FW = FALSE & scr_bypass = TRUE | 2.4 | 2.6 | uS

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Timing values are defined in comment #202

Cl **82** *SC* **82.2.18.3.1** *P* **97** *L* **1** # 284

Barrass, Hugh — Cisco

Comment Type **T** *Comment Status* **A** *scr bypass*

LPI Tx state diagram needs to change to support scrambler bypass.

SuggestedRemedy

Replace Fig 82-16 with the version supplied in a separate submission.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See resolution to comment #202

Cl **82** *SC* **82.2.3.4** *P* **81** *L* **19** # 6

D'Ambrosia, John Dell

Comment Type **T** *Comment Status* **R** *PICS*

This subclause calls out the control codes. THe pics in 82.7.4.1 call out c5 (only valid control characters are transmitted), however there isn't a corresponding SHALL statement for this in the text. The included SHALL statements address NOT transmitting values only.

SuggestedRemedy

modify PIC statement to properly address codes to be transmitted and not transmitted.

Response *Response Status* **C**

REJECT.

There are "shall" statements in the base standard for both C5 and C6 in Table 82.7.4.1.

[Set CommentType to T (not specified by commenter).]

Cl **82** *SC* **82.2.3.4** *P* **81** *L* **31** # 102

Sela, Oren Mellanox Technologie

Comment Type **T** *Comment Status* **A** *Control*

LPI should not be transmitted or received when EEE is not supported or when it is not enabled.

SuggestedRemedy

Change:
If EEE is not supported LPI shall not be transmitted and shall be treated as an error if received.
To:
If EEE is not supported or EEE is supported but not enabled LPI shall not be transmitted and shall be treated as an error if received.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Note: If EEE has not been negotiated or if the PCS that does not support EEE LPI shall not be transmitted and shall be treated as
an error if received.

Cl **82** *SC* **82.2.8a** *P* **83** *L* **2** # 331

Nicholl, Gary Cisco

Comment Type **TR** *Comment Status* **R** *OTN*

Rapid alignment markers cause issues when running over OTN equipment.

The primary ethernet PMDs used to connect to OTN equipment are likely to be optical (i.e. no backplane or copper).

For optical PMDs I believe the proposal is to only define support for the EEE fast wake mode.

For EEE fast wake mode, where the PCS, PMA and PMD are never turned of I see no reason or value in switching to rapid alignment markers.

For EEE fast wake mode I would propose to continue using standard alignment markers, and this resolves the issue with interop over OTN equipment.

SuggestedRemedy

Propose that rapid alignment makers are only used for EEE normal wake mode (where they are needed and add value), whereas standard alignment makers should continue to be used for EEE fast wake mode.

Response *Response Status* **C**

REJECT.

See also #251, 249

There is currently no objective for EEE for optical interfaces. It would be premature to make a drastic change based on a possible requirement from another project. If, at some time in the future, an optical project should choose to define EEE it would need to make a number of choices regarding OTN. The operation of EEE Fast Wake might be redefined (in a number of different ways) if such choices were made and the copper Task Force can define the optimal changes to the mechanism.

Cl **82** *SC* **82.2.8a** *P* **83** *L* **294** # 249

Trowbridge, Steve — Alcatel-Lucent

Comment Type **T** *Comment Status* **R** *OTN*

Rapid alignment markers are only needed for the "Normal Wake" mode of EEE to rapidly frame the refresh or wake signal after turning back on the transmitter. For the "fast wake" mode of operation, LPI control characters should be sent while maintaining normal lane alignment.

SuggestedRemedy

For "fast wake", LPI should be signaled while maintaining lane alignment. LPI control characters are changed to Idle characters Tw prior to resuming transmission of MAC data. This provides a simpler method of "fast wake" operation that could be reused for P802.3bm and maintain OTN compatibility for those interfaces. See supporting presentation trowbridge_01.

Response *Response Status* **C**

REJECT.

See comment #251, 331

[CommentType set to T (commenter did not specify).]

The choice of the current mechanism for Fast Wake was based on multiple presentations and discussions in the Task Force. It would be premature to make a drastic change based on a possible requirement from another project. If, at some time in the future, an optical project should choose to define EEE it would need to make a number of choices regarding OTN. The operation of EEE Fast Wake might be redefined (in a number of different ways) if such choices were made and the copper Task Force can define the optimal changes to the mechanism.

Note also that RAMs are used to convey state information across sublayer boundaries in the current architecture.

Cl **82** *SC* **82.2.8a** *P* **83** *L* **49** # 75

Wong, Don — Cisco Systems

Comment Type **T** *Comment Status* **A** *RAM*

The current propose method of distinguishing between RAM versus existing alignment marker relies upon the replacement of the bip fields with the CD. Upon sampling single a RAM or alignment marker, it's hard to tell if a bip3 or CD field is present.

SuggestedRemedy

The current propose method of distinguishing between RAM versus existing alignment marker relies upon the replacement of the bip fields with the CD. Upon sampling single a RAM or alignment marker, it's hard to tell if a bip3 or CD field is present.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

There should be a foolproof way of distinguishing between the two. Swap the position of the fields M0 - M4; M1 - M5; M2 - M6 for RAMs. The editor will change the diagram and text accordingly (82-9b, 82.2.8a)

Cl **82** *SC* **82.6** *P* **92** *L* **38** # 76

Wong, Don — Cisco Systems

Comment Type **T** *Comment Status* **R** *RAM*

Figure 82-11. When transiting from alignment marker to rapid alignment marker, there is no guidance on when the am_counter terminal count changes from 16K to 8/16 blocks.

SuggestedRemedy

Response *Response Status* **C**

REJECT.

There is no precise requirement for positioning of the first RAM after transitioning (other than the 4-block boundary rule - 82.2.8a). If such a requirement is necessary it could be added but there has been no justification for such a restriction. Therefore it is left to the system implementer to decide exactly when the terminal count changes, provided that the 8/16 block rule is observed.

Cl **82** *SC* **82.6** *P* **92** *L* **38** # 77

Wong, Don — Cisco Systems

Comment Type **T** *Comment Status* **R** *RAM*

Fig 82-11. When transiting from align marker to rapid alignment marker, will take 64K blocks (83.8 msec) to lose alignment lock. 83.8 msec seems like a long time.

SuggestedRemedy

Response *Response Status* **C**

REJECT.

When transitioning to RAMs for normal mode, the LP will stop transmitting and block_lock will fail - which causes an immediate loss of alignment_lock. When transitioning to RAMs in Fast Wake mode, the alignment is checked much more frequently because the RAMs are only 8 or 16 blocks apart - therefore the alignment loss would be 1000 or 2000 times faster then the example. When transitioning back to normal alignment markers, the time to lose alignment is 83.8 msec which is a long time but is the same for all 100G PHYs.

Cl **83A** *SC* **83A.3.2a** *P* **269** *L* **33** # 286

Barrass, Hugh — Cisco

Comment Type **T** *Comment Status* **A** *AUI*

The XLAUI/CAUI EEE behavior can be defined in the same way as 40GBASE-CR4 (etc.) as it is a similar 10Gbps interface.

SuggestedRemedy

If the EEE capability includes XLAUI/CAUI shutdown (see 78.5.2) then when tx_mode is set to ALERT, the transmit direction sublayer sends a repeating 16-bit pattern, hexadecimal 0xFF00 which is transmitted across the XLAUI/CAUI. When tx_mode is QUIET, the transmit direction XLAUI/CAUI transmitter is disabled as specified in 83A.3.3.1.1. Similarly when the received tx_mode is set to ALERT, the receive direction sublayer sends a repeating 16-bit pattern, hexadecimal 0xFF00 which is transmitted across the XLAUI/CAUI. When the received tx_mode is QUIET, the receive direction XLAUI/CAUI transmitter is disabled as specified in 83A.3.3.1.1.

Response *Response Status* **C**

ACCEPT.

Cl **83A** *SC* **83A.3.3.1.1** *P* **270** *L* **52** # 287

Barrass, Hugh — Cisco

Comment Type **T** *Comment Status* **A** *AUI*

The XLAUI/CAUI EEE behavior can be defined in the same way as 40GBASE-CR4 (etc.) as it is a similar 10Gbps interface.

SuggestedRemedy

Delete the editor's note.

Change the clause to read:

For EEE capability with XLAUI/CAUI shutdown, the XLAUI/CAUI transmitter lane's differential peak-to-peak output voltage shall be less than 30mV within 500ns of tx_mode changing to QUIET in the relevant direction. Furthermore, the CAUI transmitter lane's differential peak-to-peak output voltage shall be greater than 720mV within 500ns of tx_mode ceasing to be QUIET in the relevant direction.

Response *Response Status* **C**

ACCEPT.

Cl **83A** *SC* **83A.3.3.6** *P* **270** *L* **35** # 291

Barrass, Hugh — Cisco

Comment Type **T** *Comment Status* **A** *rx_mode*

The rx_mode changes need to be reflected in this paragraph.

SuggestedRemedy

Change the paragraph after "If no energy is being received on the CAUI for the ingress direction..." to:

SIGNAL_DETECT is set to FAIL following a transition from rx_mode = DATA to rx_mode = QUIET. When rx_mode = QUIET, SIGNAL_DETECT shall be set to OK within 500 ns following the application of a signal at the receiver input detects an ALERT signal driven from the XLAUI/CAUI link partner. While rx_mode = QUIET, SIGNAL_DETECT changes from FAIL to OK only after the valid ALERT signal is applied to the channel.

Response *Response Status* **C**

ACCEPT.

Cl **84** *SC* **84.2** *P* **106** *L* **43** # 20

D'Ambrosia, John Dell

Comment Type **TR** *Comment Status* **A** *PICS*

PIC statement for LPI, but no corresponding SHALL statement

SuggestedRemedy

add SHALL statement

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The PICS item is for the major capability that is refernced by other PICS items. This does not correspond to a "shall" - compare this to XLAUI.

However, the reference should be to 84.1 as that is the overall description of major capabilities.

Cl **84** *SC* **84.2** *P* **106** *L* **50** # 203

Slavick, Jeff Avago Technologies

Comment Type **T** *Comment Status* **A** *scr bypass*

RF_ALERT, WAKE nad RF_WAKE are no longer valid settings for tx_mode.

SuggestedRemedy

Remove the references in 84.2 to RF_ALERT, WAKE and RF_WAKE and update the number of valid values to be five. Also fix section 85.2

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Comment #106 makes the change in 84.2.

Make the same change in 85.2.

Cl **84** *SC* **84.2** *P* **106** *L* **54** # 106

Sela, Oren Mellanox Technologie

Comment Type **T** *Comment Status* **A** *scr bypass*

per latest change to the LPI transmit state diagram TX_MODE values should change

SuggestedRemedy

change:
The tx_mode parameter takes on one of up to eight values: DATA, SLEEP, QUIET, FW, ALERT, RF_ALERT, WAKE or RF_WAKE.
To:
The tx_mode parameter takes on one of up to six values: DATA, SLEEP, QUIET, FW, ALERT or BYPASS.

Response *Response Status* **C**

ACCEPT.

Cl **84** *SC* **84.7.2** *P* **106** *L* **10** # 21

D'Ambrosia, John Dell

Comment Type **TR** *Comment Status* **A** *PICS*

It would seem that there should be some SHALL statements in here.
PICS missing as well

SuggestedRemedy

change
When tx_mode is ALERT, the transmitter equalizer taps are set to the preset state specified in 72.6.10.2.3.1.
to
When tx_mode is ALERT, the transmitter equalizer taps shall be set to the preset state specified in 72.6.10.2.3.1.

add PIC

Change
When tx_mode is QUIET, the transmitter is disabled as specified in
84.7.6
to
When tx_mode is QUIET, the transmitter SHALL be disabled as specified in
84.7.6
add PIC
.
.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Make the suggested changes to 84.7.2, add 1 PICS item:

FS13 - Transmit function for EEE - Transmitter behavior during ALERT and QUIET

Cl **84** *SC* **84.7.4** *P* *L* # 22

D'Ambrosia, John Dell

Comment Type **TR** *Comment Status* **A** *Bucket*

two pic statements FS13 (signal detect during LPI) and FS14 (signal detect for EEE) but only one shall statement

SuggestedRemedy

add appropriate shall statement (believe it is for LPI)

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Combine to 1 item: signal detect function for EEE.

Cl **84** *SC* **84.7.4** *P* **107** *L* **35** # 305

Dudek, Mike QLogic

Comment Type **T** *Comment Status* **A** *Style*

Once trained the pk-pk output of the channel even with a 16 unit interval square wave will not be 720mV.

SuggestedRemedy

State that the signal detect should be set to OK within 500ns of receiving a signal that is slightly larger than the Transmitter Off amplitude (35mV). 40mV would be a good value. Remove the words about interference tolerance test channels etc.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change the sentence to read:

"When rx_mode = QUIET, SIGNAL_DETECT shall be set to OK within 500ns following the application of a signal at the receiver input that corresponds to an ALERT transmission (see 85.7.2) from the link partner."

See also comment #306

Cl **84** *SC* **84.7.6** *P* **106** *L* **50** # 23

D'Ambrosia, John Dell

Comment Type **TR** *Comment Status* **R** *PICS*

Loopback during blogal_PMD_transmit_disable Shall statement with no corresponding PIC

SuggestedRemedy

add pic to address

Response *Response Status* **C**

REJECT.

The base standard covers this with item FS9.

Cl **85** *SC* **85.7.4** *P* **111** *L* **31** # 306

Dudek, Mike QLogic

Comment Type **T** *Comment Status* **A** *Style*

Once trained the pk-pk output of the channel even with a 16 unit interval square wave will not be 720mV.

SuggestedRemedy

State that the signal detect should be set to OK within 500ns of receiving a signal that is slightly larger than the Transmitter Off amplitude (30mV). 40mV would be a good value. Remove the words about interference tolerance test channels etc.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change the sentence to read:

"When rx_mode = QUIET, SIGNAL_DETECT shall be set to OK within 500ns following the application of a signal at the receiver input that corresponds to an ALERT transmission (see 85.7.2) from the link partner."

See also comment #305

Cl **85** *SC* **85.7.6** *P* **110** *L* **49** # 24

D'Ambrosia, John Dell

Comment Type **TR** *Comment Status* **R** *PICS*

THis shall statement
Loopback, as defined in 85.7.8, shall not be affected by Global_PMD_transmit_disable.

has no PIC

SuggestedRemedy

add PIC

Response *Response Status* **C**

REJECT.

Yes it does. PF12.

Cl **85** *SC* **85.7.6** *P* **110** *L* **50** # 25

D'Ambrosia, John Dell

Comment Type **TR** *Comment Status* **R** *PICS*

Output amplitude LPI voltage and Output Amplitude ON voltage PICS Similar to TC3 and TC4 in Clause 84 PICs) missing

SuggestedRemedy

add PICs

Response *Response Status* **C**

REJECT.

See PICS items DS6, DS7