FEC Proposal for 100G KR

100 Gb/s Backplane and Cable Task Force
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Outline

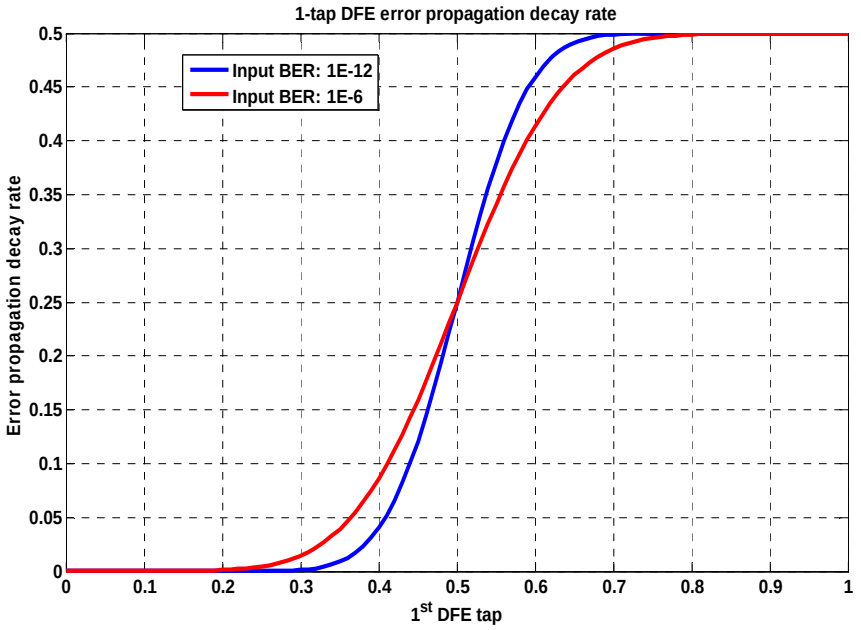
- Introduction
- DFE Burst Error Analysis
- Proposed Baseline Reed Solomon Code
- SNR Loss Due to Over Clocking
- Performance Comparison
- Conclusion

Introduction

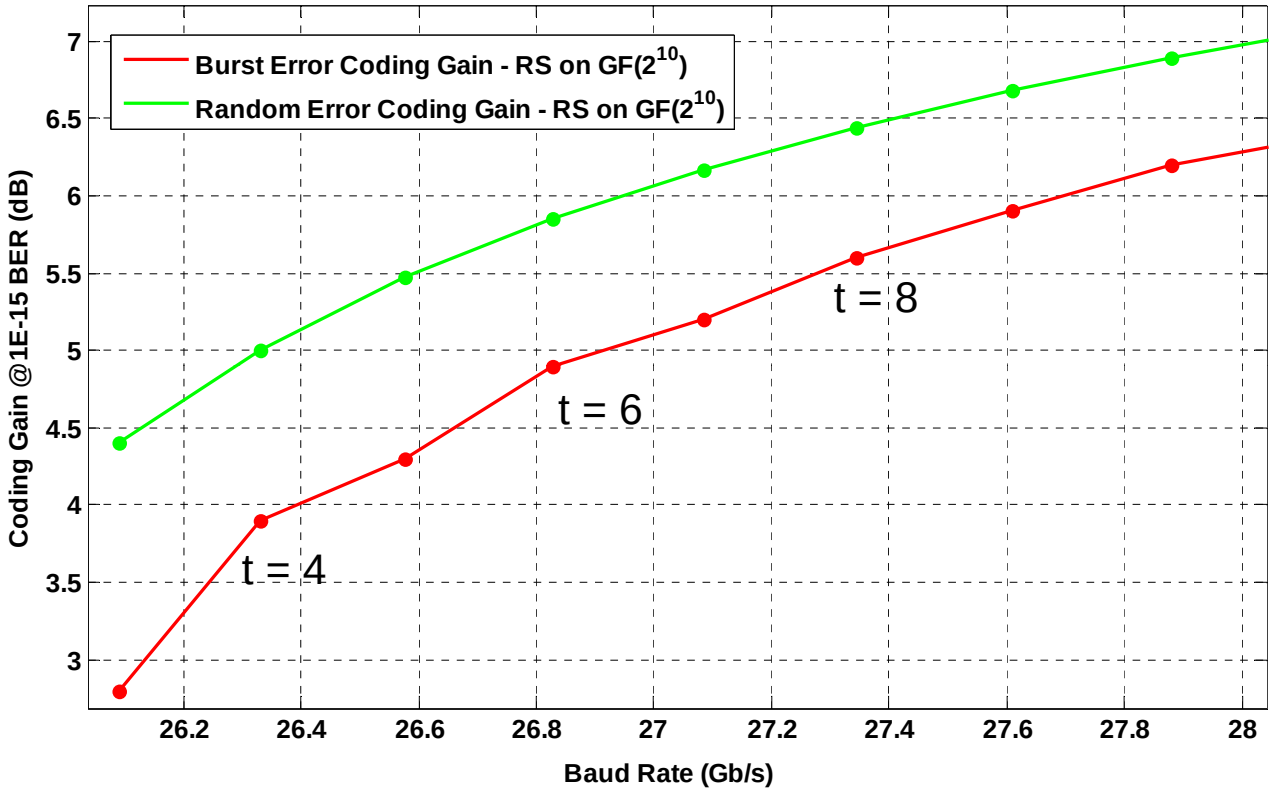
- FEC codes[1] with about 6% over-clocking and latency < 100ns, NCG > 5dB, etc have been previously proposed
  - Some applications desire even lower (end-to-end) latency
- Striping[2] across physical lanes is required for lowest latency
  - For compatibility with gustlin_02a_0511 source data size needs to divide the Alignment marker repetition rate (16384x20x65b)
  - Output size needs to be a multiple of 4 so it can be striped across 4 lanes
  - Allows skew compensation and FEC frame lock with 802.3ba PCS alignment markers
- It is desirable to have a source data size of 65 bits

DFE burst errors

- DFE's are well known to multiply errors in the feedback loop
  - A single error will become a burst error
- Consider NRZ 1 tap DFE with tap coeff = 1
  - If previous decision is wrong, then there is ½ probability of making a successive error
  - i.e. Probability of K consecutive errors = $(½)^k$
  - If DFE Input error rate = 1E-10, prob of 10 bit DFE error burst is ~1E-13
- Lower 1st DFE tap between 0.6 to 1 have similar burst length as tap coefficient of 1
  - Tap of 1: 0.5^k
  - Tap of 0.7: 0.49^k
  - Tap of 0.6: 0.42^k
- A single random error may consume multiple Reed Solomon symbols
  - Burst error coding gain is lower than coding gain for random errors

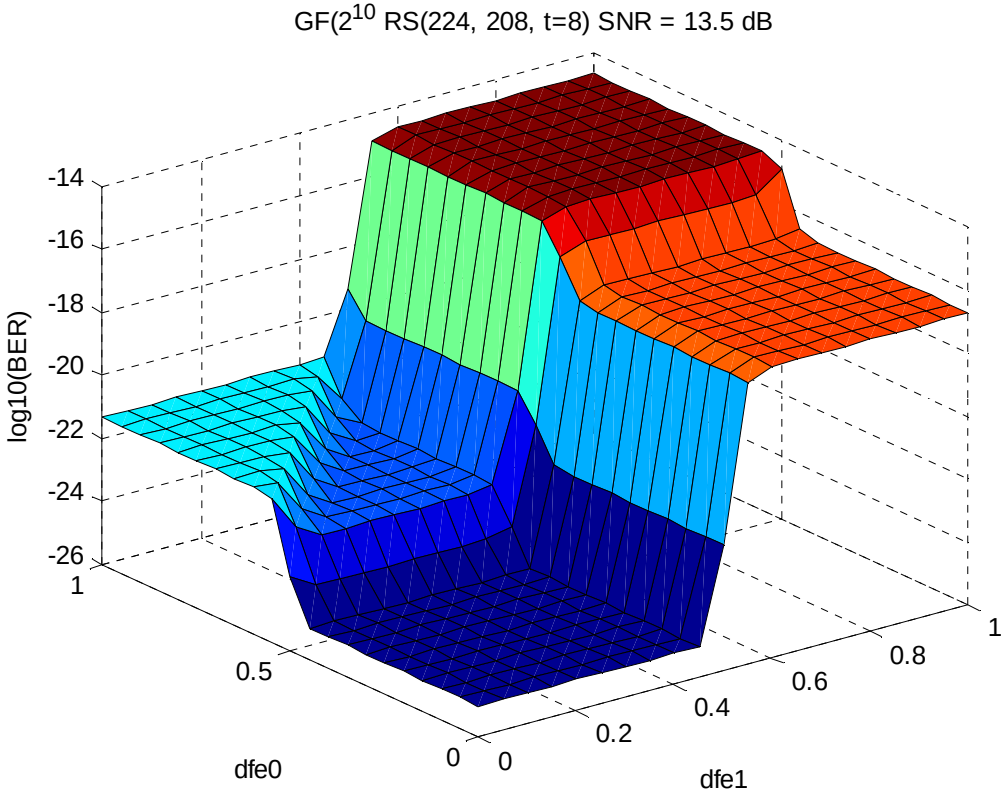


DFE Burst Error vs. Random Error Coding Gain



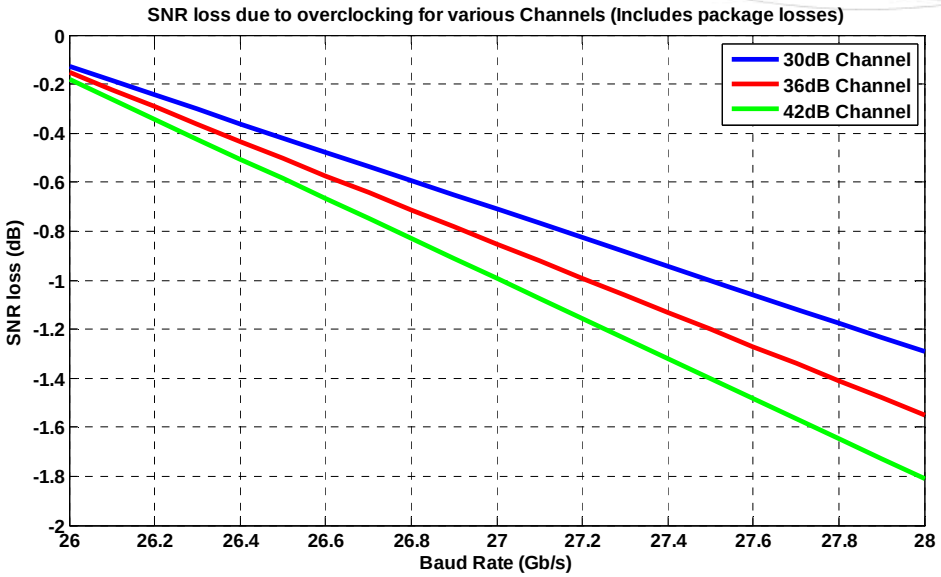
- As rate increases the delta between random errors and burst errors narrows from 1.6dB to 0.8dB
- Block size is 2240 bits

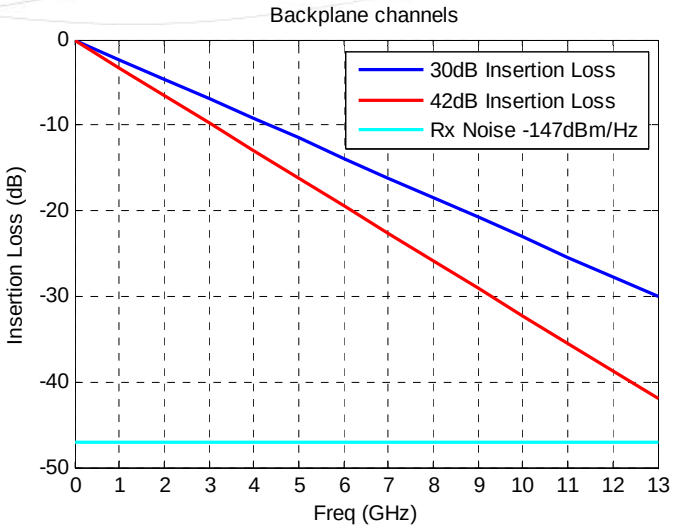
BER impact of burst errors – 2 tap DFE



- Computes burst statistics for DFE burst error events
- NRZ 2 tap DFE with taps [1 0.45] has similar burst statistics as [1 0]
- Simulations on 25G NRZ channels show
  - DFE burst statistics of 1 tap DFE with tap coeff = 1 is good proxy for channel ensemble

SNR Loss due to Over clocking





MMSE DFE SNR ≈ $(SNR_{0\ GHz} + SNR_{12.9\ GHz})/2$

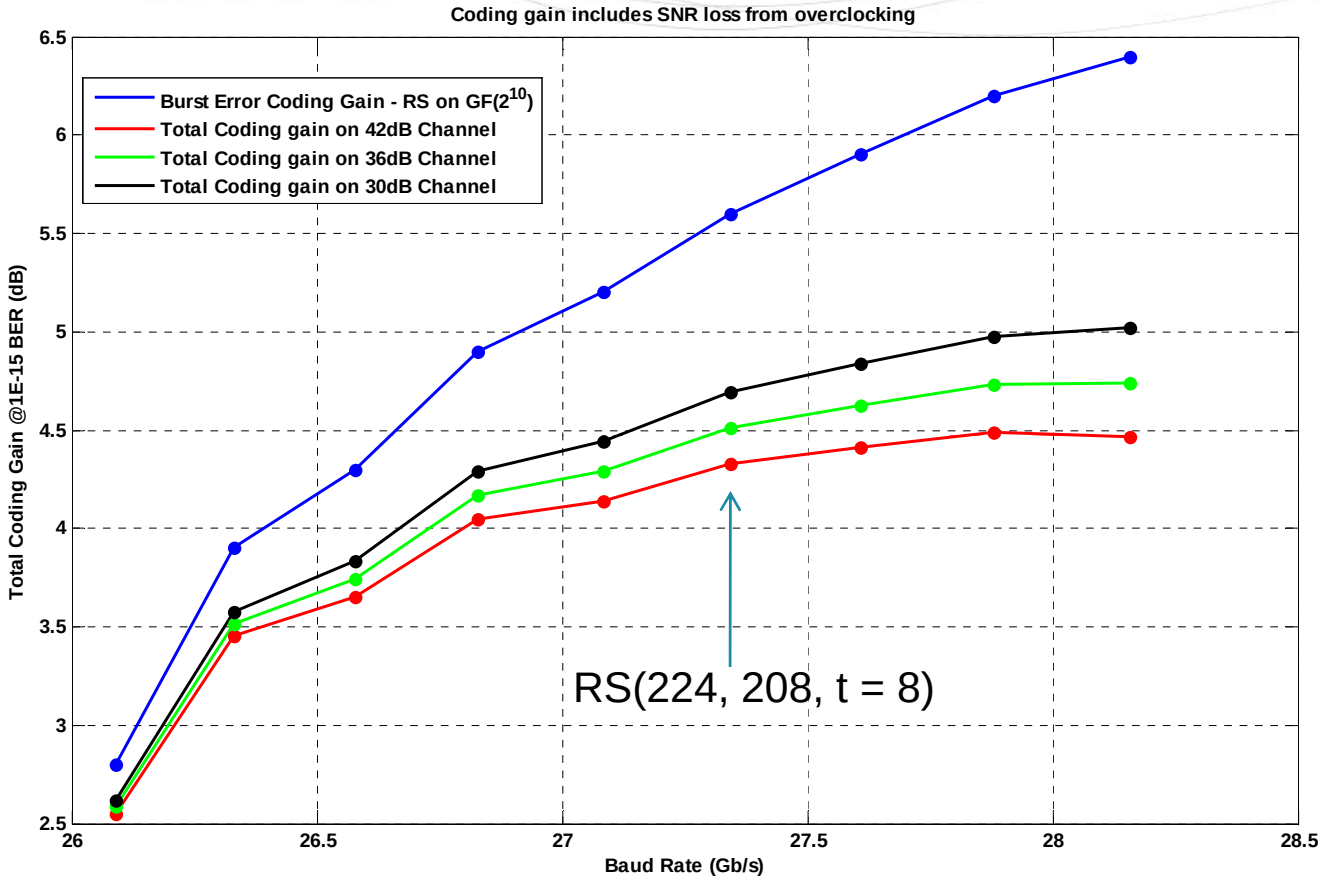
For baud rate of Fb, the SNR loss due to over clocking

- $SNR_{delta} = (IL_{Fb/2\ GHz} - IL_{12.9\ GHz})/2$

For Channels whose loss is linear in frequency and for a FEC Overhead of OH

- $SNR_{delta} = (IL_{12.9\ GHz} * (1+ oh) - IL_{12.9\ GHz})/2$
- $SNR_{delta} = IL_{12.9\ GHz} * oh / 2$

Total Coding Gain



- Total Coding gain = Burst Error Coding gain - Over Clocking SNR loss
- Results suggest 27.34 Gb/s (6% Overhead) as a good design point
  - RS(224, 208, t = 8)
  - Specific parameters chosen for compatibility with gustlin_02a_0511 proposal

Baseline Proposal: RS(224, 208, t = 8) over 10 bit symbols

- Rate is 27.34375 Gb/s, 6% over clocking, 4.5dB Coding gain for a 36dB at Nyquist channel
- Over clocking assumes compressing sync bits. Block size is 2240 bits
- Intrinsic block latency is 20.48ns for striping across physical lanes
  - Processing latency is ~2-3x block latency. Expect <50ns latency
- RS(224, 208) chosen to be compatible with gustlin_02a_0511
  - Input Data size of 2080 bits divides Alignment marker repetition rate
  - Output size can be striped across 4 lanes
- Gearbox is 165 to 175. Reference clock is156.25MHz

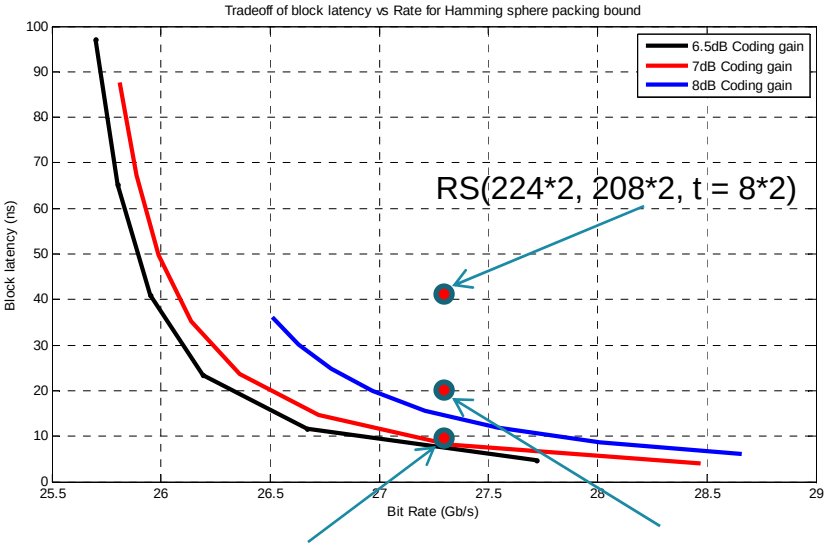
	Delta (dB)	Coding Gain (dB)
Random Error		6.43
DFE Burst Error Penalty	-0.83	5.6
36dB Channel 6% over clocking loss	-1.09	4.5

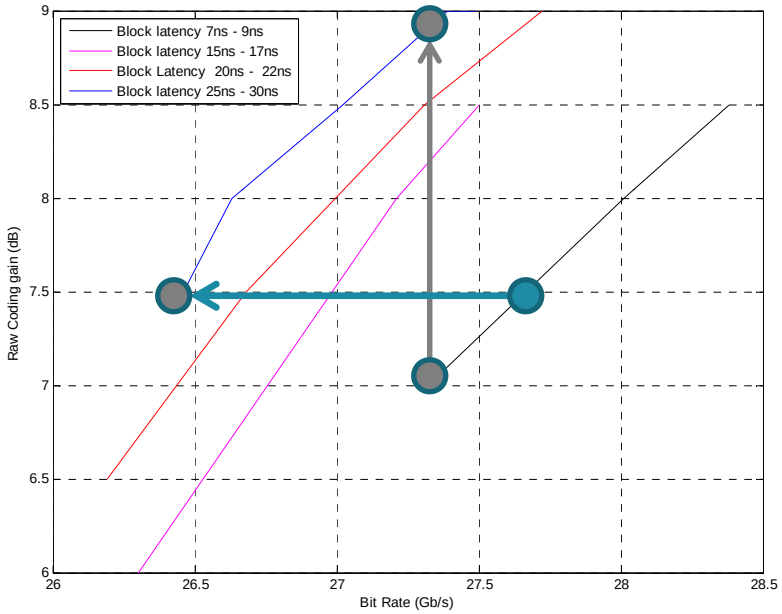
Channel loss includes package loss.

Triple tradeoffs

- Choice of code parameters involves a triple tradeoff
  - Latency
  - Coding gain
  - Over clocking (higher Baud rate)

See Gustlin_01_0311.pdf





RS(224*0.5, 208*0.5, t = 4)

RS(224, 208, t = 8)

- Theoretical limits show block latency increasing sharply for rate <26.75 Gb/s
- Proposed Reed Solomon codes are compared to theoretical latency limits
  - 27.34Gb/s RS(224, 208, t = 8) over GF(2^10) at ~2x latency limit
  - It is desirable to reuse the 27.34Gb/s rate to explore the tradeoffs

Exploring the triple tradeoff, Latency vs. Coding gain for 10 bit symbol

RS(448, 416, t = 16)	Delta (dB)	Coding Gain (dB)
Random Error		7.34
DFE Burst Error Penalty	-0.47	6.87
36dB Channel 6% over clocking loss	-1.09	5.78 (<100ns total latency)

RS(112, 104, t = 4)	Delta (dB)	Coding Gain (dB)
Random Error		5.24
DFE Burst Error Penalty	-1.49	3.75
36dB Channel 6% over clocking loss	-1.09	2.66 (<25ns total latency)

- Two options that double and halve the block latency compared to RS(224, 208, t = 8) baseline are proposed
  - Same rate 27.34375Gb/s. They can be set during training (ex: CL72 in 10GKR)
  - Block latency ~41ns (+1.3dB) and ~10ns (-1.8dB) compared to ~20ns for baseline proposal

Mean Time To False Packet Acceptance (MTTFPA)

- Assume any FEC block known to be in error is marked. (10G KR supports this)
- The probability of a RS false decode (i.e. outputting a false codeword) is 1/t! where t is the strength of the code
  - The output codeword will generally contain 2t + 1 errors
- Ethernet CRC32 cannot guarantee detection for 2t + 1 errors
  - A false CRC32 match is random with probability 2^{-32}
- If FEC BER objective is 1E-12 then
  - Probability of false codeword acceptance (Pf) = Prob of RS false decode * FEC BER Objective * 2^{-32}
- Baseline Option: RS(224, 208, t = 8)
  - Pf = 5.77E-27. MTTFPA = 1/Pf * 1/ (27.34E9 * 4) * 1/ (60*60*24*365) years
  - MTTFPA = 50 Million years

Similar to 10GKR, the FEC proposed address MTTFPA issues due to DFE error propagation

Summary

- FEC solves MTTFPA issues due to DFE error multiplication
- The FEC code proposed adds noise margin or 9dB insertion loss over a conventional DFE Equalizer
  - RS(224, 208, t = 8) Symbol size = 10. Baud rate=27.34375Gb/s, Over clocking = 6%
  - Gearbox is 165 to 175. Legacy compatible reference clock of 156.25MHz
  - Total Coding Gain = 4.5dB. Total Latency <50ns
  - Compatible with striping over physical lanes proposal in gustlin_02a_0511.pdf
  - Helps solve ~35dB BGA to BGA backplane for 1E-15 BER
- For rates < 26.75Gb/s the FEC latency increases sharply
- For rates > 27.5Gb/s the FEC coding gain flattens due to SNR loss
- Optionally a lower latency or higher coding gain FEC can be supported
  - The two options are derived from the baseline proposal. Both options run at 27.34375Gb/s
  - Total latency <100ns (+1.3dB) and <25ns (-1.8dB) respectively

References

1. wang_01_0511, “Feasibility of 100G KR FEC”
2. gustlin_02a_0511, “FEC Striping Options for 100 Gb/s Backplane and Copper Study Group”