A Preliminary Proposal for PAM-4 TX Specification

for IEEE 802.3
100Gbps over backplane and copper cable task force

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Will Bliss, Broadcom Corp.
Kent Lusted, Intel Corp.
Vasu Parthasarathy, Broadcom Corp.
Supporter; Matt Brown, Applied Micro

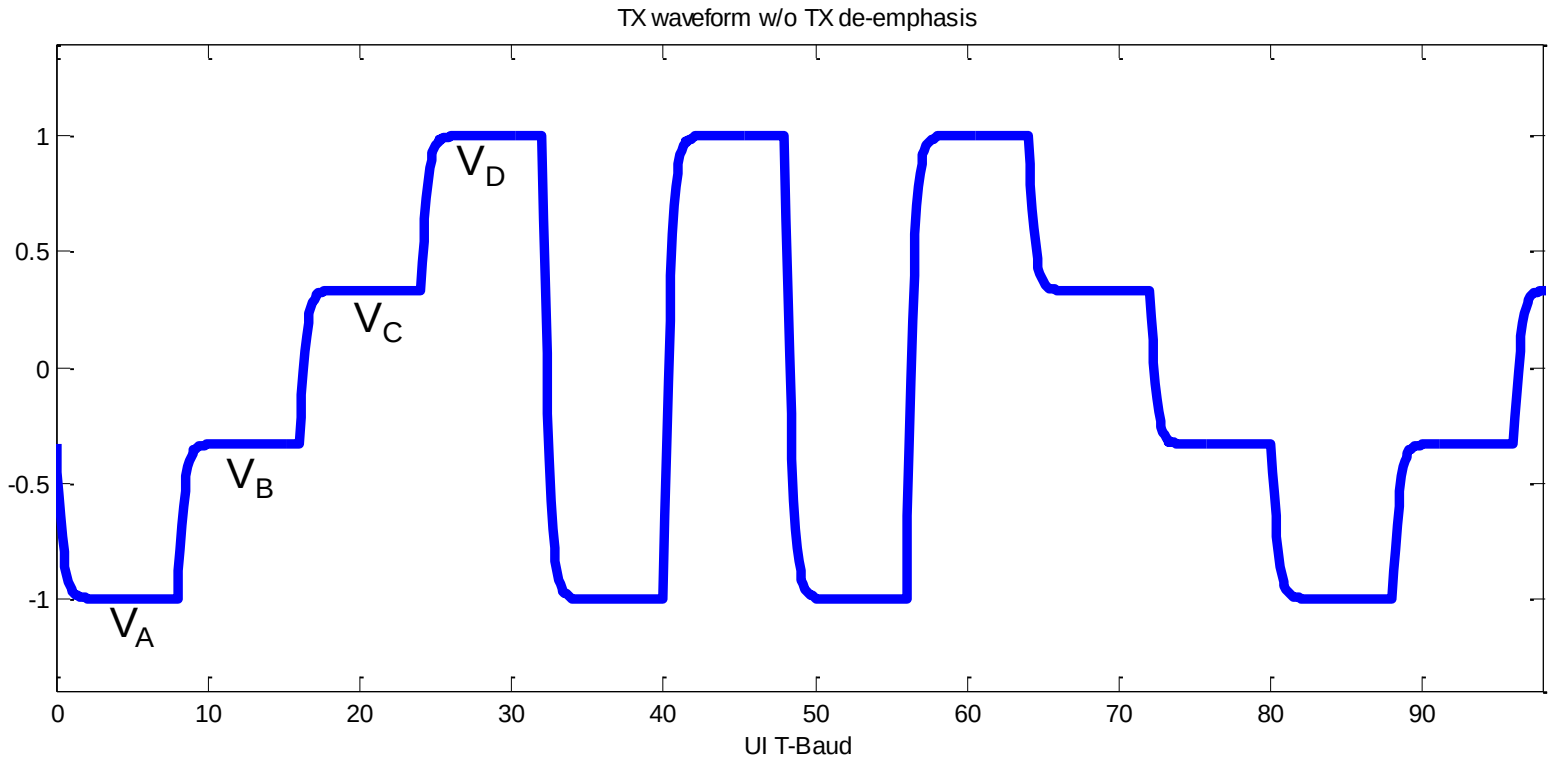
Motivation and Proposal

- Address concerns from some participants that “PAM-4 is too difficult to test and qualify”
- Leverage all the TX tests from 10GBASE-KR
  - NRZ is a proper subset of PAM-4, so all NRZ tests can be reused
    - Tj, Rj, and Dj tests using PRBS9 (or PRBS31)
    - TX De-Emphasis ratios using SQUARE8
    - DCD, Peak Amplitude, and Signaling Rate using SQUARE1
- Add a single new test waveform for PAM-4
  - Requires one extra scope capture and post-processing

Scaling of 10GBASE-KR TX Specifications

- Baud Rate Scaling by 10 /12.5 = 0.8 of 10GBASE-KR
  - Rise Times scaled down to 19 – 38 psec
    - May want to reduce by any FEC overclocking to track actual Baud Rate (small effect)
- Bit Rate Scaling by 10/25 = 0.4 of 10GBASE-KR
  - Rj (Random Jitter) spec was 0.15 UI 'worst case' (prob. 1e-12) for NRZ
    - Change to 0.15 of 'bit Period' (not Baud Period)
      - 0.075 UI for the new PAM-4 'UI', so same actual jitter spec in psec as an equal data rate NRZ system
      - Derivation to be given in presentation "Eye diagrams for PAM-4 and NRZ"
  - Dj and Tj scale (similar to RJ) with bit rate, so 0.4
    - Same physical Dj and Tj in psec as NRZ at the same user rate
  - DCD (Duty Cycle Distortion) similarly scales with bit rate
    - Equal asymmetry in psec as NRZ at 25Gbps

A Proposed TX Stairstep Test Waveform for PAM-4



- **PAM-4 test waveform is period 80T with stair steps up, stair steps down, and full swing transitions**
- **Each transmitted level is of duration 8 Baud periods**
- **Each transmitted level is measured after 3-7 Baud periods of settling**

TX Specification for PAM-4 Levels

- The most important specification for PAM-4 is that the four levels (w/o TX de-emphasis) are approximately equally spaced, else low frequency Signal to Distortion Ratio (SDR) suffers
  - Define $V_{LOW} = (V_C - V_B)/2$
  - Define $V_{HIGH} = (V_D - V_A)/6$
  - Define $V_{AVG} = (V_{HIGH} + V_{LOW})/2$
  - Spec $|V_{HIGH} - V_D/3| < 0.06\ V_{AVG}$
  - Spec $|V_{HIGH} + V_A/3| < 0.06\ V_{AVG}$
  - Spec $|V_{LOW} - V_C| < 0.06\ V_{AVG}$
  - Spec $|V_{LOW} + V_B| < 0.06\ V_{AVG}$

V_{AVG} is the ~amount of noise voltage at the slicer that will cause an error

- More specifications can be tested with the single proposed waveform and capture
  - Symmetry between 'up' and 'down' steps
    - Rise and fall times
    - Duty cycle
  - Symmetry between steps of magnitude 2 and steps of magnitude 6
    - Rise and fall times the same

Disclaimer; this is a Preliminary Proposal

- Final specification tolerances need to be decided in the context of an overall SNR 'implementation loss' budget (which hasn't been discussed yet)
- Specifications and tests are best targeted at known and anticipated circuits problems (which haven't been discussed yet)
- This proposal isn't meant to preclude any additional functional tests, such as an 'overall wideband test'
  - E.g., Linearity fitting to a longer and random-like pattern
  - Such pass-fail tests can be very helpful, but frequently they don't help circuit designers understand requirements nor help them discover root causes of any failures

Summary

- A scaling of the 10GBASE-KR specifications for Rise time, Rj, Dj, Tj, and DCD was presented
- A proposal to add one test waveform and capture for PAM-4 was presented
  - A proposed set of specifications for PAM-4 accuracy was presented