

PAM-2 on a simulated 1 Meter Backplane Channel including manufacturing tolerance

Mike Dudek (Qlogic)

Scott Kipp (Brocade)

Pravin Patel (IBM)

Mike Li (Altera)

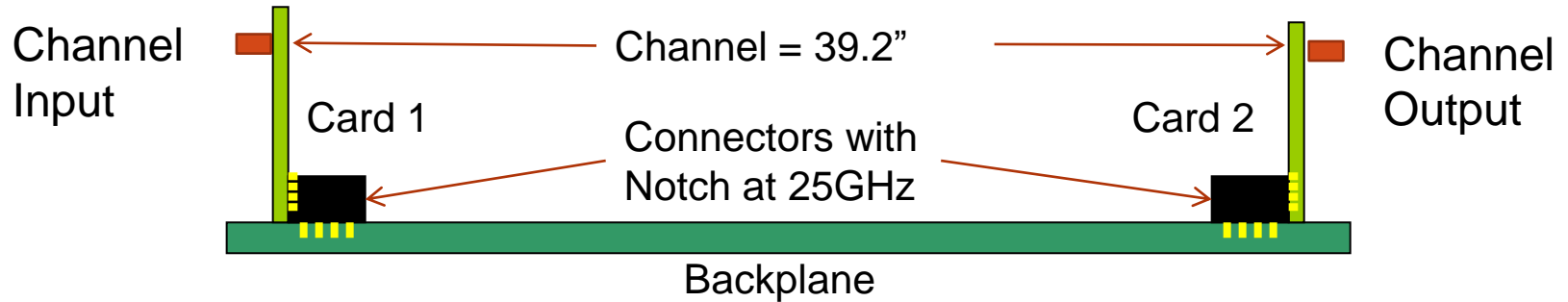
Karl Muth (TI)

Sept 2th, 2011

Meeting the 1 Meter Objective

- Patel_01_0911 shows that PAM-2 can operate over a 1 Meter measured backplane channel without FEC
- This presentation investigates the effect of printed circuit board manufacturing tolerances (10% impedance mismatch) and connectors with an insertion loss notch at 25GHz using a simulated channel
- It shows simulations from three companies with an open eye indicating that PAM-2 can handle these degradations
- This channel will be available on the 802.3bj website at:
 - <http://www.ieee802.org/3/100GCU/public/channel.html>
- We encourage other companies to verify the results with their simulations

1 Meter Backplane simulated degraded Channel

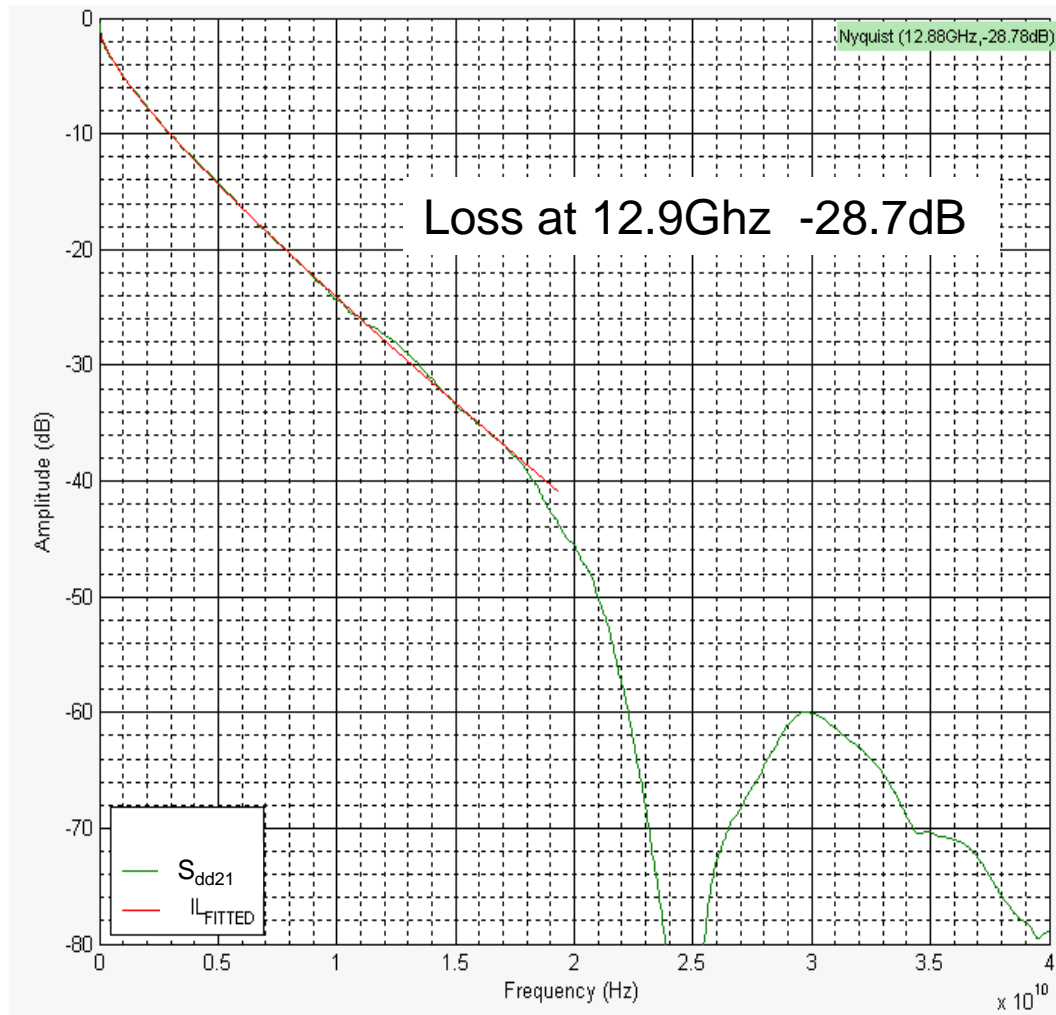


	Card 1	Backplane	Card 2
Length	5.1"	29"	5.1"
Board Impedance (mils)	110	90	110

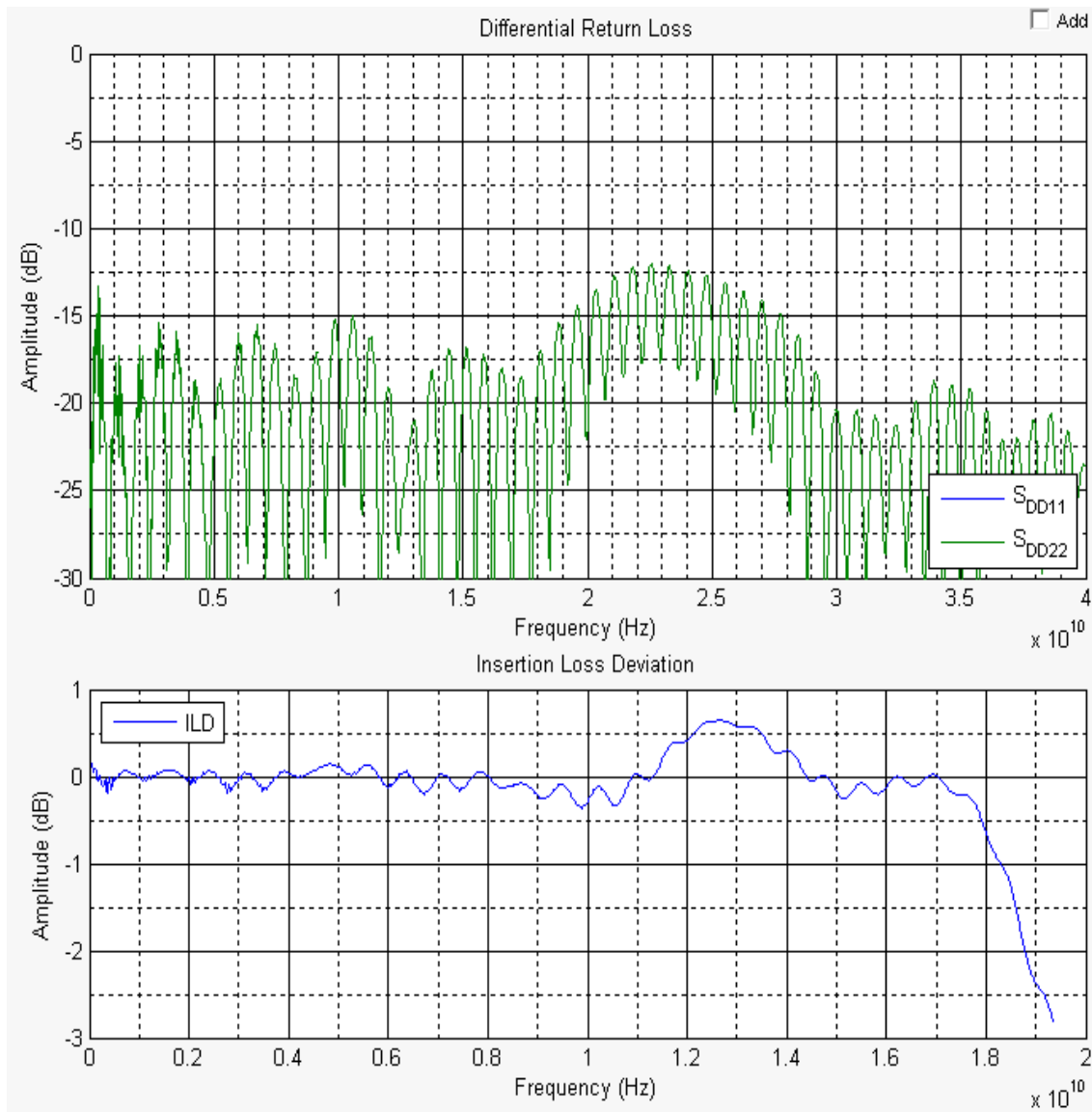
No pair-to-Pair Coupling in PCB's

Responses of 1.0 Meter degraded Channel

Differential Insertion Loss

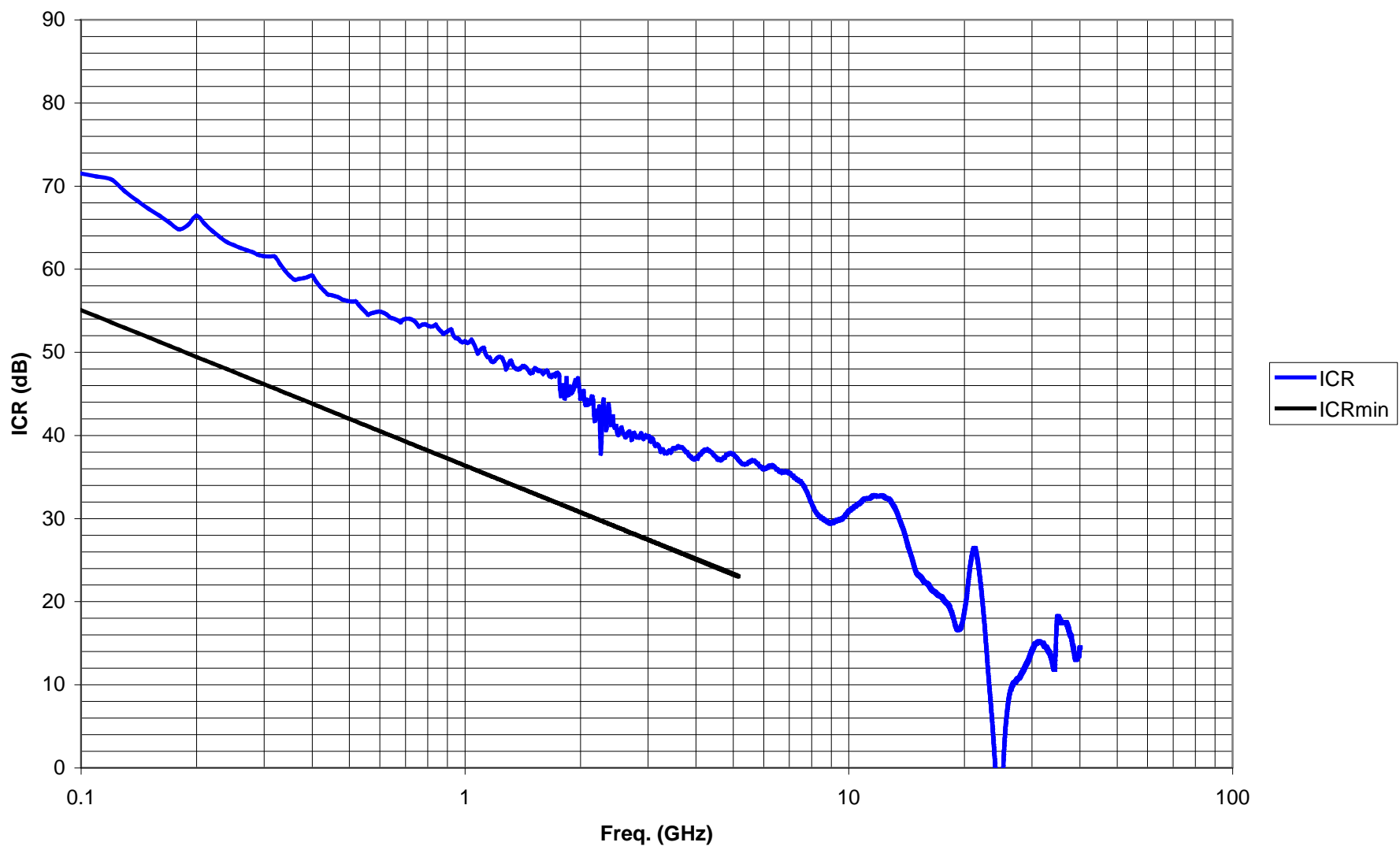


Responses of 1.0 Meter degraded Channel

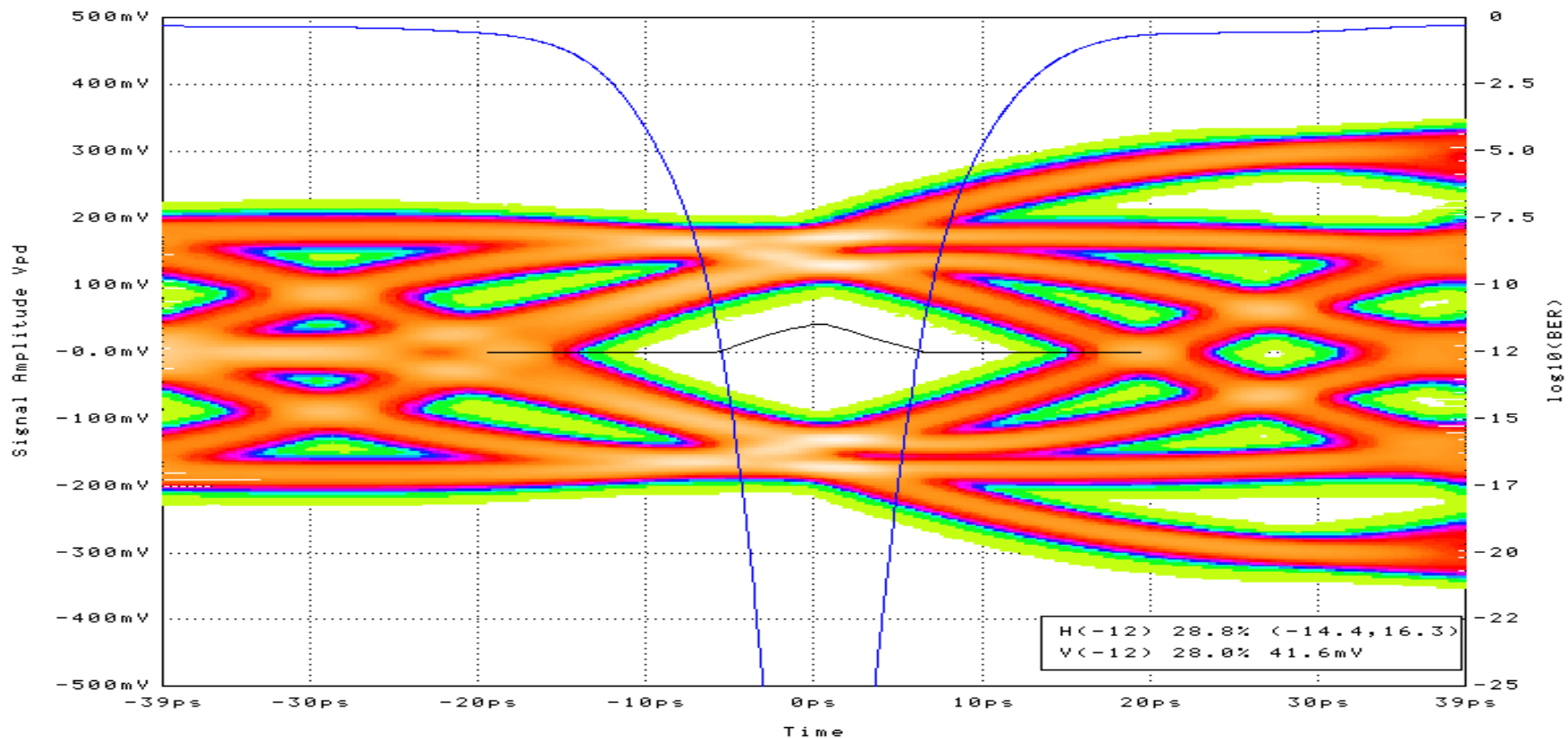


Responses of 1.0 Meter degraded Channel

Insertion Loss to Crosstalk Ratio

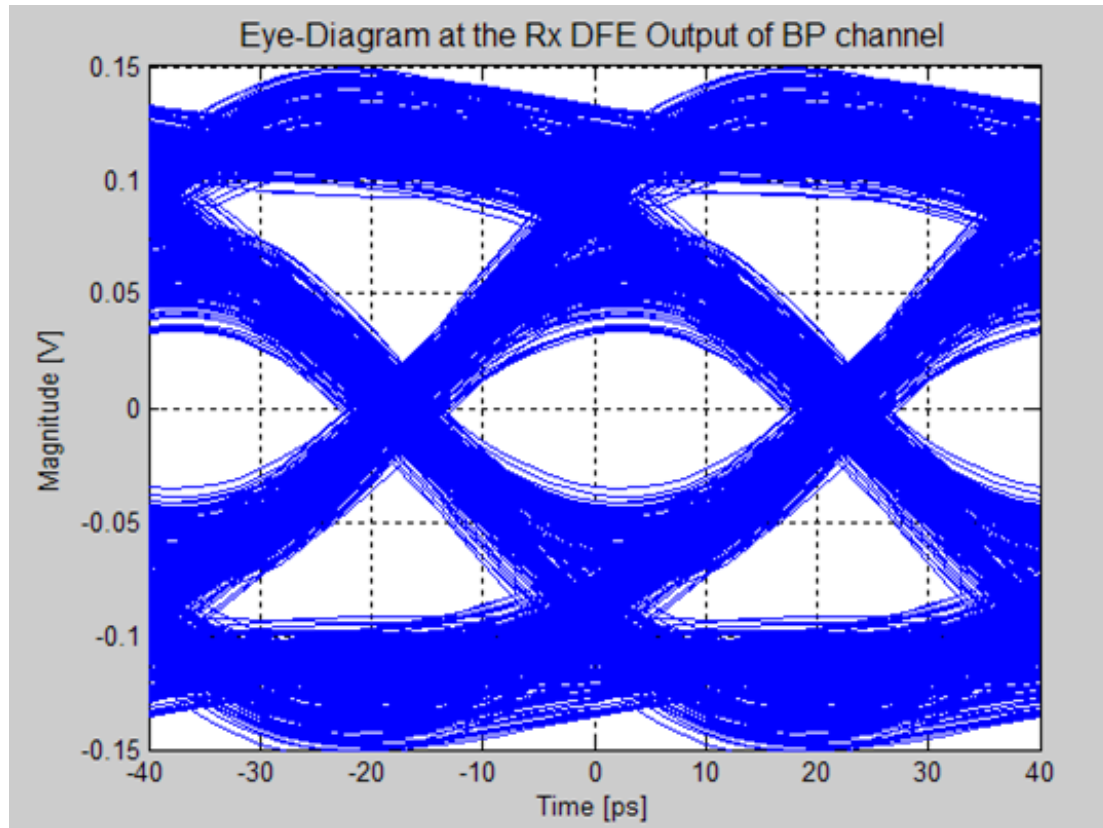


IBM SERDES Simulation Results for the 1 m degraded channel



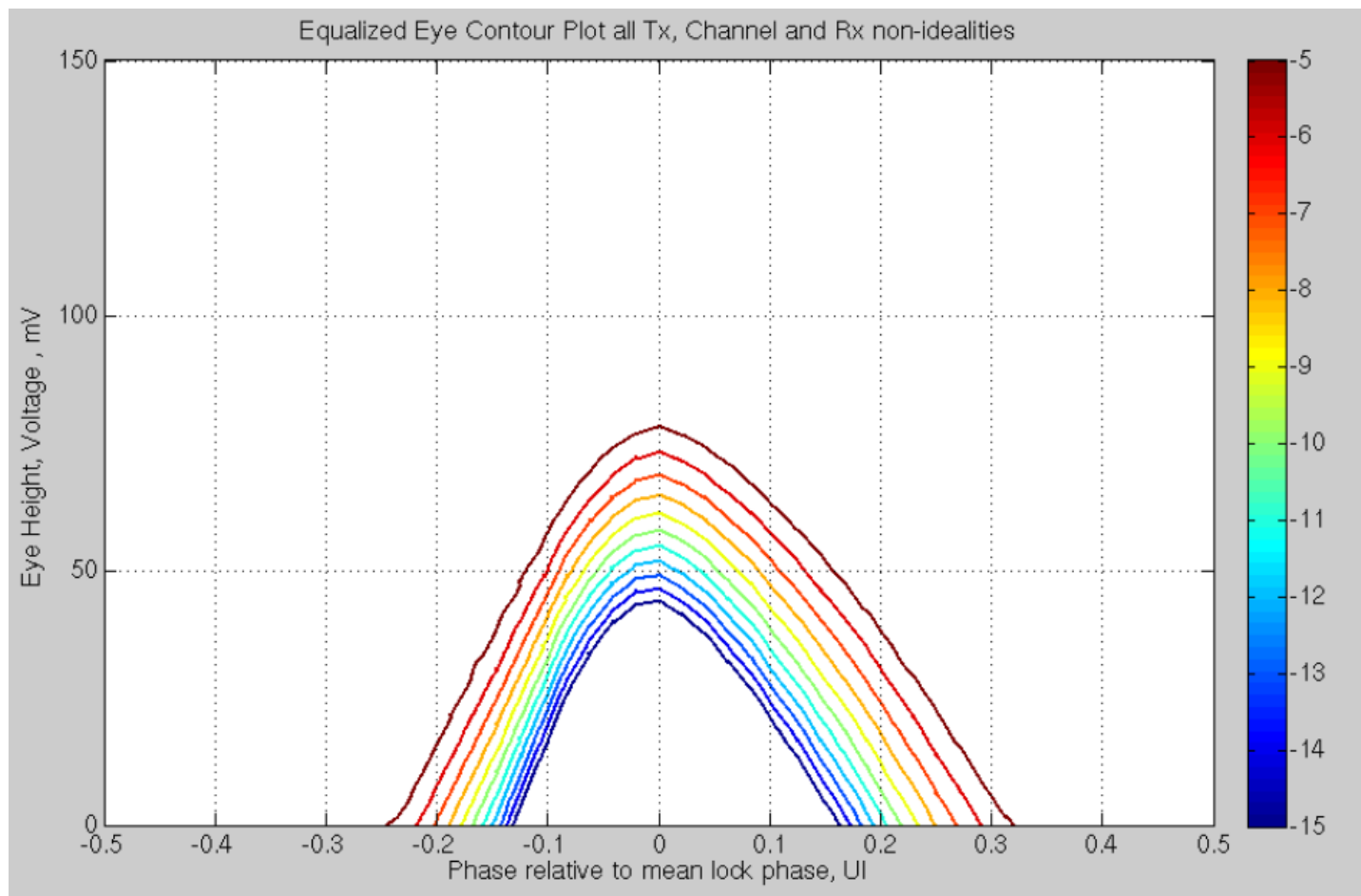
Channel Length (meter)	Vertical EYE (1E-12)	Horizontal EYE (1E-12)	VerticalEYE (1E-15)	Horizontal EYE (1E-15)	Meet IEEE 1M Backplane Objective
1.0	41.6mV	28.8%	36.4mV	24.8%	Yes

Altera SERDES Simulation Results for the 1 m degraded channel



Channel Length (meter)	Eye Height (1E-12)	Eye Width (1E-12)	Eye Height (1E-15)	Eye Width (1E-15)	Meet IEEE P802.3bj 1 m Length and 1e-12 BER Objective
1.0	40.3 mV	0.534 UI	36.06 mV	0.509 UI	Yes

TI SERDES Simulation Results for the 1m BP (PAM-2 Signaling)



Channel Length (meter)	EYE (1E-12)	Horizontal EYE (1E-12)	Vertical EYE (1E-15)	Horizontal EYE (1E-15)	Channel Loss @12.5Ghz dB	Meet IEEE 1M Backplane Objective
1.0	52.1mV	34%	42.9mV	29%	-28dB	Yes

Conclusion and Summary

- This presentation has shown that PAM-2 on a 1m channel without FEC is resilient to the effects of typical manufacturing tolerance of printed circuit board impedance and an insertion loss notch at 25GHz.

Reference Material

1. Troy Beukema, "Line signaling performance comparison on extended loss backplanes", July 2011, Ethernet Alliance
--- http://www.ethernetalliance.org/events/technology_exploration_forums/tef_presentations.
2. Mike Li, "A Study of 25 Gbps Signaling Over Complied 10G-KR Channels", May 2011, IEEE 802.3 100Gb/s Ethernet Electrical Backplane and Twinaxial Copper Cable Assemblies Study Group Interim Meeting
---- <http://ieee802.org/3/100GCU/public/may11/index.html>
3. TI simulation parameters. [Analog-DFE-based 16Gb/s SerDes in 40nm CMOS that operates across 34dB loss channels at Nyquist with a baud rate CDR and 1.2Vpp voltage-mode driver](#)
Joy, A.K. Mair, H. Hae-Chang Lee Feldman, A. Portmann, C. Bulman, N. Crespo, E.C. Hearne, P. Huang, P. Kerr, B. Khandelwal, P. Kuhlmann, F. Lytollis, S. Machado, J. Morrison, C. Morrison, S. Rabii, S. Rajapaksha, D. Ravinuthula, V. Surace, G.
Page(s): 350 - 351
settings used:
Signal data rate: 25.8 Gbps
Tx and Rx equalization capabilities
Tx: FIR 3-taps, 1 pre-, one post cursor
Rx: CTLE (15 dB max) + DFE (15-tap DFE)
Signal modulation: PAM-2
TI's Matlab simulation environment
Data pattern: prbs2^31-1, 6x2^20 bit
Vod: 1.2mVpp