Precoding proposal for PAM4 modulation

100 Gb/s Backplane and Cable Task Force
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**PAM4 DFE burst errors**

- DFE’s are well known to multiply errors in the feedback loop
  - A single error will become a burst error
- Consider PAM4 1 tap DFE with tap coeff = 1
  - If previous decision is wrong, then there is 3/4 probability of making a successive error
  - i.e. Probability of K consecutive errors = \((3/4)^k\)
- Lower 1st DFE tap between 0.6 to 1 have similar burst length as tap coefficient of 1
  - Tap of 1: 0.75^k
  - Tap of 0.7: 0.72^k
  - Tap of 0.6: 0.62^k
- A single random error may consume multiple Reed Solomon symbols
  - Burst error coding gain is lower than coding gain for random errors

![Graph showing error propagation and DFE tap values](image)
PAM4 DFE Burst Error vs. Random Error Coding Gain

- Block size is 2240 bits
- Severe coding gain loss due to long DFE burst error propagation
The burst error length of the DFE error events for PAM4 can be reduced by using precoding.

PAM4 Tx precoding uses a $1/(1+D)$ mod 4.

- See bliss_01_0311, "Signaling Terminology; PAM-M and Partial Response Precoders"
  - Multilevel version of the duo-binary precoder
  - Rx uses a $(1+D)$ mod 4 after slicing

Simple to implement

Very low Complexity

Reduces 1 tap DFE burst error runs into 2 errors per error event

- One error at the entry, one error at the exit
1/(1+D) Precoding worked example

- Precoder Input : \text{tx}(n)
  - 2 2 2 2 0 3 2 0 1 3 3 0 0 0 0 2 3 0 3
- Precoder Output : \text{p}(n)
  - 0 2 0 2 2 1 1 3 2 1 2 2 2 2 2 2 0 3 1 2
- DFE, Slicer Output : \text{d}(n)
  - 0 1 1 1 3 0 2 2 3 0 3 1 3 1 3 0 3 1 2
- Error Event : \text{p}(n) – \text{d}(n)
  - 0 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 0 0 0 0
- Decoder Output after 1+D at Rx : \text{r}(n)
  - 2 1 2 2 0 3 2 0 1 3 3 0 0 0 0 3 3 0 3

Entry Error
Exit Error
**FEC performance for 1 tap DFE with 1/(1+D) mod 4 precoder**

RS on GF($2^{10}$). Block size 2240 bits

- The delta between burst error and random error is ~1.45dB with 1/(1+D) mod 4 precoding
For FEC baud rate of 13.67G, the SNR loss due to over clocking

\[ \text{SNR}_{\text{delta}} = \frac{(IL_{6.84\text{GHz}} - IL_{6.45\text{GHz}})}{2} = 0.9\text{dB} \]
1/(1+D) mod 4 Precoding + PAM4 Coding Gain
for RS(224, 208, t = 8) over 10 bit symbols

- Rate is 13.671875GBaud, 6% over clocking, 4.2dB Coding gain for Extended KR channel
- Over clocking assumes compressing sync bits. Block size is 2240 bits
- Intrinsic block latency is 20.48ns for striping across physical lanes
  - Processing latency is ~2-3x block latency. Expect <50ns latency
- RS(224, 208) chosen to be compatible with gustlin_02a_0511 FEC
  - Input Data size of 2080 bits divides Alignment marker repetition rate
  - Output size can be striped across 4 lanes
- Rate is 87.5 x reference clock of 156.25MHz

<table>
<thead>
<tr>
<th></th>
<th>Delta (dB)</th>
<th>Coding Gain (dB)</th>
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<tbody>
<tr>
<td>Random Error</td>
<td></td>
<td>6.6</td>
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<tr>
<td>DFE Burst Error Penalty</td>
<td>-1.5</td>
<td>5.1</td>
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<tr>
<td>Extended KR channel</td>
<td>-0.9</td>
<td>4.2</td>
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<td>6% over clocking loss</td>
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### 1/(1+D) mod 4 Precoding + PAM4 FEC gain results

<table>
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<th>RS(448, 416, t = 16)</th>
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<th>Coding Gain (dB)</th>
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<tr>
<td>Random Error</td>
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<tr>
<td>DFE Burst Error Penalty</td>
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<tr>
<td>Extended KR channel 6% over clocking loss</td>
<td>-0.9</td>
<td>5.4</td>
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<table>
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<th>RS(112, 104, t = 4)</th>
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<th>Coding Gain (dB)</th>
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<tr>
<td>Random Error</td>
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<tr>
<td>DFE Burst Error Penalty</td>
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<td>3.8</td>
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<tr>
<td>Extended KR channel 6% over clocking loss</td>
<td>-0.9</td>
<td>2.9</td>
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- **Two options that double and halve the block latency compared to RS(224, 208, t = 8) baseline are analyzed**
  - Same rate 13.671875GBaud. They can be set during training (ex: CL72 in 10GKR)
  - Block latency ~41ns (+1.2dB) and ~10ns (-1.3dB) compared to ~20ns for baseline proposal
Digital Receiver performance over KR-Compliant installed base

- 3 tap TX de-emphasis, 32 tap FFE, 1 tap DFE, Continuous time filter (CTF), 6 ENOB ADC, FEC & RS(224, 208), Precoding, 1E-12 target BER
- Full coverage on the installed base feasible with significant SNR margin
Summary

• DFEs may produce severe burst error multiplication
• $1/(1+D)$ mod 4 precoding helps break long DFE burst errors
• Precoding is very simple to implement
• Precoding + RS(224, 208) over GF($2^{10}$) FEC can achieve 4.2dB total coding gain with < 50ns total latency
• PAM4 at 13.7GBaud has sufficient margin over installed base