# PAM-2 on a 1 Meter Backplane Channel

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# Meeting the 1 Meter Objective

- The 1 meter objective is a lofty goal, but this presentation shows that PAM-2 (NRZ) is technically feasible on a measured channel without Forward Error Correction (FEC)
- This presentation shows simulations from multiple companies with an open eye over a 39.2” channel with two connectors and less then 30dB of loss budget
- This channel is available on the 802.3bj website at:
  - http://www.ieee802.org/3/100GCU/public/channel.html
    - (patel_02_0911.pdf)
- We encourage other companies to verify the results with their simulations

# 8023.bj Objectives

- Support full-duplex operation only
- Preserve the 802.3 / Ethernet frame format utilizing the 802.3 MAC
- Preserve minimum and maximum FrameSize of current 802.3 standard
- Support a BER of better than or equal to $10^{-12}$ at the MAC/PLS service interface
- Define a 4-lane 100 Gb/s backplane PHY for operation over links consistent with copper traces on "improved FR-4" (as defined by IEEE P802.3ap or better materials to be defined by the Task Force) with lengths up to at least 1m.
- Define a 4-lane 100 Gb/s PHY for operation over links consistent with copper twin-axial cables with lengths up to at least 5m.

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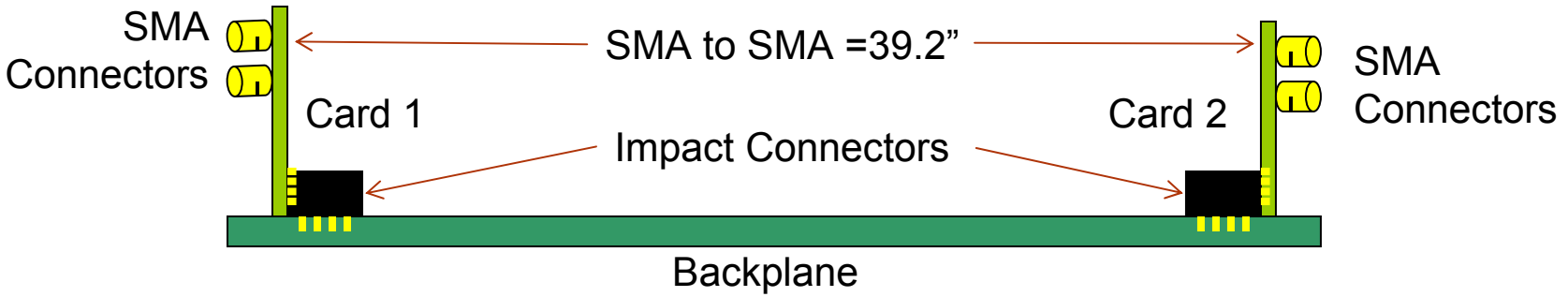
100Gb/s Backplane and Copper Cable Study Group

Objectives approved by IEEE 802.3 WG
July 2011 IEEE 802 Plenary

# 1 Meter Backplane Channel Construction:



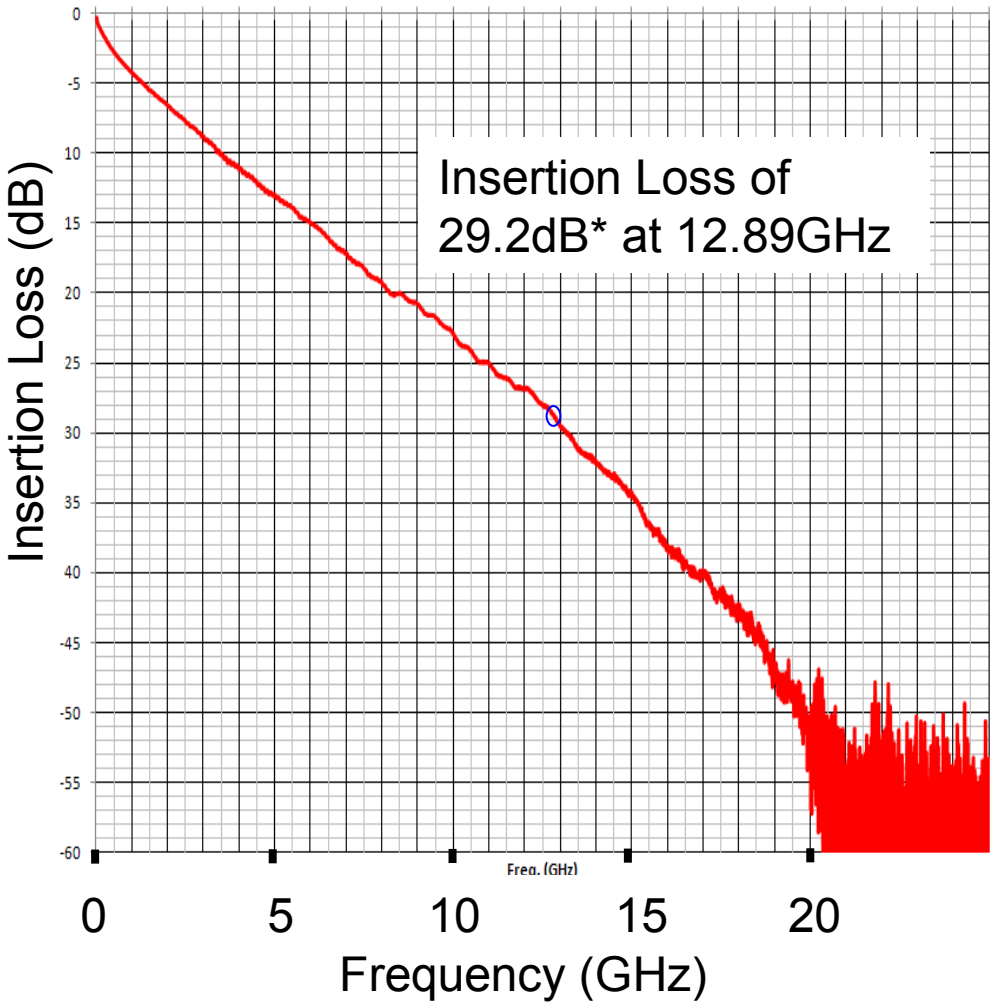

| | Card 1 | Backplane | Card 2 |
|---|---|---|---|
| Length | 5.1” | 29” | 5.1” |
| Board Thickness (mils) | 110 | 250 | 110 |
| Trace Widths/spacing/Width (mils) | 5.7/9.3/5.7 | 7.0/9.0/7.0 | 5.7/9.3/5.7 |
| Trace Copper Foil | VLP | HVLP | VLP |
| # of Layers | 14 | 26 | 14 |

**All Printed Circuit Boards:**

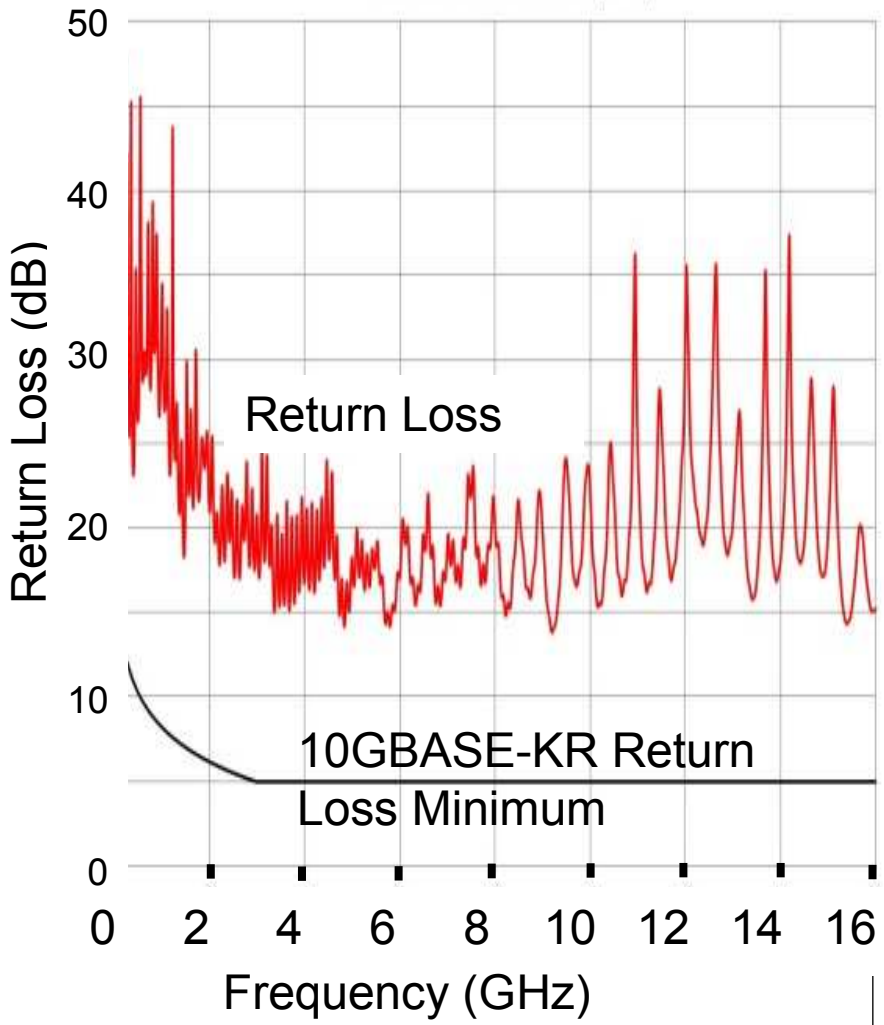
Signal Layer: 1 oz copper
Stripline: Yes
Material: Megtron 6
Via stub: ~ 10mil
Differential Impedance: 100 Ohm +/- 10%

# 1.0 Meter Channel Response (1 of 3)

## Insertion Loss

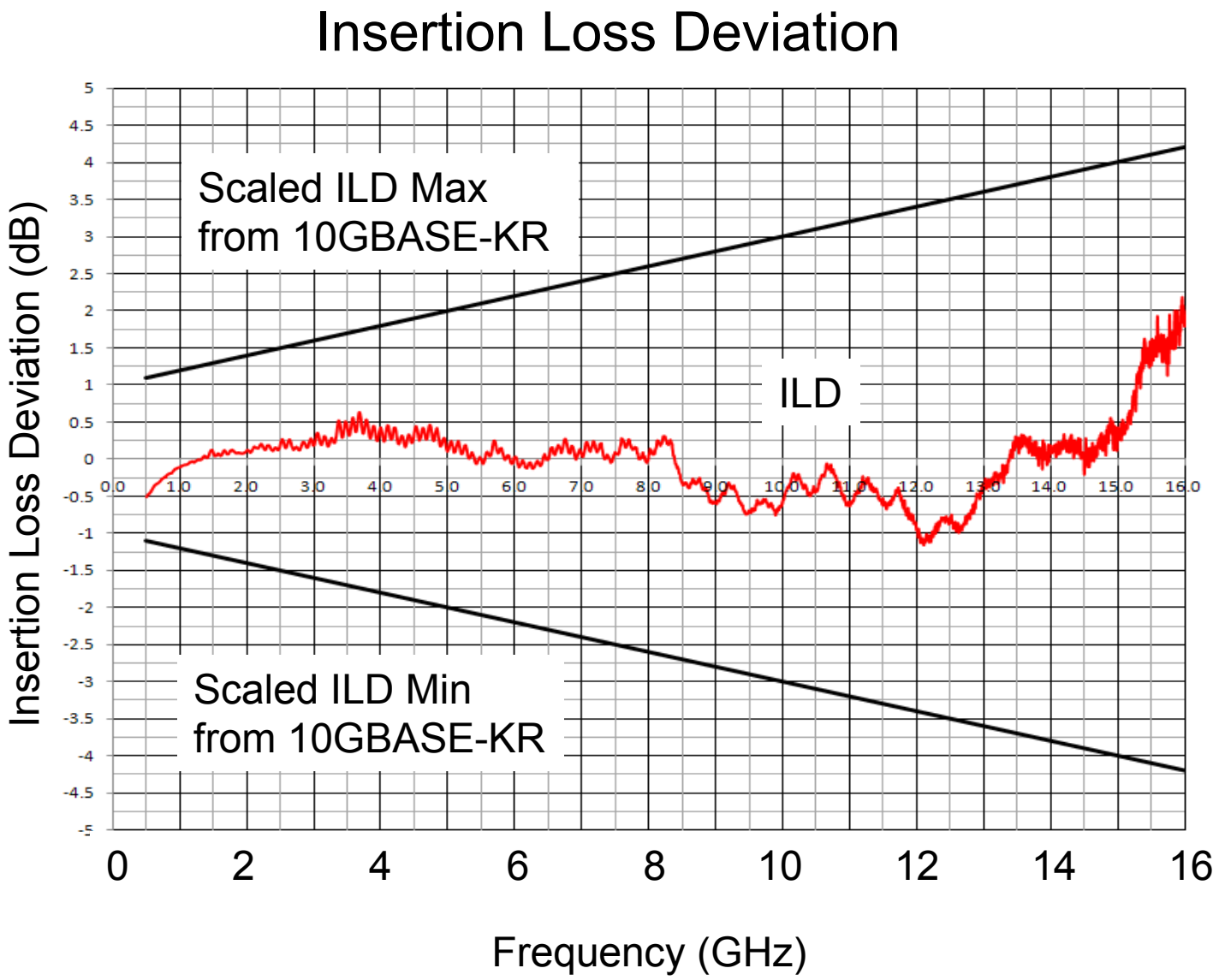



## Return Loss

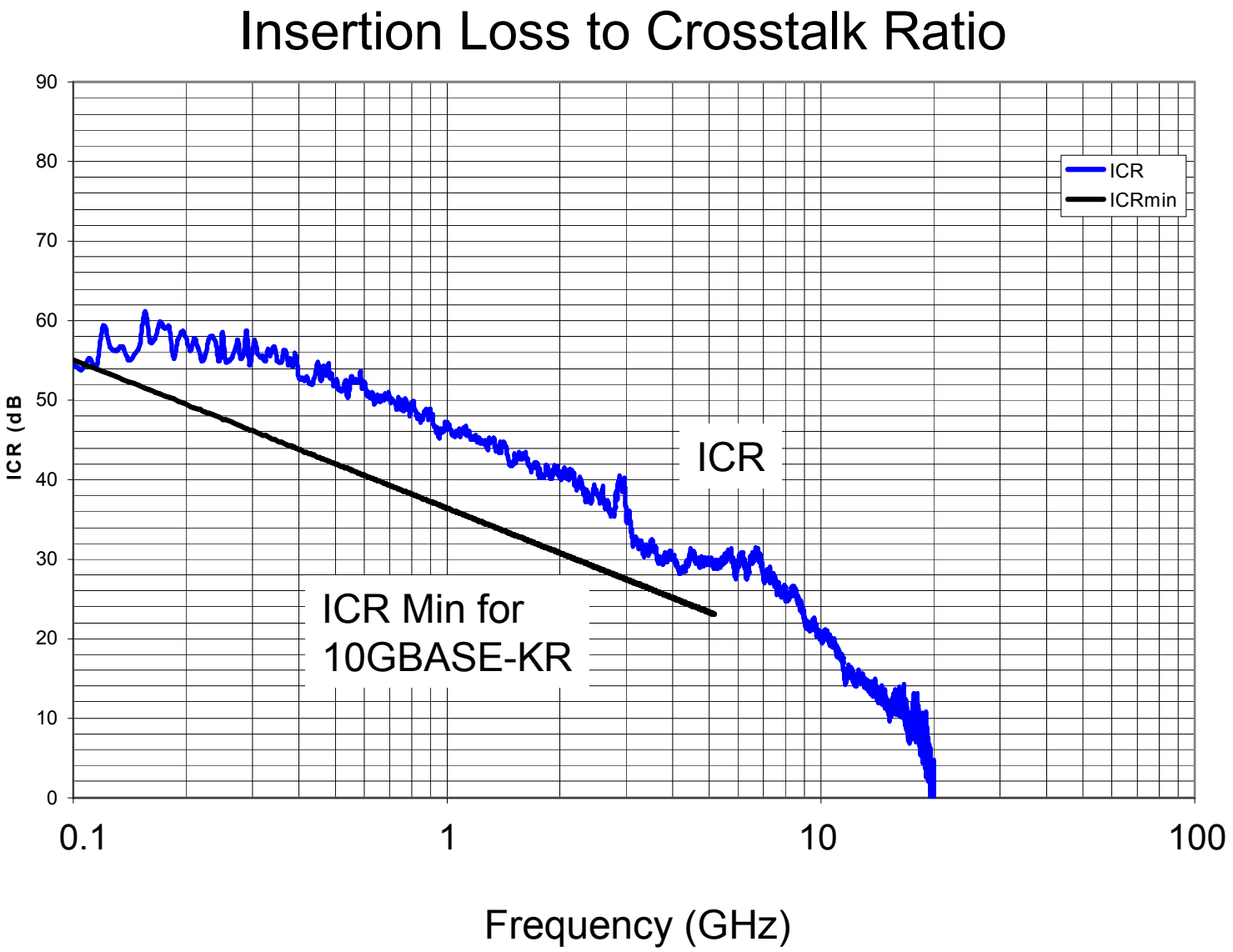



*The loss of this 1m channel is equivalent to the loss of a 29 inch “improved FR-4” channel (see Georgen_01_0511.pdf)

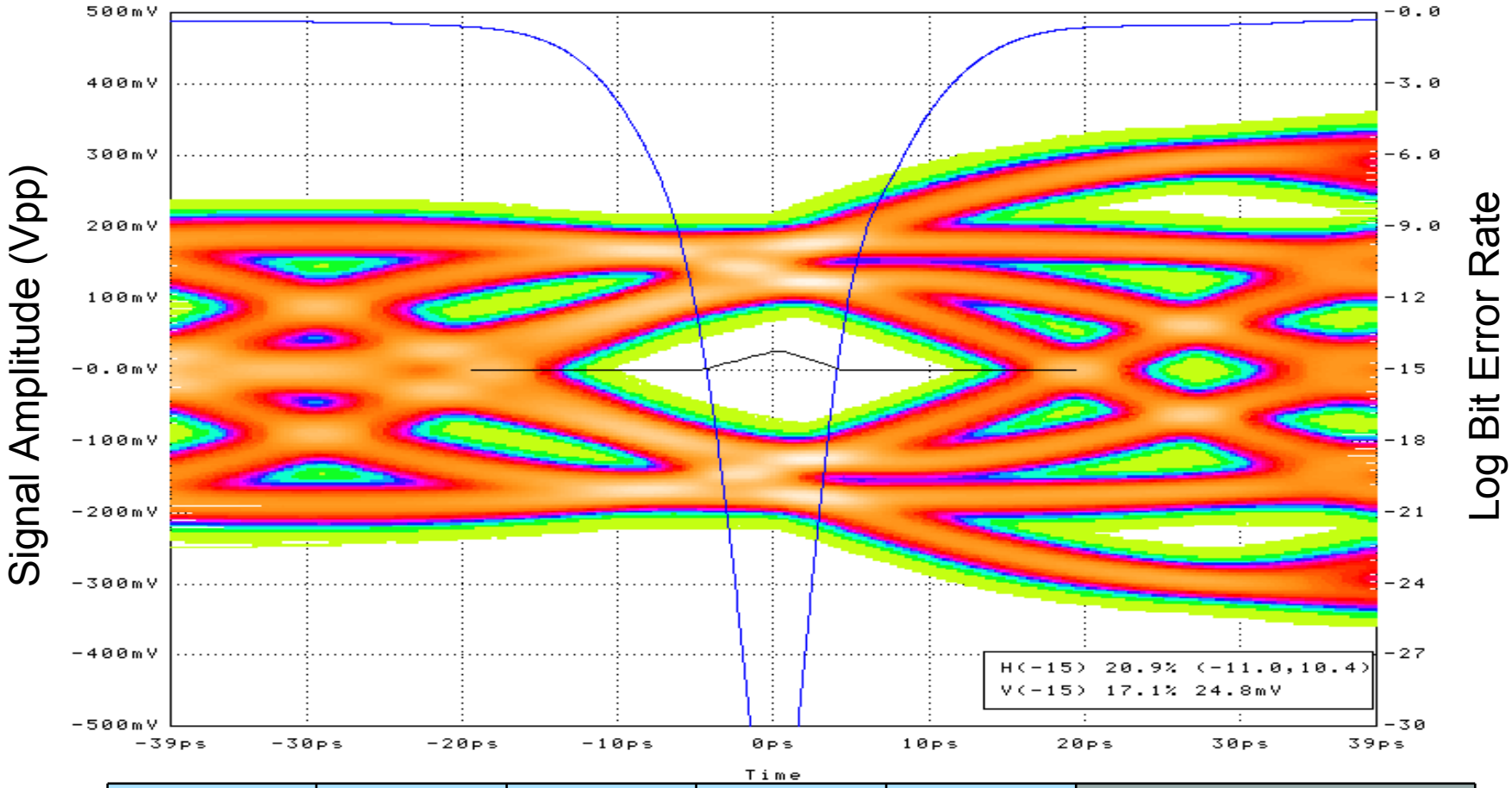
# 1.0 Meter Channel Response (2 of 3)



# 1.0 Meter Channel Response (3 of 3)



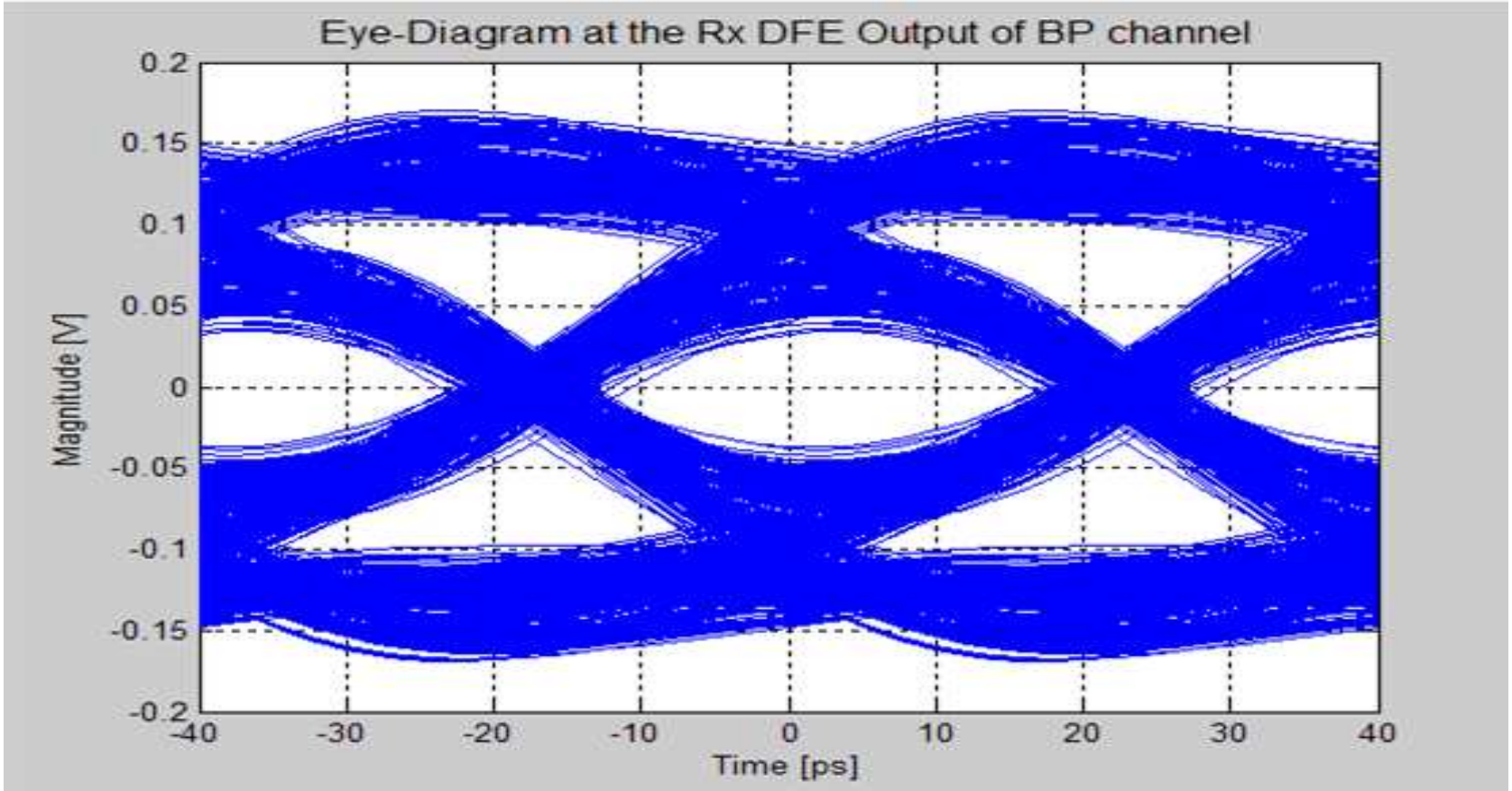
# IBM SERDES Simulation Results for the 1 m BP (PAM-2 Signaling)




| Channel Length (meter) | Eye Height (1E-12) | Eye Width (1E-12) | Eye Height (1E-15) | Eye Width (1E-15) | Satisfies 1 m and 1E-12 BER objective |
|---|---|---|---|---|---|
| 1.0 | 29.4mV | 24.7% | 24.8mV | 20.9% | Yes |

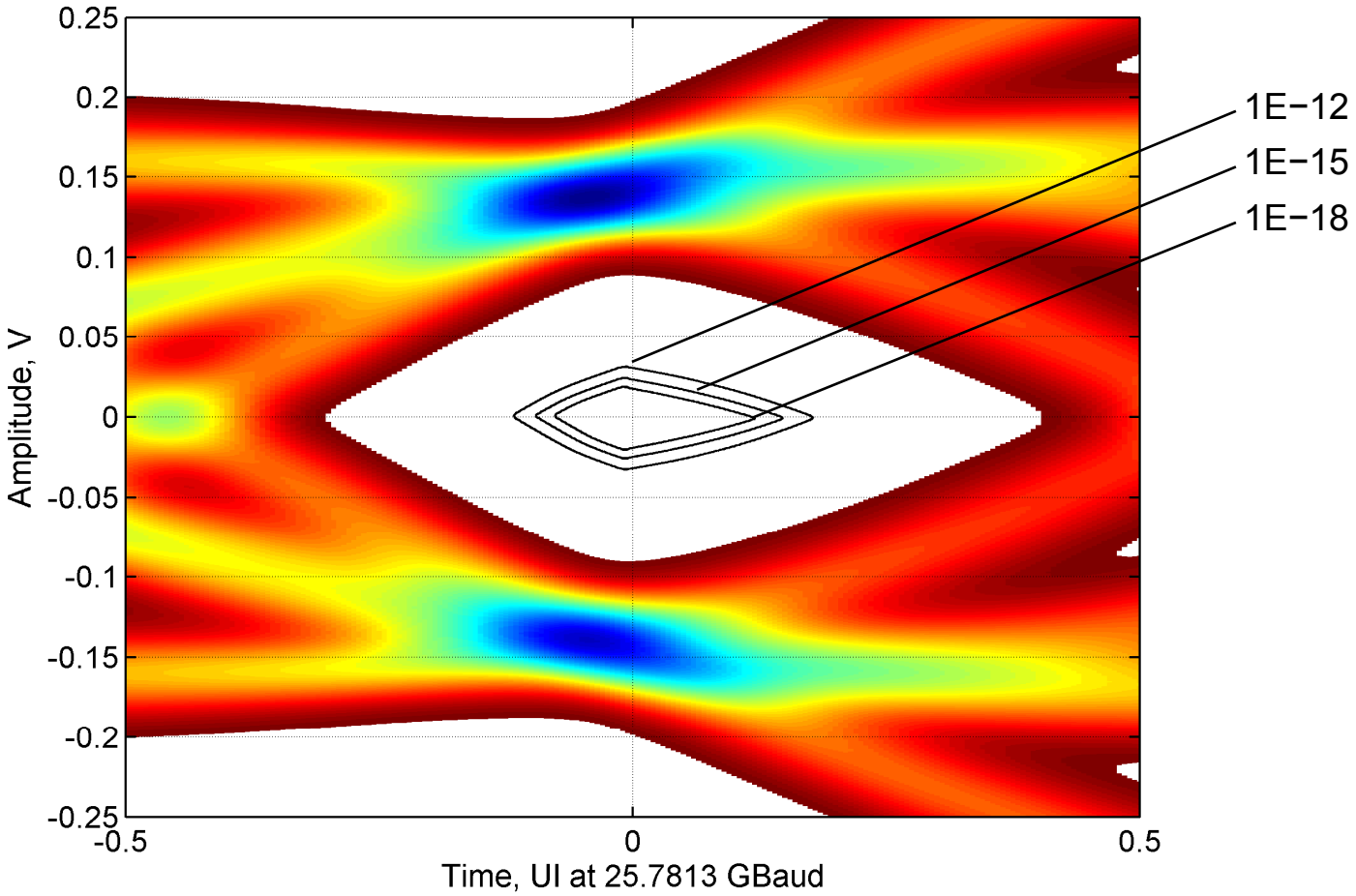
Simulation condition: Reference 1

# Altera SERDES Simulation Results for the 1m BP (PAM-2 Signaling)




| Channel Length (meter) | Eye Height (1E-12) | Eye Width (1E-12) | Eye Height (1E-15) | Eye Width (1E-15) | Satisfies 1 m and 1E-12 BER objective |
|---|---|---|---|---|---|
| 1.0 | 42.3 mV | 0.469 UI | 38.06 mV | 0.444 UI | Yes |

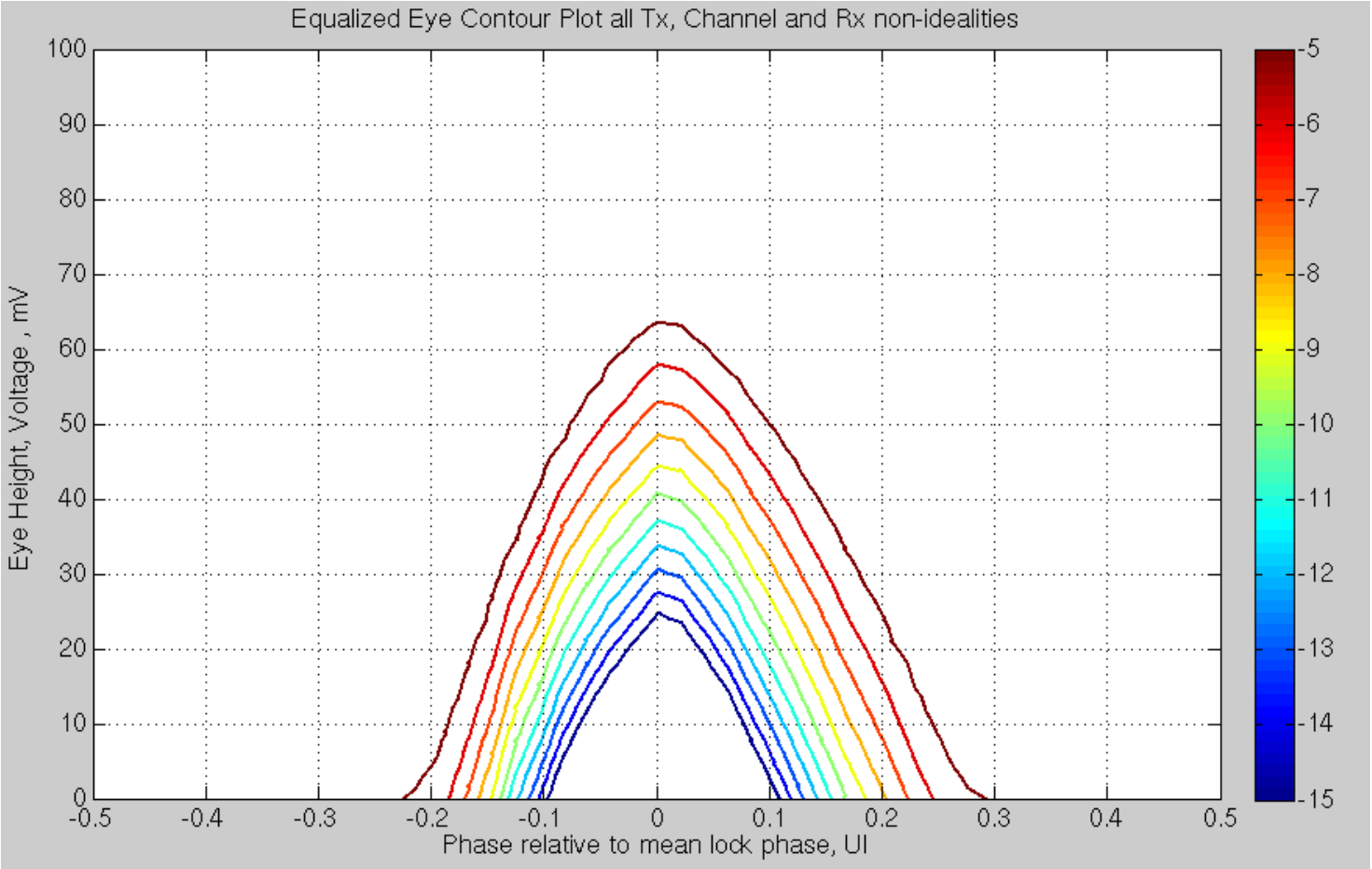
# LSI simulation results (NRZ)




| Channel Length (meter) | Eye Height (1E-12) | Eye Width (1E-12) | Eye Height (1E-15) | Eye Width (1E-15) | Satisfies 1 m and 1E-12 BER objective |
|---|---|---|---|---|---|
| **1.0** | **31 mV** | **23.3%** | **23 mV** | **19%** | **Yes** |

Simulation conditions: Reference 3

# TI SERDES Simulation Results for the 1m BP (PAM-2 Signaling)




| Channel Length (meter) | EYE (1E-12) | Horizontal EYE (1E-12) | Vertical EYE (1E-15) | Horizontal EYE (1E-15) | Channel Loss @12.5Ghz dB | Satisfies 1 m and 1E-12 BER objective |
|---|---|---|---|---|---|---|
| 1.0 | 33.2mV | 27% | 24.1mV | 21% | -28dB | Yes |

# PAM-2 Signaling Standards from 25-28Gbps

- OIF CEI-25G-LR, CEI-28G-SR, CEI-28G-VSR
- 32GFC Fibre Channel
- FDR and EDR InfiniBand

- Previous PAM-2 Signaling
  - KX, KX4, KR, KR4 Ethernet
  - OIF CEI-6G and CEI-11G
  - 1GFC to 16GFC Fibre Channel
  - SDR to QDR InfiniBand
  - Many more…

# PAM-2 Signaling Benefits

- Backward compatibility with most ASIC/FPGA implementations
- One ASIC/FPGA for backplane and module ports
  - Common port for copper and optical
- Same SERDES design can support multiple standards
  - CEI-25-LR
  - InfiniBand EDR
  - 32G Fibre Channel
- Experienced debugging environment
- FEC is not required for this channel to meet the 1E-12 BER objective

# Conclusion and Summary

- Multiple SERDES vendors have demonstrated PAM-2 technical feasibility via simulations of 1 m reach channel with 1e-12 BER and 4 lanes per 802.3 bj objectives
- The loss of this 1m channel is equivalent to the loss of a channel with 29 inch of “improved FR-4” (see Georgen_01_0511.pdf)
- These simulations were done without FEC that could add significant coding gain that can be used on a higher loss channel
- Adopting  PAM-2 signaling enables IEEE 802.3bj to be compatible with other 25-28 G standards, permitting “single SERDES does all”, backward compatibility, and large market potential

# Reference Material


1. Troy Beukema, “Line signaling performance comparison on extended loss backplanes”,July 2011, Ethernet Alliance

   --- http://www.ethernetalliance.org/events/technology_exploration_forums/tef_presentations.
2. Mike Li, “A Study of 25 Gbps Signaling Over Complied 10G-KR Channels”, May 2011, IEEE 802.3 100Gb/s Ethernet Electrical Backplane and Twinaxial Copper Cable Assemblies Study Group Interim Meeting

   ---- http://ieee802.org/3/100GCU/public/may11/index.html
3. Adam Healey, “Simulation parameters and results template with example,” healey_01_1109.xlsx.
4. Analog-DFE-based 16Gb/s SerDes in 40nm CMOS that operates across 34dB loss channels at Nyquist with a baud rate CDR and 1.2Vpp voltage-mode driver

   Joy, A.K. Mair, H. Hae-Chang Lee Feldman, A. Portmann, C. Bulman, N. Crespo, E.C. Hearne, P. Huang, P. Kerr, B. Khandelwal, P. Kuhlmann, F. Lytollis, S. Machado, J. Morrison, C. Morrison, S. Rabii, S. Rajapaksha, D. Ravinuthula, V. Surace, G.

   Page(s): 350 - 351 settings used:


Tx and Rx equalization capabilities
Tx: FIR 3-taps, 1 pre-, one post cursor
Rx: CTLE (15 dB max) + DFE (15-tap DFE)
Signal modulation: PAM-2
TI's Matlab simulation environment
Data pattern: prbs2^31-1, 6x2^20 bit
Vod: 1.2mVpp