100G-Cu FEC and PCS Encoding Thoughts

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Assumptions

- Serial Line rate when FEC is on and off are the same
- Latency hit when FEC is on needs to be “minimized”
  - FEC Frame size is major latency component
- Reed-Solomon ECC technique
- Target is 11b burst error protection

FEC encoding

- RS with m=10 (bits per RS block) means 2 blocks cover 11b
- Need twice the number of parity RS blocks compared to correctable RS block count
- 11b error protection means 4 RS parity blocks
  - 2*(2 correctable blocks)*(10b per RS block) = 40b of parity
- 64/66 provides 1b per PCS block for parity blocks
  - 40*66 = 2640b FEC frame size
  - Clause 74 FEC frame is 2112b

An approach to reduce FEC frame size

- Increase the base overhead of the PCS block
  - 160/168 provides up to 7b of parity per PCS block
  - 7b * 6 PCS blocks = 42b which is >= 40b
  - 6 PCS Blocks * 168b = 1008b FEC frame

- 1008 / 2640 = ~62% reduction
- 1008 / 2112 = ~53% reduction

- NOTE: 1008 frame size is requirement **per lane** to provide minimum 11b protection. In other words, you can't stripe this.

Line rate and FEC block transmission size

- 64/66 encoding
  - 10.3125*(10/4) => 25.78125 GHz
  - 2112 * 96.97ps ~ 204 ns (10G Clause 74)
  - 2640 * 38.8ps ~ 102 ns (RS at 25G)

- 160/168 encoding
  - 156.25*168 => 26.25 GHz
  - Increase of 1.8% in rate over 64/66
  - 1008 * 38.1ps ~ 38.4 ns

Other potential affects of more overhead

- Benefits
  - Encode lane ID in overhead
  - Embed deskew characters in overhead
- Detriments
  - Not same as 40G

Alternate block encoding

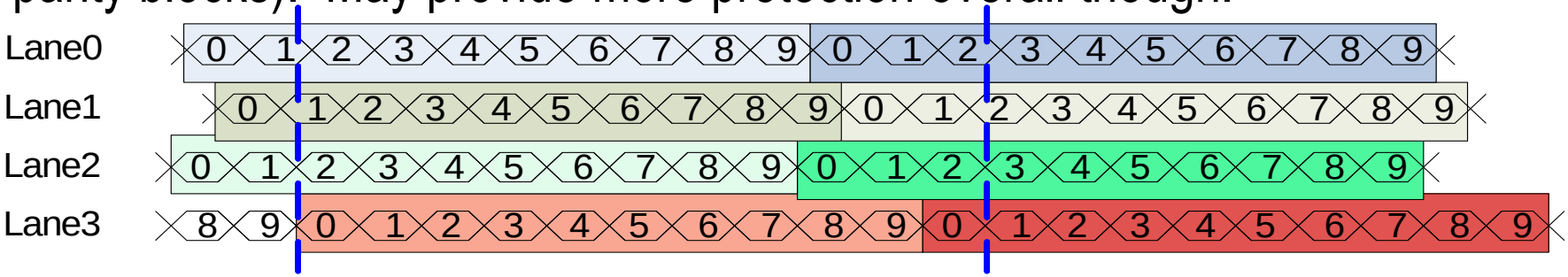
- 80/84
  - 3b of overhead per PCS block
    - 14 * 3b > 40b => 14*84b = 1176b FEC frames
  - 26.25GHz line rate (same as 160/168)
  - ½ block size reduces gear box area increase
  - Insertion of Lane Marker may not be possible
  - "Just" 2 extra characters per block over 64/66
    - This could be a "minor" extension of current encoder

Final Remarks

- FEC latency is greatly affected by FEC frame size
  - Have to receive entire frame before you can begin processing
  - To error mark the frame, latency >= 2x FEC frame size
- Number of overhead bits in the PCS block affects how large the FEC frame size
- Increasing the base overhead of PCS block helps to reduce FEC frame size

Backup – Why 1008 is per lane

- Corruption of data will occur on series of bits coming out of a given lane.
- Assuming worst case length is 11b
- All 4 lanes could be affected simultaneously or at different times with in same FEC frame
- Need to protect 8 RS blocks, which is 4x increase over single lane
- No parity savings with striping since you need larger frames (16 RS parity blocks). May provide more protection overall though.



Backup – Why 1008 is per lane cont.

- Striping RS blocks across lanes
  - 11b string on each lane affects 3 RS blocks per lane
  - So 3 RS blocks per event * 4 events = 12 RS blocks corrupted
  - 12 * 2 = 24 parity RS blocks