Response to Comment #80 and Proposal for an alternate 45/46 code for KP4

Will Bliss, Broadcom Corp.
Dariush Dabiri, AMCC

Sept. 17, 2012

for IEEE 802.3bj 100GBASE-KP4 task force
Geneva

Outline

- Comment #80
- Motivation for proposal to modify 45/46 Partial State Pinning
- Details of this proposal
- Open items for resolution

Comment #80 from Charles Moore

Cl **94** *SC* **94.2.2.4** *P* **147** *L* **40** # 80

Moore, Charles — Avago Technologies

Comment Type **T** *Comment Status* **D**

Termination bits complicate the coding and add 2.2% overhead. It is not clear that we receive real benefit in return. If a ML receiver is used it will allow us to correct a single bit error in a 45 bit block. Such errors are not likely to be what gets past FEC. Most likely multibit errors, which the termination block is less likely to correct, will be what cause FEC failures. Also if the receiver does not use ML, there is no value to the termination bits.

SuggestedRemedy

Remove termination bits and either use the reduced overhead to strengthen FEC or reduce line rate.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

The termination bits have been included in this draft as a result of the consensus presentations brown_01_0312 and brown_01_0512. The benefits of the termination bits have been shown to outweigh the benefit of increasing the FEC stength or reducing the line rate in dabiri_01_0911, parthasarthy_01_0911, and dabiri_01_1111. The utility of termination bits is not limited to MLSD as explained in brown_01_0312 and dabiri_01b_0112. The termination bits enable a wide range of efficient implementations of enhanced performance receivers.

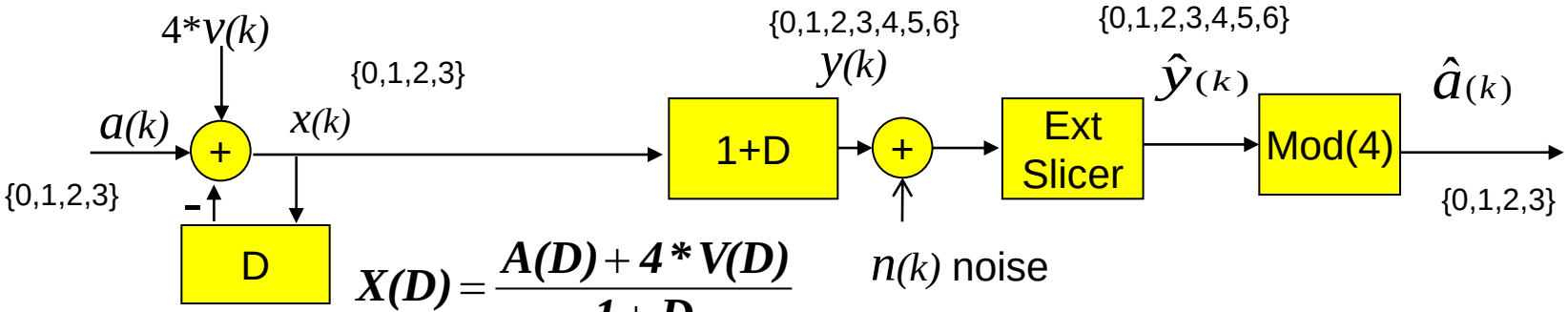
Overview of draft 1.0 KP4 Partial State Pinning Scheme

- Draft 1.0 KP4 format includes a 45/46 rate PSP Scheme.
- PSP is partially intended to allow:
  - A lower cost implementation of MLSD by supporting parallel processing of non-overlapping blocks
  - Error detection with DFE implementation.
  - No support for the PR Extended Constellation Slicer
  - Reference [dabiri_01a_0112]
- Every 23rd PAM-4 symbol is limited to state {0 or 3}, so only 1 user data bit is sent with these symbols
- 22 symbols of each of block of 23 are precoded with a 1/(1+D) mod(4) precoder
- Every 23rd symbol is a ‘boundary’ that is transmitted without precoding
- Each of these boundary symbols is used to force the state of the precoder, which is used for the precoding of the next block

Motivations to Modify draft 1.0 KP4 Format

- A PSP scheme can be applied to detect errors with Partial Response (PR) Extended Slicer Detectors.
- A simple 45/46 code can detect single bit errors.
  - Can we make such a code still support block parallel VA implementation?
- The current PSP scheme disallows implementation of the simple and low latency detector, the PR Extended Slicer.
  - The extended slicer requires all symbols must be precoded, which current PSP violates
- We'd like a 45/46 PSP scheme that 'partially pins' the channel states, that precodes all the symbols, and that can be used for error detection and/or correction with all detectors

Review of PR Extended Slicer, see ref. [Bliss_01_0311]



$$X(D) = \frac{A(D) + 4 * V(D)}{1 + D}$$

$Y(D) = A(D) + 4*V(D)$

$y(k) = a(k) + 4* v(k)$

$4* v(k)$ is the hypothetical input on {0 or 4}

$a(k) = \{ y(k) \}$ Mod-4

- The input to the slicer is 'expanded', which is identical to that of a DFE with 1-tap FBF of value *1* and identical to that of the VA
- This detector performs asymptotically (high SNR) the same as the DFE above, but with zero error propagation
  - The same *d_min=1*, but the extended slicer has fewer cases of 'harmless noise' pushing beyond the extreme max or min signal
  - The Error Event Rate of the Extended slicer is 5/4 * the EER of this DFE
- Implementation is near zero cost, zero latency, and unlimited parallelism
  - E.g., round to integer and discard MSB, etc.
- The 'detector' and the 'precoder decoder' are now intermingled, so all symbols must be precoded

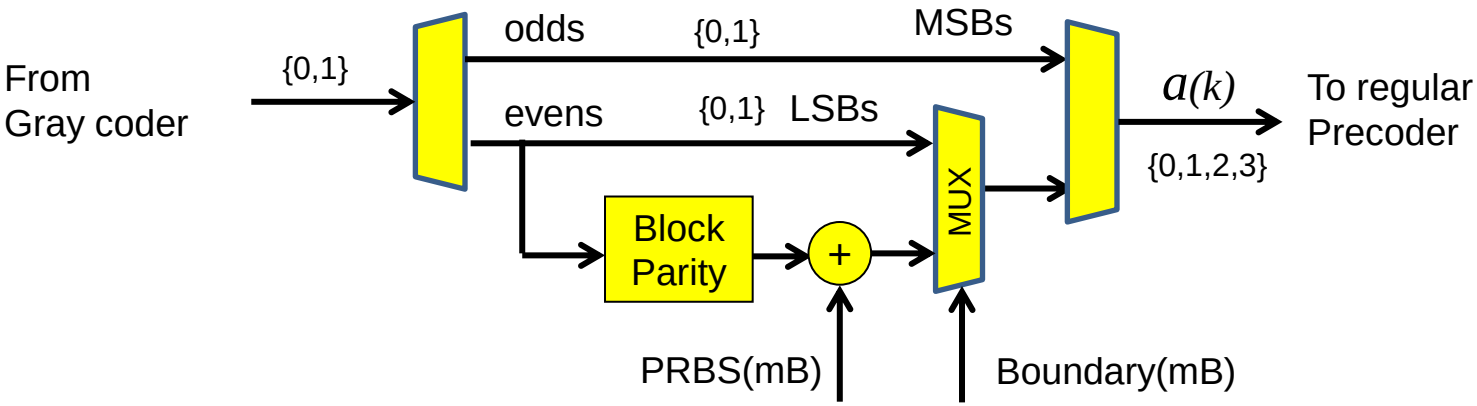
Proposal for Modified KP4 Format

- Based on a variant of PSP denoted ‘constant power termination symbol’ where the channel *x(k)* state pinning was either on the set {0,2} or on the set {1,3}, and where the choice of set was driven by a PRBS
  - The choice within a set is the 1-bit of ‘user information’
  - The PRBS choice of set sufficiently ‘randomizes’ the selection to keep the power spectrum both white and time-invariant
  - Presented in reference [Dabiri_01a_0112] backup slides
- Proposal suggested by Dabiri is minor addition to ‘constant power termination’
  - The ‘MSB’ of the boundary symbol is the ‘one user bit’ on {0,2} (same as above)
  - Let the ‘LSB’ of the boundary symbol be PRBS (same as above) XORed with a parity over the 22 user symbols

$$LSB\{a(mB)\} \quad = \; PRBS(mB) + \sum_{k=1}^{22} a(mB-k) \quad all\ Modulo(2)$$

    - The PRBS can be thought of as randomizing between even and odd block parity
    - Because a(k) is PAM-4 on {0,1,2,3}, this sum ignores the MSBs, and is a parity on the LSBs
  - All symbols, including the boundary symbols, are input to the precoder, which is never ‘forced’ or ‘set’

Block Diagram of Modified 45/46 code



- The LSB of the boundary symbol is the XOR (modulo 2 sum) of the PRBS randomizer bit and block parity on the even bits in the input stream

Proof the Modified KP4 Format supports PSP

$$\sum_{k=1}^{23} a(mB-k)\ \ Mod(2) = PRBS(mB)\ by\ construction$$

- The 45/46 encoder *Mod(2*) sum above is a special subset of the *Mod(4)* alternating sum of the precoder

$$\sum_{k=1}^{23} a(mB-k)\ (-1)^k\ \ Mod(4) = \{0\ or\ 2\}\ only$$

  - If the starting state was on *{0,2},* then the ending state is on *{0,2}* + *PRBS(mB)*
  - If the starting state was on *{1,3},* then the ending state is on *{1,3}* – *PRBS(mB*)
  - Because *PRBS(mB)* is known a priori, all the Boundary state sets are known a priori (can be computed ahead of time)

Summary of Modified 45/46 code Results

- Partial State Pinning (PSP) of the channel state is achieved, which still supports block parallel VA and DFE implementations
- All symbols are precoded, which additionally supports the simple PR Extended Slicer
- All symbols are protected by the 45/46 parity code
  - Parity of every symbol's LSB is covered
  - Which covers all likely single error events, which are all +/-1/3 (one level) error patterns
  - All detectors are enabled to use this code for detection and/or post processor correction as desired
- The TX power spectrum is both time-invariant and white

To Do Work for Modified 45/46 code

- The PRBS used to randomize the parity of each block needs to be defined, and some RXs need to be synchronized
  - If block parallel VA or DFE is implemented, or if Error Detection or Correction from the parity code is implemented, then RX synchronization is needed
  - The KP4 draft Training (lusted_01_0912) appears able to support this synchronization with a minor addition
- The TX precoder initial state needs to be defined, and some receivers need to be synchronized
  - Again, If block parallel VA or DFE, or if Error Detection or Correction from the parity code is implemented, then RX synchronization is needed
  - The KP4 draft Training (lusted_01_0912) appears able to support precoder synchronization as defined (needs to be verified)
- The draft Training PRBS seeds were chosen based on the Draft 1.1 PSP
  - Likely need a new choice of seeds