30.5.1.1.16 aFECmode

ATTRIBUTE

APPROPRIATE SYNTAX:

A ENUMERATION that meets the requirement of the description below

unknown	initializing, true state not yet known
disabled	FEC disabled
enabled	FEC enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the optional FEC sublayer for forward error correction (see 65.2 and Clause 74).

A GET operation returns the current mode of operation of the PHY. A SET operation changes the mode of operation of the PHY to the indicated value. When Clause 73 Auto-Negotiation is enabled a SET operation is not allowed and a GET operation maps to the variable FEC enabled in Clause 74.

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the FEC control register (see 45.2.7.3) for 1000BASE-PX or FEC enable bit in BASE-R FEC control register (see 45.2.1.88).;

30.5.1.1.17 aFECCorrectedBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresetable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s and 40 Gb/s implementations, and 2 500 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 1000BASE-PX PHYs or 10/40/100GBASE-R PHYs, an array of corrected FEC block~~s~~ counters. The counters will not increment for other PHY types. The indices of this array (0 to N – 1) denote the PCS lane number where N is the number of PCS lanes in use. The number of PCS lanes in use is set to one for PHYs that do not use PCS lanes. Each element of this array contains a count of corrected FEC blocks for that PCS lane.

Increment the counter by one for each received block that is corrected by the FEC function in the PHY for the corresponding lane.

If a Clause 45 MDIO Interface to the PCS is present, then this attribute maps to the FEC corrected blocks counter(s) (see 45.2.8.5, 45.2.1.87, and 45.2.1.89).;

30.5.1.1.18 aFECUncorrectableBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresetable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, and 5 000 000 counts per second for 10 Gb/s and 40 Gb/s implementations, and 2 500 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 1000BASE-PX PHYs or 10/40/100GBASE-R PHYs, an array of uncorrectable FEC block~~s~~ counters. The counters will not increment for other PHY types. The indices of this array (0 to N – 1) denote the PCS lane number where N is the number of PCS lanes in use. The number of PCS lanes in use is set to one for PHYs that do not use PCS lanes. Each element of this array contains a count of uncorrectable FEC blocks for that PCS lane.

Increment the counter by one for each FEC block that is determined to be uncorrectable by the FEC function in the PHY for the corresponding lane.

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the FEC uncorrectable blocks counter(s) (see 45.2.8.6, 45.2.1.88, and 45.2.1.90).;

30.5.1.1.19 aSNROpMarginChnlA

ATTRIBUTE
APPROPRIATE SYNTAX:
INTEGER
BEHAVIOUR DEFINED AS:
The current SNR operating margin measured at the slicer input for channel A for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel A register (see 45.2.1.63).;

30.5.1.1.20 aSNROpMarginChnlB

ATTRIBUTE
APPROPRIATE SYNTAX:
INTEGER
BEHAVIOUR DEFINED AS:
The current SNR operating margin measured at the slicer input for channel B for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel B register (see 45.2.1.64).;

30.5.1.1.21 aSNROpMarginChnlC

ATTRIBUTE
APPROPRIATE SYNTAX:
INTEGER
BEHAVIOUR DEFINED AS:
The current SNR operating margin measured at the slicer input for channel C for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel C register (see 45.2.1.65).;

30.5.1.1.22 aSNROpMarginChnlD

ATTRIBUTE
APPROPRIATE SYNTAX:
INTEGER
BEHAVIOUR DEFINED AS:
The current SNR operating margin measured at the slicer input for channel D for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to

30.5.1.1.15 aFECCorrectedBlocks

Change the behaviour definition to read as follows:

For 1000BASE–PX~~ PHYs or,~~ 10GBASE–R, 10GBASE–PR or 10/1GBASE–PRX PHYs, a count of corrected FEC codewords. This counter ~~will~~does not increment for other PHY types.

Increment the counter by one for each received block that is corrected by the FEC function in the PHY.

If a Clause 45 MDIO Interface to the PCS is present, then this attribute ~~will~~ maps to the FEC corrected codewords counter (see 45.2.7.5 and 45.2.1.86 for 10GBASE–R, 45.2.3.32 for 10GBASE–PR and 10/1GBASE–PRX).;

30.5.1.1.16 aFECUncorrectableBlocks

Change the behaviour definition to read as follows:

For 1000BASE–PX~~ PHYs or,~~ 10GBASE–R, 10GBASE–PR or 10/1GBASE–PRX PHYs, a count of uncorrectable FEC codewords. This counter ~~will~~does not increment for other PHY types.

Increment the counter by one for each received block that is determined to be uncorrectable by the FEC function in the PHY.

If a Clause 45 MDIO Interface to the PCS is present, then this attribute ~~will~~ maps to the FEC uncorrectable codewords counter (see 45.2.7.5 and 45.2.1.87 for 10GBASE–R, 45.2.3.33 for 10GBASE–PR and 10/1GBASE–PRX).;

30.5.1.1.10b aLaneMapping

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of INTEGERs.

BEHAVIOUR DEFINED AS:
For 40/100GBASE-R PHYs, an array of PCS lane identifiers. The indices of this array (0 to n – 1) denote the service interface lane number where n is the number of PCS lanes in use. Each element of this array contains the PCS lane number for the PCS lane that has been detected in the corresponding service interface lane.
If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the Lane mapping registers (see 45.2.3.38 and 45.2.3.39).;

Change 30.5.1.1.14, 30.5.1.1.15, and 30.5.1.1.16 for FEC as follows:

30.5.1.1.14 aFECmode

ATTRIBUTE

APPROPRIATE SYNTAX:
A ENUMERATION that meets the requirement of the description below

unknown	initializing, true state not yet known
disabled	FEC disabled
enabled	FEC enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the optional FEC sublayer for forward error correction (see 65.2 and Clause 74).

A GET operation returns the current mode of operation of the PHY. A SET operation changes the mode of operation of the PHY to the indicated value. When Clause 73 Auto-Negotiation is enabled a SET operation is not allowed and a GET operation maps to the variable FEC enabled in Clause 74.

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the FEC control register (see 45.2.7.3) for 1000BASE-PX or FEC enable bit in ~~10G~~BASE-R FEC control register (see 45.2.1.86).;

30.5.1.1.15 aFECCorrectedBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of generalized ~~Generalized~~ nonresetable counters. ~~This~~Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, ~~and~~ 5 000 000 counts per second for 10 Gb/s and 40 Gb/s implementations, and 2 500 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:
For 1000BASE-PX PHYs or 10/40/100GBASE-R PHYs, ~~a count~~ an array of corrected FEC block~~s~~ counters. The counters will not increment for other PHY types. The indices of this array (0 to N – 1) denote the PCS lane number where N is the number of PCS lanes in use. The number of PCS lanes in use is set to one for PHYs that do not use PCS lanes. Each element of this array contains a count of corrected FEC blocks for that PCS lane.

Increment the counter by one for each received block that is corrected by the FEC function in the PHY for the corresponding lane.

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the FEC corrected blocks counter(s) (see 45.2.8.5, ~~and~~ 45.2.1.87, and 45.2.1.89).;

30.5.1.1.16 aFECUncorrectableBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized ~~Generalized~~ nonresetable counters. ~~This~~Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, and 5 000 000 counts per second for 10 Gb/s and 40 Gb/s implementations, and 2 500 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 1000BASE-PX PHYs or 10/40/100GBASE-R PHYs, ~~a count~~ an array of uncorrectable FEC block~~s~~ counters. The counters will not increment for other PHY types. The indices of this array (0 to N – 1) denote the PCS lane number where N is the number of PCS lanes in use. The number of PCS lanes in use is set to one for PHYs that do not use PCS lanes. Each element of this array contains a count of uncorrectable FEC blocks for that PCS lane.

Increment the counter by one for each FEC block that is determined to be uncorrectable by the FEC function in the PHY for the corresponding lane.

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the FEC uncorrectable blocks counter(s) (see 45.2.8.6, ~~and~~ 45.2.1.88, and 45.2.1.90).;

Change 30.6.1.1.5 for autoneg ability and FEC request as follows:

30.6.1.1.5 aAutoNegLocalTechnologyAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE that meets the requirements of the description below:

global	Reserved for future use
other	See 30.2.5
unknown	Initializing, true state or type not yet known
10BASE-T	10BASE-T half duplex as defined in Clause 14
10BASE-TFD	Full duplex 10BASE-T as defined in Clause 14 and Clause 31
100BASE-T4	100BASE-T4 half duplex as defined in Clause 23
100BASE-TX	100BASE-TX half duplex as defined in Clause 25
100BASE-TXFD	Full duplex 100BASE-TX as defined in Clause 25 and Clause 31
FDX PAUSE	PAUSE operation for full duplex links as defined in Annex 31B
FDX APAUSE	Asymmetric PAUSE operation for full duplex links as defined in Clause 37, Annex 28B, and Annex 31B
FDX SPAUSE	Symmetric PAUSE operation for full duplex links as defined in Clause 37, Annex 28B, and Annex 31B
FDX BPAUSE	Asymmetric and Symmetric PAUSE operation for full duplex links as defined in Clause 37, Annex 28B, and Annex 31B
100BASE-T2	100BASE-T2 half duplex as defined in Clause 32

unknowninitializing, true state not yet known
disabled FEC disabled
enabled FEC enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the optional FEC sublayer for forward error correction (see 65.2 and Clause 74).

A GET operation returns the current mode of operation of the PHY. A SET operation changes the mode of operation of the PHY to the indicated value. When Clause 73 Auto-Negotiation is enabled a SET operation is not allowed and a GET operation maps to the variable FEC enabled in Clause 74.

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the FEC control register (see 45.2.8.3) for 1000BASE-PX or FEC enable bit in BASE-R FEC control register (see 45.2.1.90).;

30.5.1.1.17 aFECCorrectedBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s and 40 Gb/s implementations, and 2 500 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/40/100GBASE-R PHYs, an array of corrected FEC block counters. The counters will not increment for other PHY types. The indices of this array (0 to N – 1) denote the PCS lane number where N is the number of PCS lanes in use. The number of PCS lanes in use is set to one for PHYs that do not use PCS lanes. Each element of this array contains a count of corrected FEC blocks for that PCS lane.

Increment the counter by one for each received block that is corrected by the FEC function in the PHY for the corresponding lane.

If a Clause 45 MDIO Interface to the PCS is present, then this attribute maps to the FEC corrected blocks counter(s) (see 45.2.8.5, 45.2.1.91, and 45.2.1.93).;

30.5.1.1.18 aFECUncorrectableBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, and 5 000 000 counts per second for 10 Gb/s and 40 Gb/s implementations, and 2 500 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 1000BASE-PX PHYs or 10/40/100GBASE-R PHYs, an array of uncorrectable FEC block counters. The counters will not increment for

other PHY types. The indices of this array (0 to N – 1) denote the PCS lane number where N is the number of PCS lanes in use. The number of PCS lanes in use is set to one for PHYs that do not use PCS lanes. Each element of this array contains a count of uncorrectable FEC blocks for that PCS lane.

Increment the counter by one for each FEC block that is determined to be uncorrectable by the FEC function in the PHY for the corresponding lane.

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the FEC uncorrectable blocks counter(s) (see 45.2.8.6, 45.2.1.92, and 45.2.1.94).;

30.5.1.1.19 aSNROpMarginChnlA

ATTRIBUTE
APPROPRIATE SYNTAX:
INTEGER
BEHAVIOUR DEFINED AS:
The current SNR operating margin measured at the slicer input for channel A for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel A register (see 45.2.1.65).;

30.5.1.1.20 aSNROpMarginChnlB

ATTRIBUTE
APPROPRIATE SYNTAX:
INTEGER
BEHAVIOUR DEFINED AS:
The current SNR operating margin measured at the slicer input for channel B for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel B register (see 45.2.1.66).;

30.5.1.1.21 aSNROpMarginChnlC

ATTRIBUTE
APPROPRIATE SYNTAX:
INTEGER
BEHAVIOUR DEFINED AS:
The current SNR operating margin measured at the slicer input for channel C for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel C register (see 45.2.1.67).;

30.5.1.1.22 aSNROpMarginChnlD

ATTRIBUTE
APPROPRIATE SYNTAX:
INTEGER
BEHAVIOUR DEFINED AS:
The current SNR operating margin measured at the slicer input for channel D for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to