What We Learned from XAUI and How to Apply it to Ethernet in the Backplane

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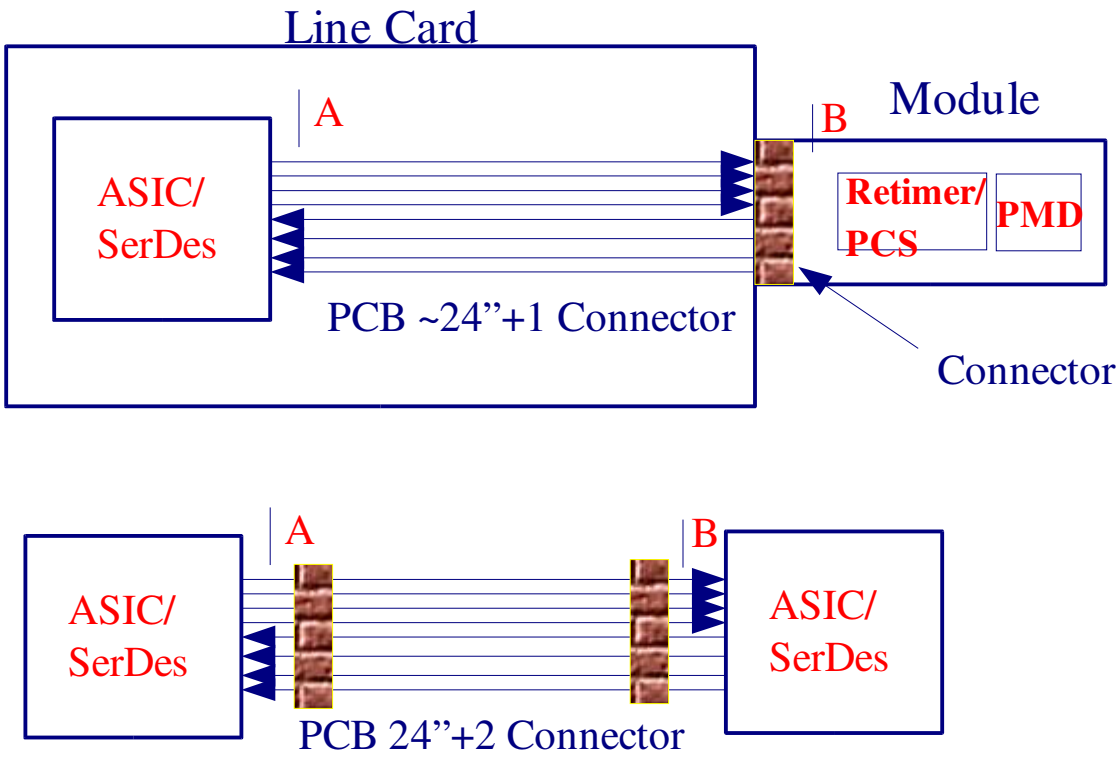
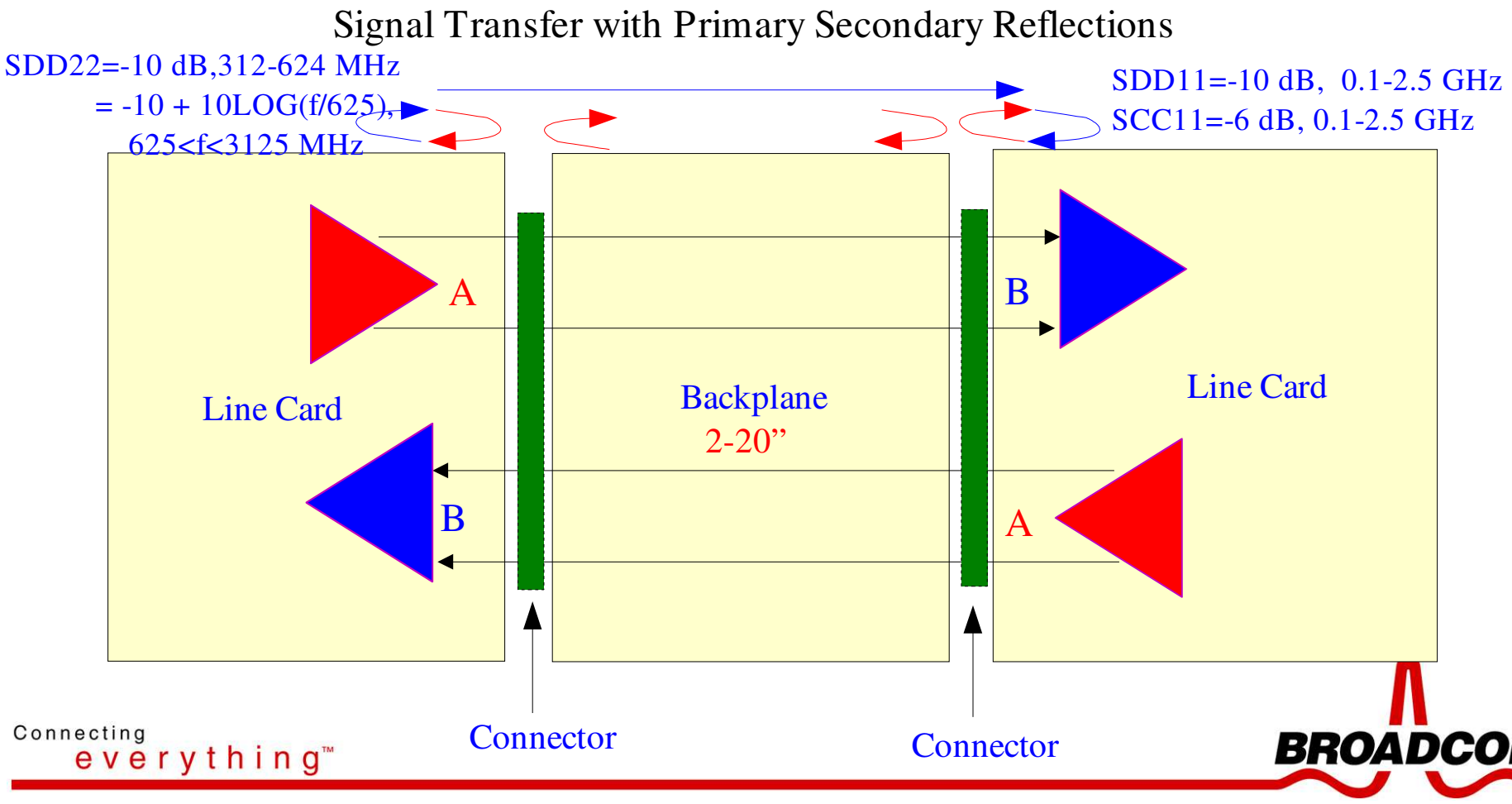
Original XAUI Application Diagram

- **Focus was on chip specifications coupled to an ideal lossy transmission line.**



A Typical Backplane Showing Primary and Secondary Reflections

- **XAUI only defines reflections shown in blue for the IC's.**



Impact of Channel Return Loss on a XAUI Link

- **The primary effect of return loss is the amount of signal gets transfered to the receiver.**
- **A multiple reflection caused by the finite return loss of driver RL in conjunction with channel introduces additional amplitude distortion as well as jitter.**
- **Compliance Channel incorporates effect of channel return loss indirectly even though it was not specified.**
  - ⇨ **But it does not take into account multiple reflection caused between the receiver looking back in to channel.**
  - ⇨ **A single channel reflection of -10dB reduces transmit budget by 3.2 dB or 26% of XAUI total loss budget !**

Impact of Secondary Reflection

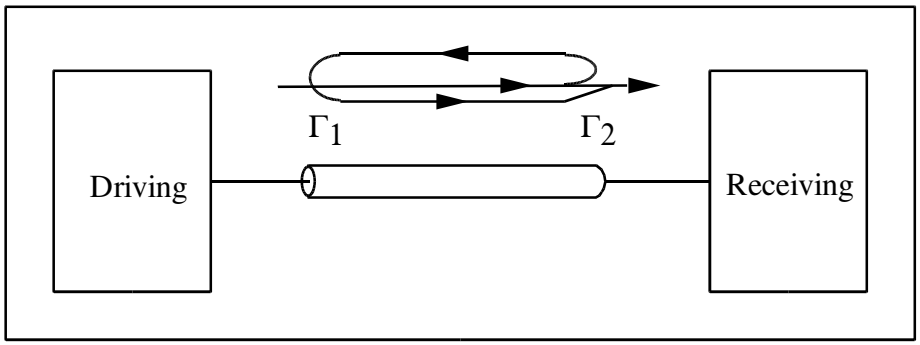


Fig 1
Multiple reflection between driver output & receiver input

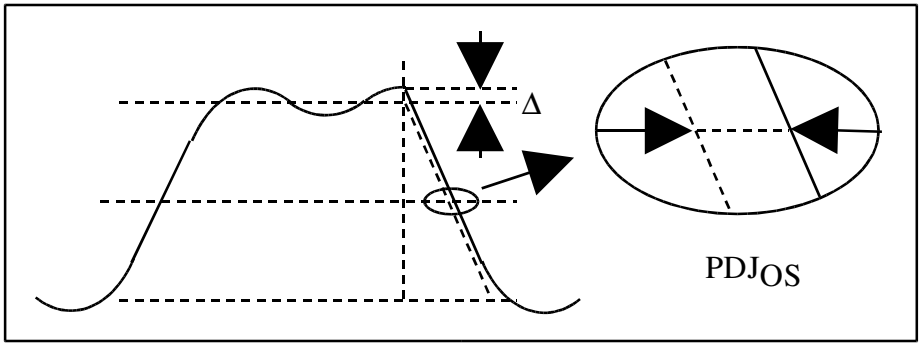


Fig 2
Worst case voltage at receiver input for DJ calculation

Assume

Driving device: S22 $=\Gamma_1$

Receiving device: S11 $=\Gamma_2$

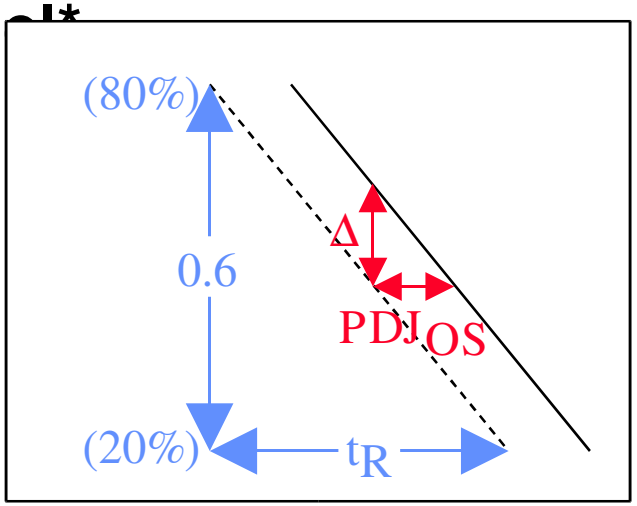
So, the maximum voltage overshoot/undershoot at receiving input (ignore transmission line loss):

$$\delta = |\Gamma_1|*|\Gamma_2| + |\Gamma_1|*|\Gamma_2|*|\Gamma_1|*|\Gamma_2| + |\Gamma_1|*|\Gamma_2|*|\Gamma_1|*|\Gamma_2|*|\Gamma_1|*|\Gamma_2| + \ldots..$$

Calculation provided by Quentan Tan of Maxim

Link Jitter and Amplitude Penalty Estimation

- **Multiple reflection penalty between receiver and channel***



Refer to Fig 2 and this drawing:

$$\frac{|PDJ_{OS}|}{\delta} = \frac{t_R}{0.6}$$

$$PDJ_{OS} = \pm\frac{\delta}{0.6}\cdot t_R$$

t_R : 20%-80% Edge speed

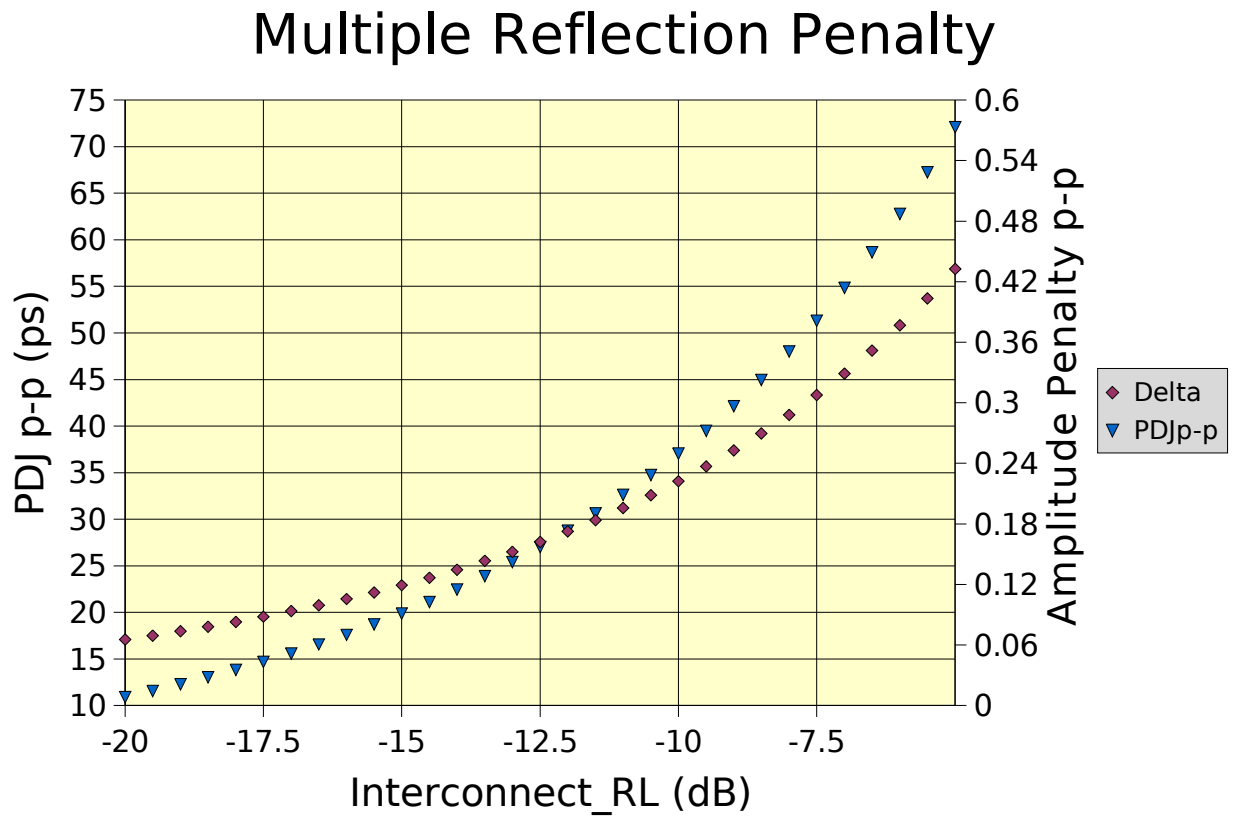
⇨The RL at the B is estimated to be -10 dB

⇨Assume channel RL is -10 dB at 1.57 GHz, then $\Gamma 1 x \Gamma 2$= 0.31x0.31=0.1 with Tr=125 ps, gives Δ=0.11 and PDJ= +/-23 ps = +/-0.072 UI.

* Assuming source reflection are taken in to account as part of compliance channel test.

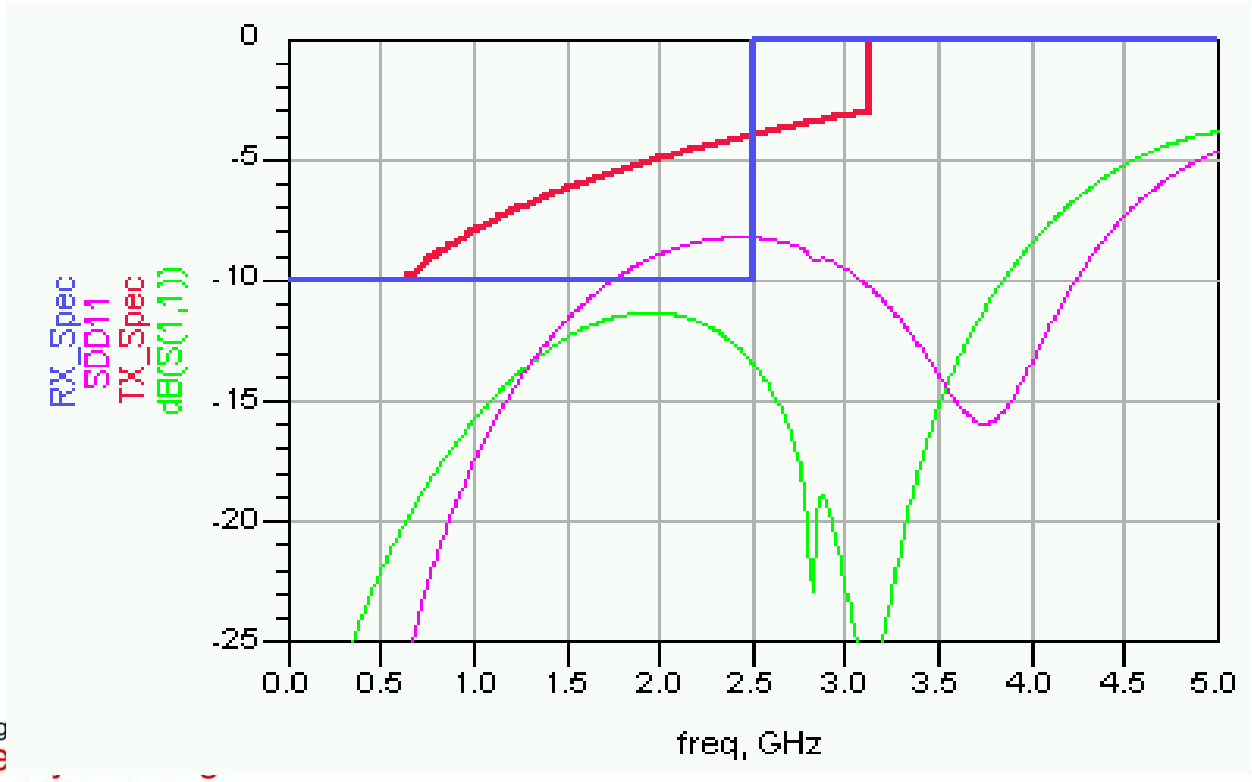
Link Penalty Due to Multiple Reflections

- **By defining backplane/channel RL max penalty is bounded**
  - ⇨Assumes chip RL to be -10 dB at 1.51 GHz .



XAUI RL Compare to Typical BGA Package with ESD Diode

- **BGA Package, parasitics, with 0.75 pf ESD diode.**
  - ⇨XAUI transmitter mask specification resembles a typical receiver input with ESD.
  - ⇨XAUI RX mask has extra burden at high frequency



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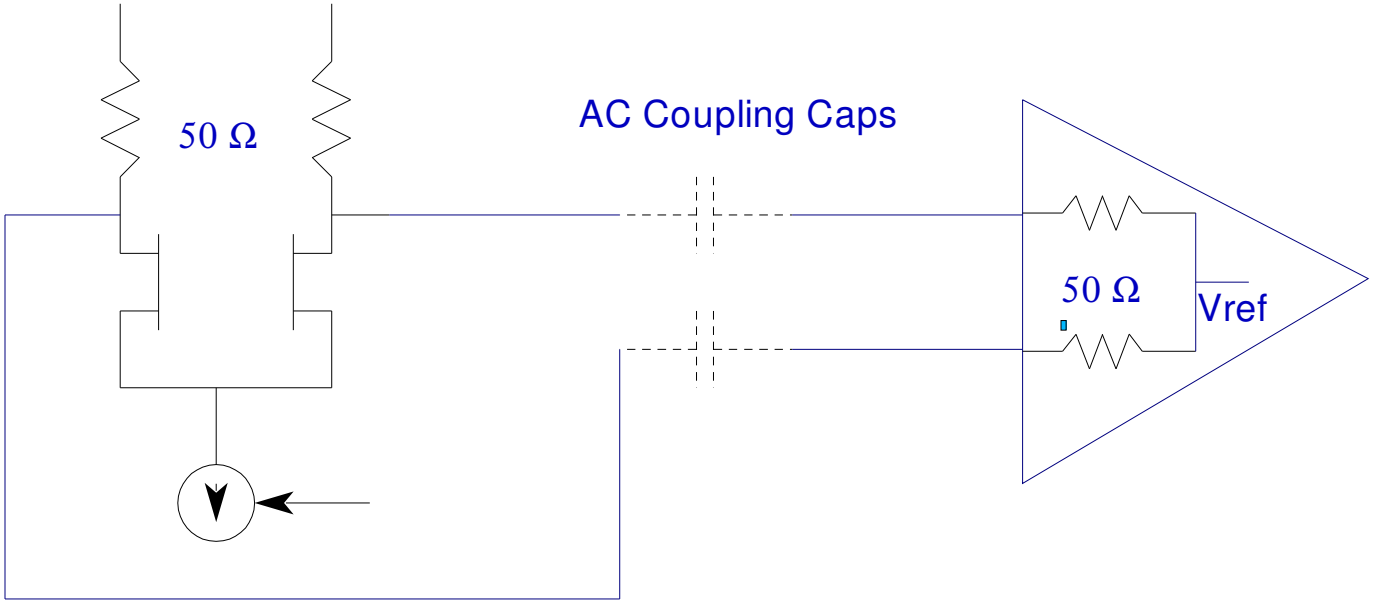
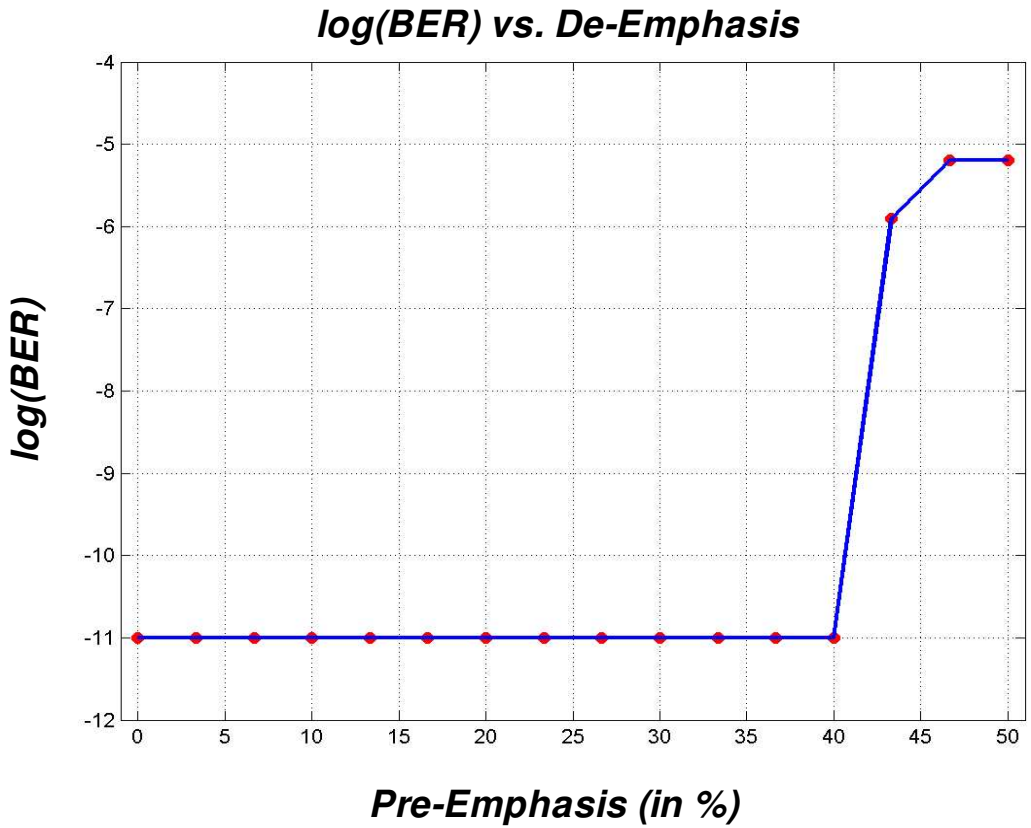
CML Driver Structure

- **XAUI defines common mode RL for receiver but not for the driver.**
  - ⇨CML driver provide CM RL for free but CM RL at the receiver has performance and cost penalty.
    - XAUI only specifies receiver CM!



Pre-Emphasis

- **In XAUI it was assumed excess pre-emphasis is ok.**

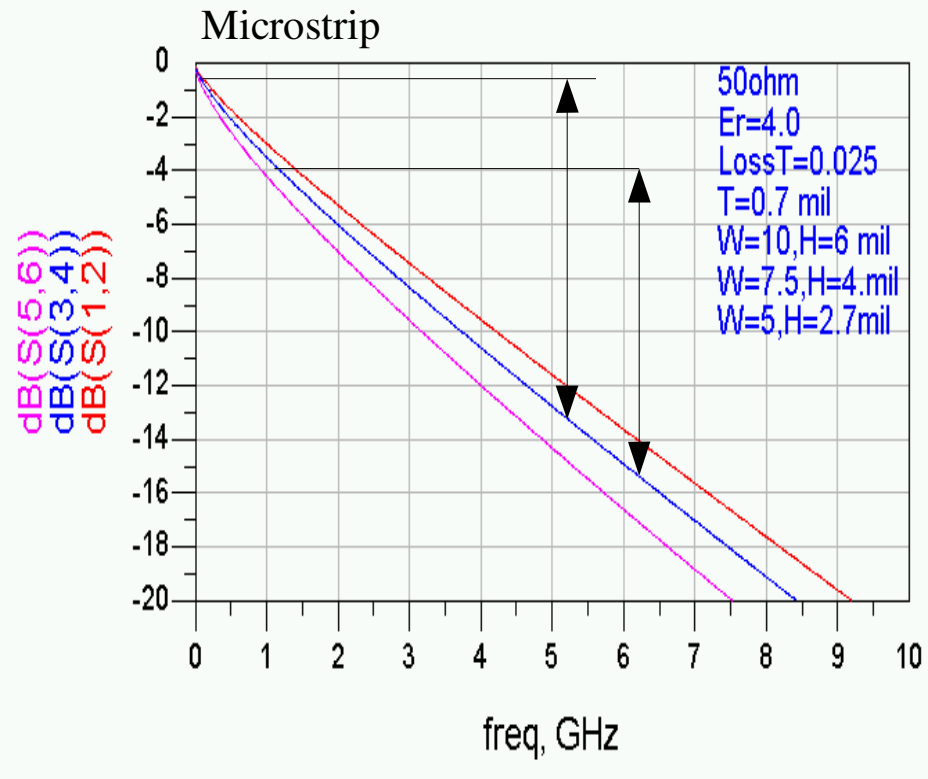


Ethernet in the Backplane Architectural Requirement

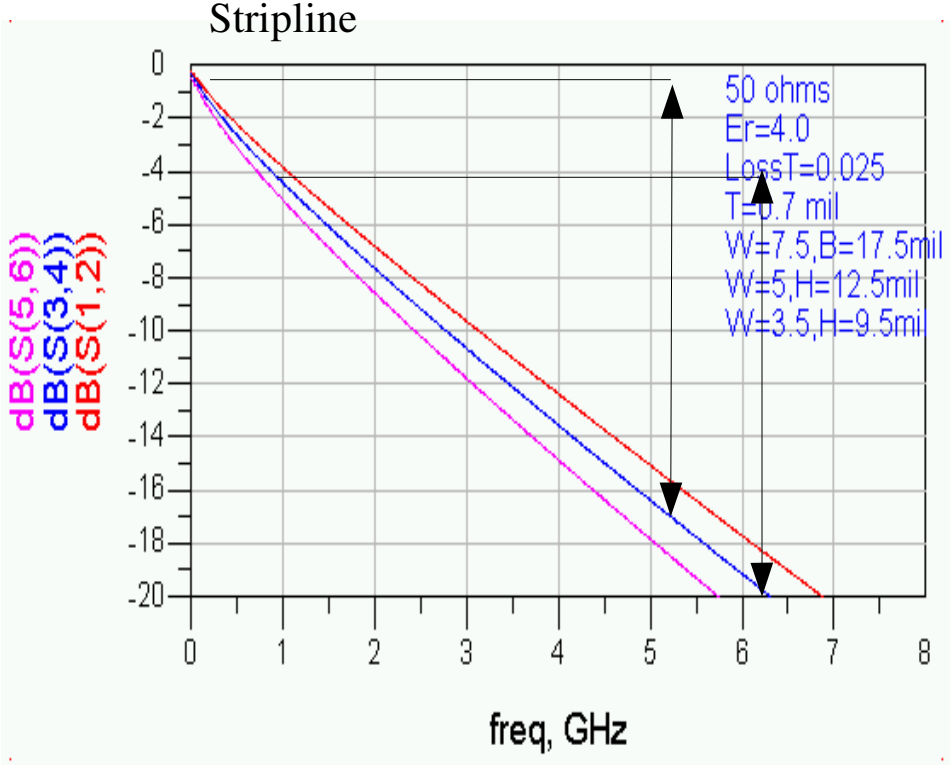
- **Backward compatibility with XAUI?**
  - ⇨Operating rate 2X, 4X rate of XAUI
- **Speed negotiation?**
- **Lane width negotiation similar to IB?**
- **Coding 8B/10B vs 64/66B?**
  - ⇨Overhead penalty
  - ⇨Latency penalty

20” FR4 Loss Property

- **XAUI had only an ISI Loss of 4 dB**



ISI Loss
10.31 Gig 64/66B ~ 12.5 dB
12.5 Gig 8B10B ~ 11.5 dB



ISI Loss
10.31 Gig 64/66B ~ 16 dB
12.5 Gig 8B10B ~ 16 dB

Comparison of 8B/10B with 64/66B

Parameter	8B/10B	64/66B
Compatibility With XAUI	Yes	Dual Encoder/Decoder
Overhead	20.00%	3.00%
Encoder+Decoder Latency	~ 50 bits	~800 bits
Run Length	5	Statistically 2n53
Low Frequency Cutoff	0.1% f	~0.001 f
ISI Penalty For the Same Payload	Similar	Similar

Conclusion

- **XAUI was one of first interface to define HS chip to chip and backplane link.**
- **Looking back we have learned and we can leverage XAUI to define Ethernet in the Backplane.**
- **At the physical layer we can also leverage work of CX4, 4 Gig FC, XFI, and OIF CEI.**
  - ⇨ **But even more important is defining the architectural requirement of Ethernet in the Backplane.**