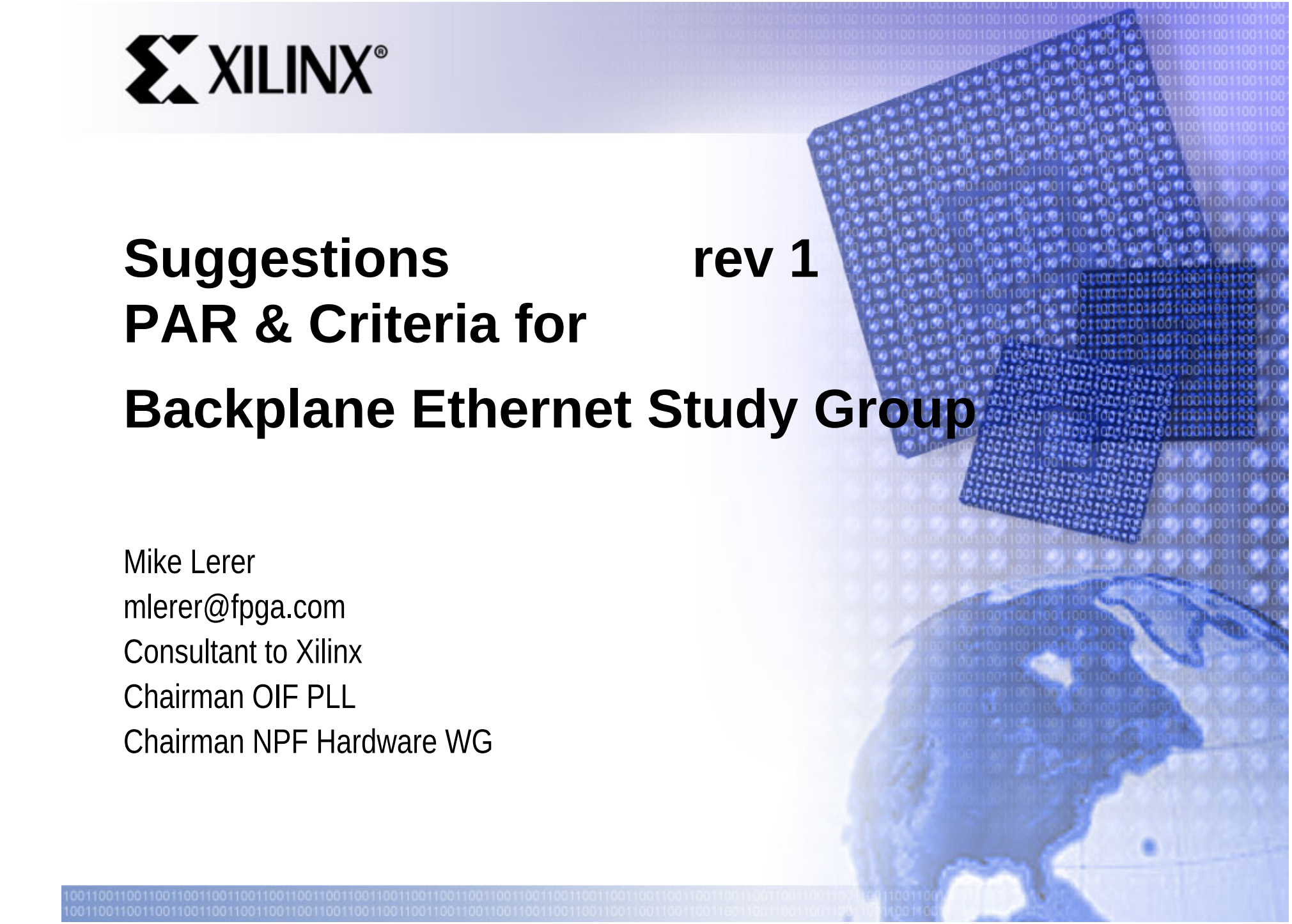

# Suggestions rev 1 PAR & Criteria for Backplane Ethernet Study Group

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# PAR Suggestions (1 of 4)

- Scope
  - Define Physical Layer Characteristics to extend Ethernet to Backplane Applications.
    - Environment
      - Greenfield Backplanes
      - Existing ATCA Backplane
      - Full Mesh, Star, and Dual Star Interconnect Topology
    - “Plug and Play” Interoperable Initialization Sequence for Links.

      This is currently Missing from OIF CEI.

# PAR Suggestions (2 of 4)

- Scope
  - Define Physical Layer Characteristics to extend Ethernet to Backplane Applications.

    - Speeds

      **The Backplane application needs 50 to 100% speedup**

      - 3.125 Gigabits per Lane 1 or 4 Lanes
      - 6.250 Gigabits per Lane 1, 2, or 4 Lanes
      - 10.3125 Gigabits per Lane 1 or 2 Lanes

# PAR Suggestions (3 of 4)

- Scope
  - Define Physical Layer Characteristics to extend Ethernet to Backplane Applications.

    - Objectives
      - Minimize Power Dissipation
      - Control EMI

# PAR Suggestions (4 of 4)

- Purpose
  - Extend 802.3 for use in internal system interconnect ( Backplane) for several markets:
    - Telecom Equipment ( PICMG ATCA )
    - Enterprise Computing

# 5 Criteria

- Broad Market Potential
- Compatibility with IEEE Std 802.3
- Distinct Identity
- Technical Feasibility
- Economic Feasibility

# 5 Criteria

- Broad Market Potential
  - Ethernet inside the box solutions already have a substantial market presence
    - PICMG Compact PCI 2.16
    - PICMG ATCA 3.1
    - Blade Servers
  - Forecast's indicate an increasing future market potential

# 5 Criteria

- Compatibility with IEEE Std 802.3
  - Absolutely
  - The only intent should be to extend the electrical specifications to cover the backplane.

# 5 Criteria

- Distinct Identity
  - Not in conflict with other work
  - Backplane is a unique environment
  - Substantially different from other 802.3 specs/ solutions

# 5 Criteria

- Technical Feasibility
  - OIF CEI work has developed a methodology for Channel Compliance and both 6+ Gig and 11+ Gig signaling over copper backplane.
  - UXPi Consortium committed to backplane signaling at speeds up to 11+ Gigabits/sec
  - SerDes capable of 3.125 to 11+ Gigabit are currently available from many manufacturers
    - Xilinx has Virtex-II Pro™ FPGA's
      - From 4 to 24 SerDes
      - Each Capable of 622Mbps to 3.125 Gigabits/sec
    - Xilinx has Virtex-II Pro X™ FPGA's
      - From 8 to 20 SerDes
      - Each Capable of 2.488 to 10.3125 Gigabits/sec
  - Channel (Backplane and Connector's) capable of 11+ Gigabit are available from many manufacturers. (Further details in Brian Seemann presentation later)

# 5 Criteria

- Economic Feasibility
  - Existing SerDes capable devices demonstrate reasonable costs and product viability.
  - The benefits of Ethernet Standardization almost inevitably lead to increased volume and multiple interoperable suppliers. This only accelerates the cost advantages.