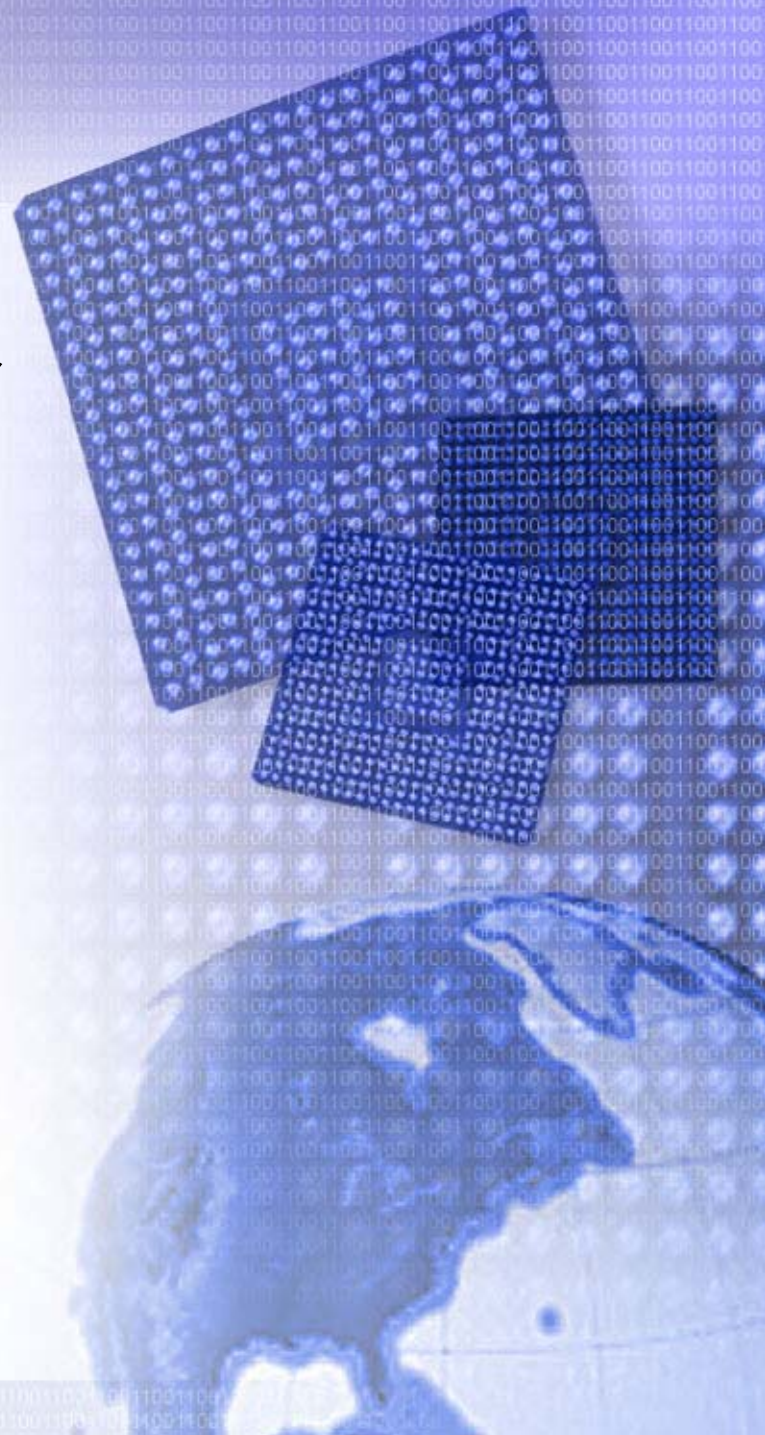
# Demonstration of Technical & Economic Feasibility

**Results are presented which demonstrate the technical and economic feasibility of backplane signaling at 5+ and 10+ Gigabits/second**

Brian Seemann

Xilinx



# Goals of Technical Study

- Produce a representative set of backplanes that use currently available components and construction technology
- Characterize the backplanes' performance capabilities
- Demonstrate transmission of signals using currently available, mainstream silicon product

# Objectives of this Presentation

- Present a body of existing evidence, representative of the industry's knowledge of backplane technology
- Demonstrate technical feasibility of 10Gbps NRZ Physical Electrical layer backplane communication
- Demonstrate that the proposed "Backplane Ethernet" is feasible

# Presentation flow

- Backplanes analyzed
  - Matrix
  - Pictures
  - Descriptors
- Technical approach
  - Characterization
  - Signaling assumption – NRZ – least equalization
  - Simulation
  - Stat eye
  - Silicon signal
- Results
  - Picture
  - Shots of sim/stat eye/silicon
  - Conclusion for each
- Summary matrix – green squares for good
- Conclusions

# Backplanes Characterized

- BP-A XAUI Reference Design / Tyco HM-Zd / Nelco
- BP-D Xilinx-designed / Teradyne GBX / Rogers
- BP-DF Xilinx-designed / Teradyne GBX / FR4
- BP-ER Xilinx-designed / ERNI 0XT / Rogers
- BP-E Xilinx-designed / ERNI 0XT / FR4
- BP-F Winchester-designed / SIP 1000 / Rogers
- BP-F20 Winchester-designed ATCA / SIP 1000-I / Rogers
- BP-F40 Winchester-designed ATCA / SIP 1000-I / Rogers
- BP-G "Tier 1" Systems mfg / ERNI ERmet-Zd / Rogers

# Backplanes Studied

| Designator | Configuration | Connector | Designed by | Routing | Backplane Material, Layers | Line Card | Distances | Traces |
|---|---|---|---|---|---|---|---|---|
| BP-A | XAUI Reference Design | Tyco HM-zD | Tyco | Partial Route | 0.185", Nelco 4000-2, | Nelco | 2+30+2 =34 inch Nelco | 8 pairs routed |
| BP-C | ATCA Platform | Tyco HM-zD | Kaparel PICMG | High Density, full route | FR4 | FR4 | | |
| BP-D | Full Mesh and Star | Teradyne GBX | Xilinx | High Density, full route | 0.220", Rogers Hybrid, 8 signal layers | FR4 | 3+20+3 =26 inch | W=8mil / S=8mil 55 pairs routed |
| BP-DF | Full Mesh and Star | Teradyne GBX | Xilinx | High Density, full route | 0.220", FR4, 8 signal layers | FR4 | 3+20+3 =26 inch | W=8mil / S=8mil 55 pairs routed |
| BP-ER | Full Mesh and Star | ERNI 0xT | Xilinx | High Density, full route | 0.265", Rogers Hybrid, 8 signal layers | FR4 | 3+21+3 =27 inch | W=8mil / S=8mil, 8 signal layers, 40 pair (star) 16 pair (mesh) routed |
| BP-E | Full Mesh and Star | ERNI 0xT | Xilinx | High Density, full route | 0.225", Rogers Hybrid, 8 signal layers | FR4 | 3+21+3 =27 inch | W=8mil / S=8mil, 8 signal layers, 40 pair (star) 16 pair (mesh) routed |
| BP-F | Full Mesh and Star | Winchester SIP 1000 | Wincester | Partial Route, Representative adjacent aggressors | Rogers Hybrid, | Probe | 4+26+4 =34 inch | |
| BP-F20 | ATCA Form Factor Selective Route | Winchester SIP 1000 I-Platform | Winchester | Partial Route, Representative adjacent aggressors | Rogers Hybrid, | Rogers | 20 inch | |
| BP-F40 | ATCA Form Factor Selective Route | Winchester SIP 1000 I-Platform | Winchester | Partial Route, Representative adjacent aggressors | Rogers Hybrid, | Rogers | 40 inch | |
| BP-G | Dual Star | ERNI ERMET-zD | Tier 1 Customer | Actual application route | 0.230" Rogers Hybrid | Probe | 3.5+15.5 +3.5 =22.5 Inch | |

# Analysis Procedure

Physical Backplane

Physical Silicon

Measure Through and Crosstalk S-Parameters

Drive Backplane with silicon

Generate Linear Eq Parameters

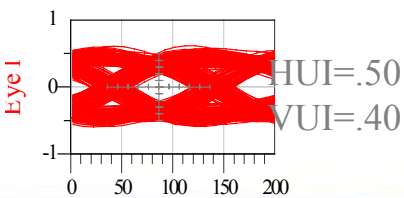
Generate DFE Eq Parameters

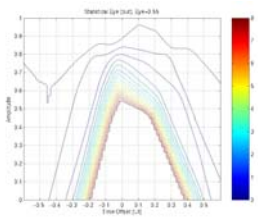
Utilize Signal specifications from OIF and UXPi

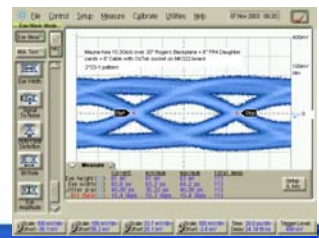
Simulate in Time Domain

Plot Statistical Eye

Monitor Channel Output with Scope

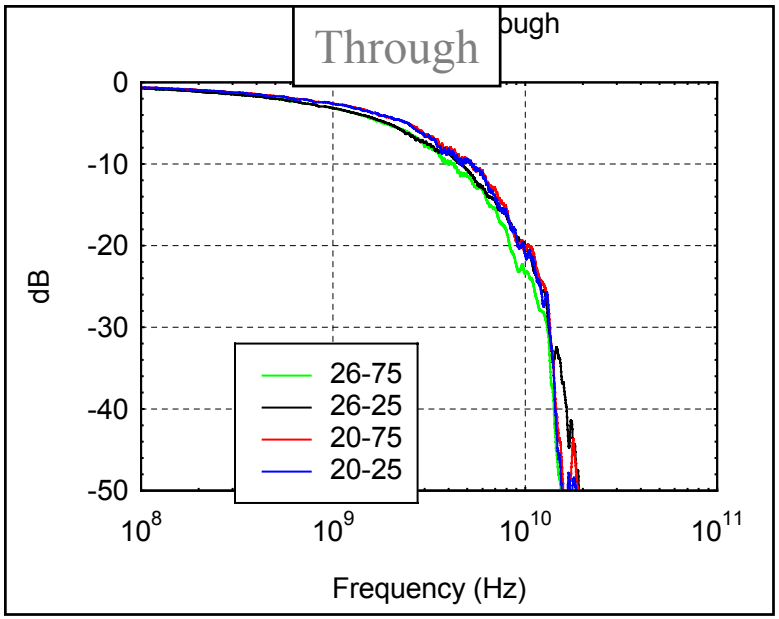


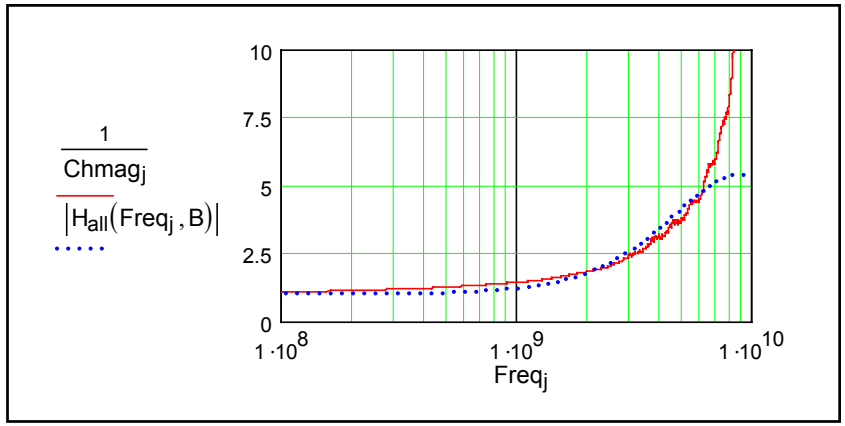


# EXAMPLE - Characterization

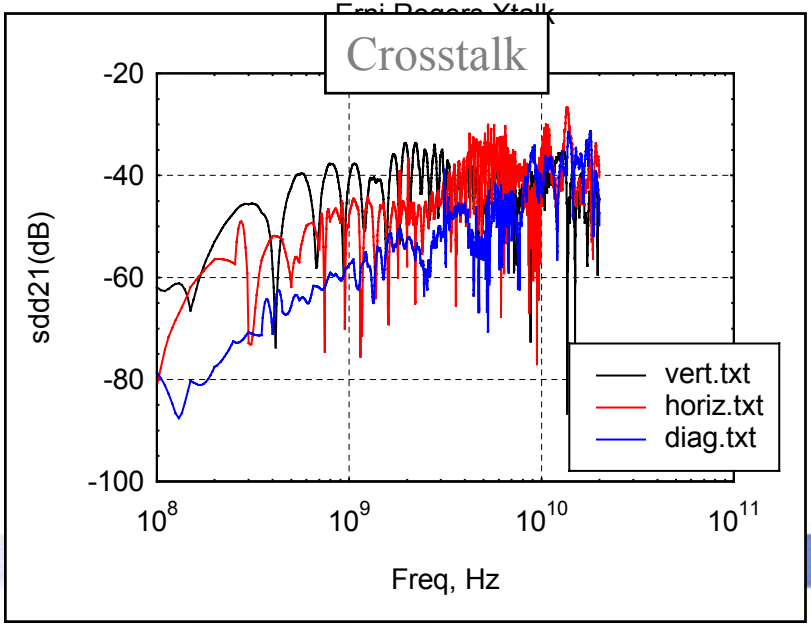
Through



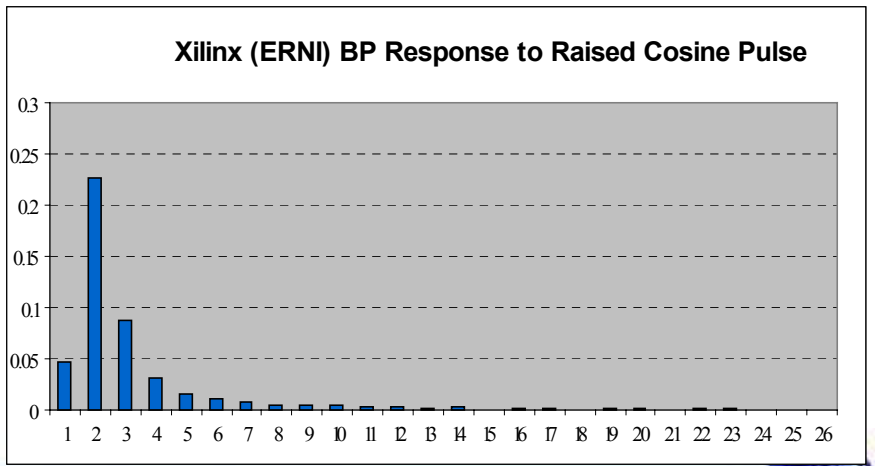

Equalizer Fit to Through




Crosstalk

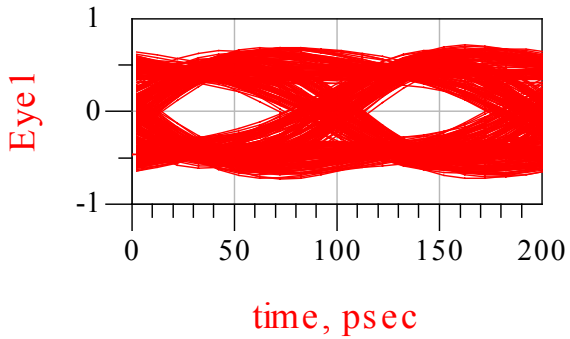



Pulse Response

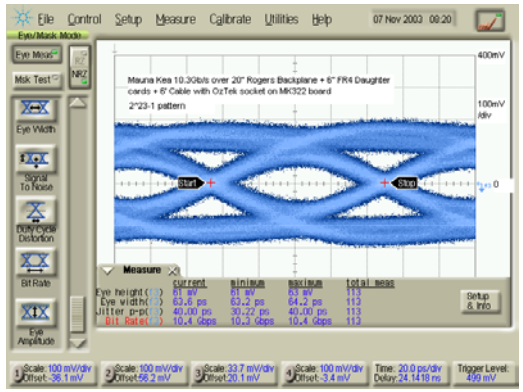


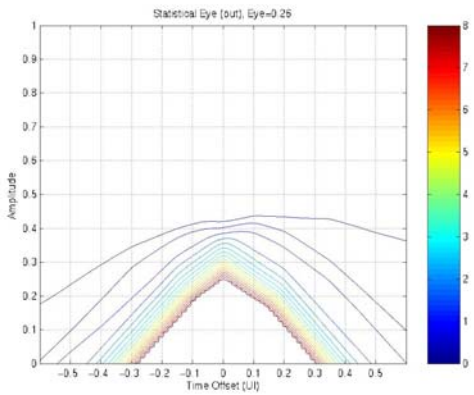
# EXAMPLE Results

Simulated Signal + X-Talk
- after Linear Equalizer

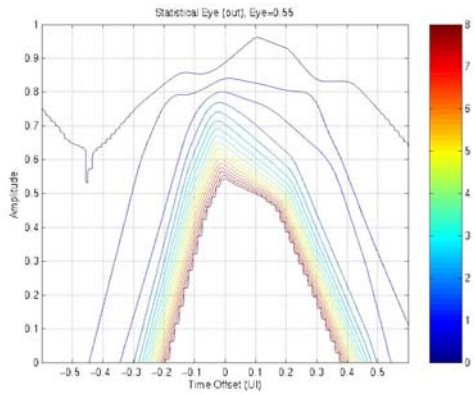



10Gbps Signal from Xilinx Virtex-II Pro-X FPGA
Measured Eye @ Channel Output , No Equalization



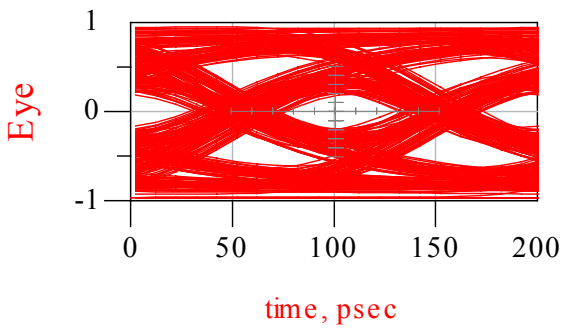




Stat Eye Signal + X-Talk
- after DFE Equalizer




Stat Eye Signal + X-Talk
- after Linear Equalizer

# Comparison of Statistical Eye to Time Domain Eye

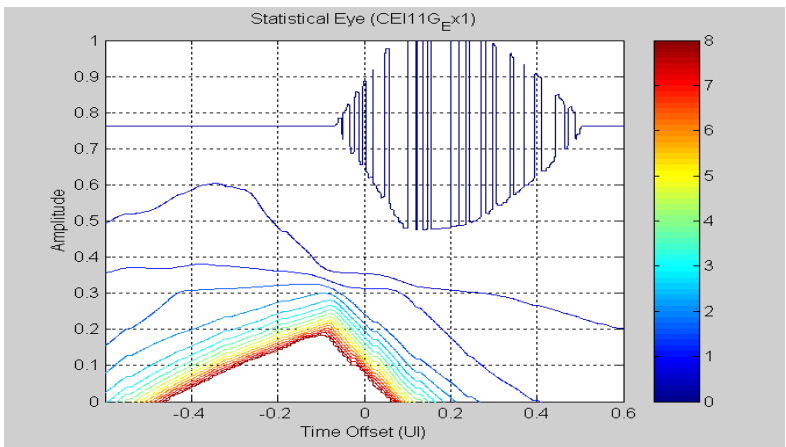



H-UI=.55
V-UI=.30

- Compare Simulated and Stat Eyes
- with no Equalization,
- no crosstalk.
- 800 bits random data.

- Sim hor. opening = 0.55 UI

- Sim vert. opening = 0.3 units.




- Compare Simulated and Stat Eyes
- with no Equalization,
- no crosstalk.

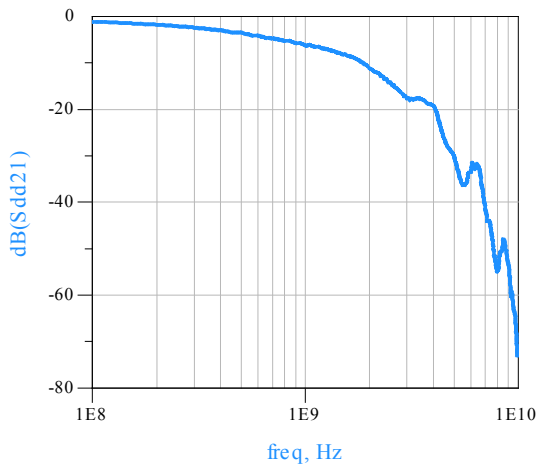
- Stat hor. opening (Q=8) = 0.51 UI

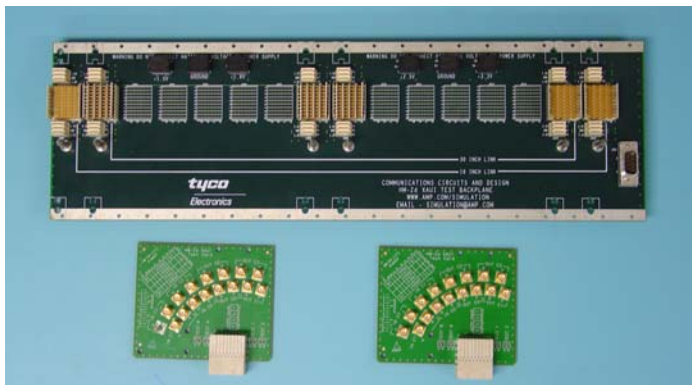
- Stat vert. opening = 0.35 units.

# BP-A (XAUI / HM-Zd) Configuration

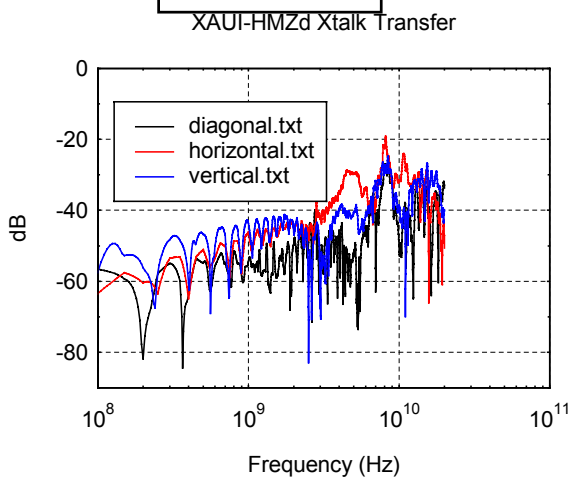
| Backplane | Config | Connector | Backplane Material | Lengths Inches | Traces | Vias |
|---|---|---|---|---|---|---|
| **BP-A XAUI** | Reference Design | Tyco HM-Zd | Nelco 4000-2 | 2+30+2 =34 inch | Low Density, Partial Route | Thru vias, Not Backdrilled |

Through



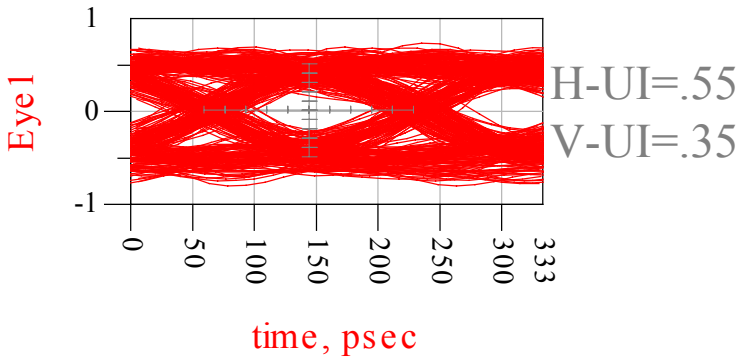




Crosstalk



# BP-A (XAUI) 6Gbps Results

Simulated Signal + X-Talk
- after Linear Equalizer




6.25Gbps Signal from Xilinx Virtex-II Pro-X FPGA
Measured Eye @ Channel Output

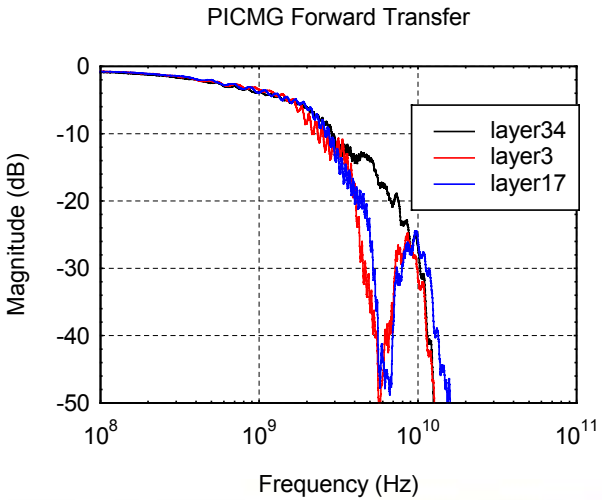
Stat Eye Signal + X-Talk
- after DFE Equalizer

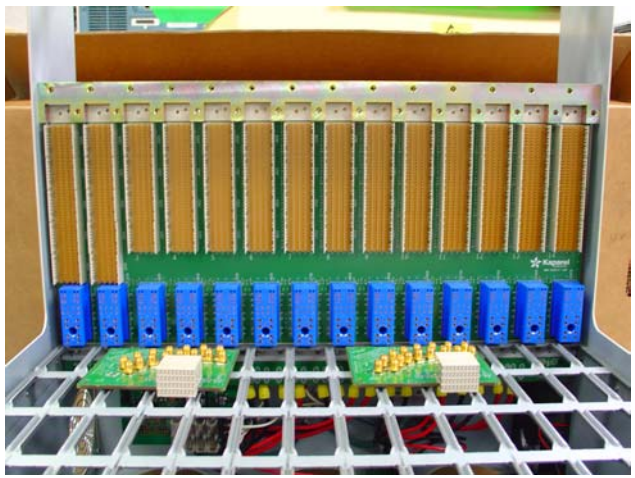
Stat Eye Signal + X-Talk
- after Linear Equalizer

# BP-C (PICMG ATCA) Configuration

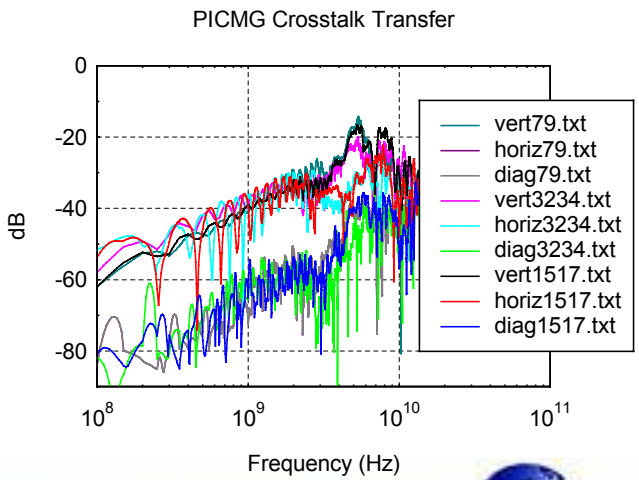
| Backplane | Config | Connector | Backplane Material | Lengths Inches | Traces | Vias |
|---|---|---|---|---|---|---|
| **BP-C** | Standard Backplane | Tyco HM-Zd | FR4 | | | Thru vias, Not Backdrilled |

Through



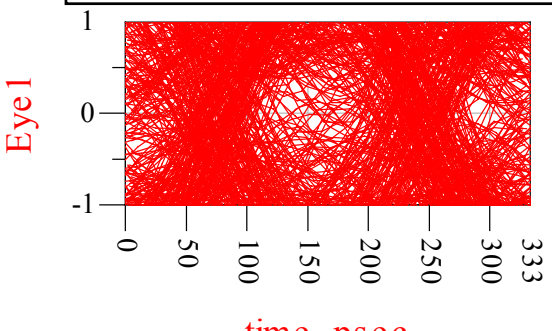



Crosstalk

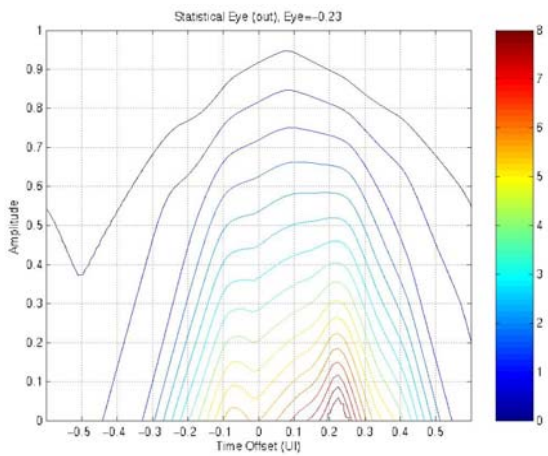


# BP-C (PICMG ATCA) Results – Layer 34

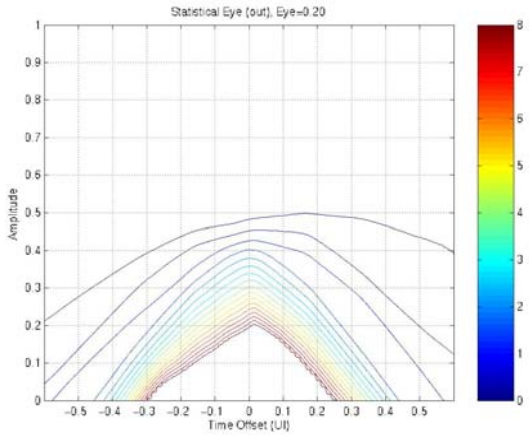
Simulated Signal + X-Talk
- after Linear Equalizer




Signal from Xilinx Virtex-II Pro-X FPGA
Measured Eye @ Channel Output



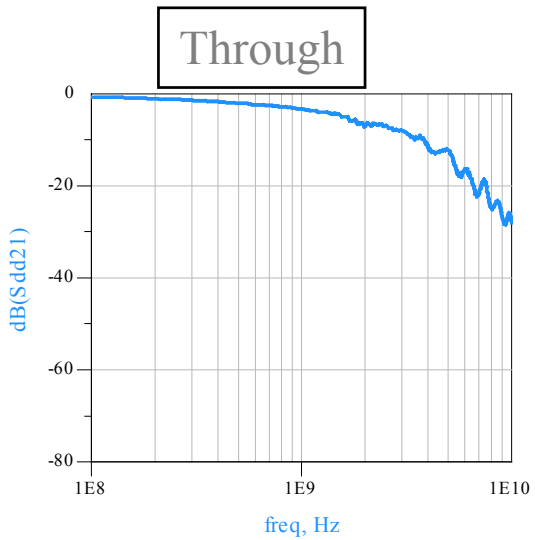

Stat Eye Signal + X-Talk
- after DFE Equalizer

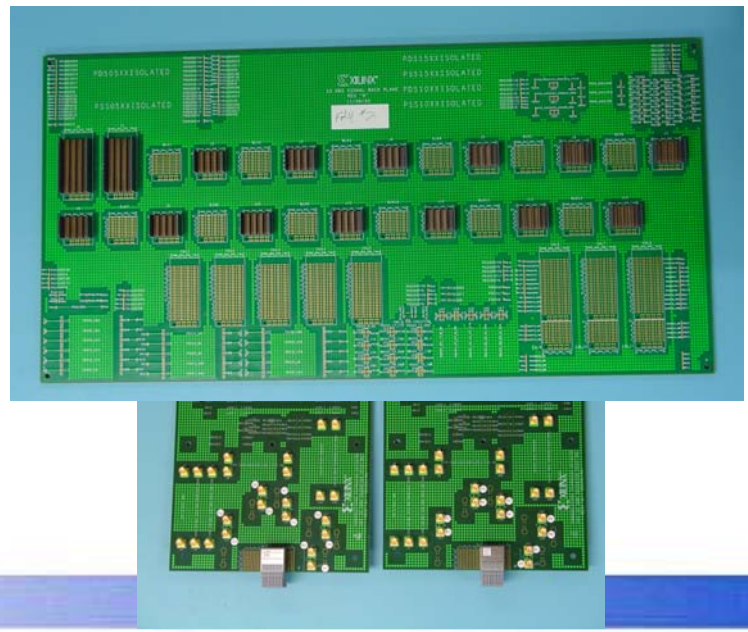


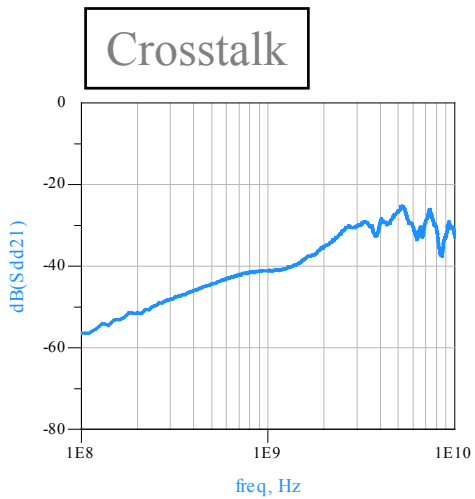

Stat Eye Signal + X-Talk
- after Linear Equalizer

# BP-D (Xilinx/GbX) Configuration

| Backplane | Config | Connector | Backplane Material | Lengths Inches | Traces | Vias |
|---|---|---|---|---|---|---|
| **BP-D Xilinx** | Concept Full Mesh and Star | Teradyne GBX | Rogers Hybrid (Daughters are FR4) | 3+20+3 =26 inch | W=8mil / S=8mil, 8 signal layers, High Density, Full Route | Thru vias, Backdrilled |

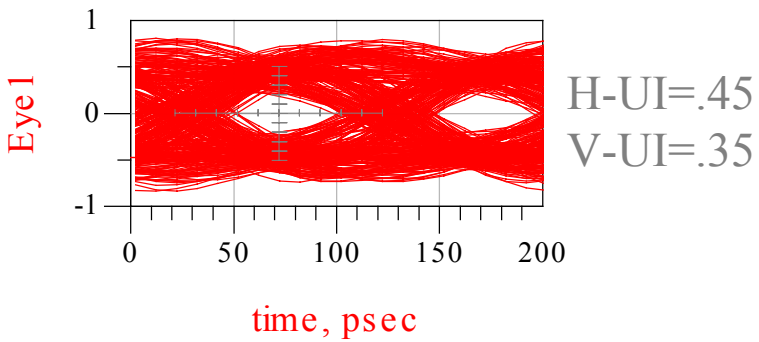




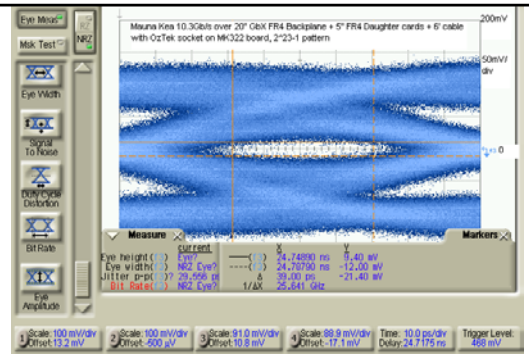
# BP-D (Xilinx/GBX) Results

Simulated Signal + X-Talk
- after Linear Equalizer




H-UI=.45
V-UI=.35

10Gbps Signal from Xilinx Virtex-II Pro-X FPGA
Measured Eye @ Channel Output , No Equalization
(this is actually from FR4 version of board)



Stat eye unavailable

Stat eye unavailable

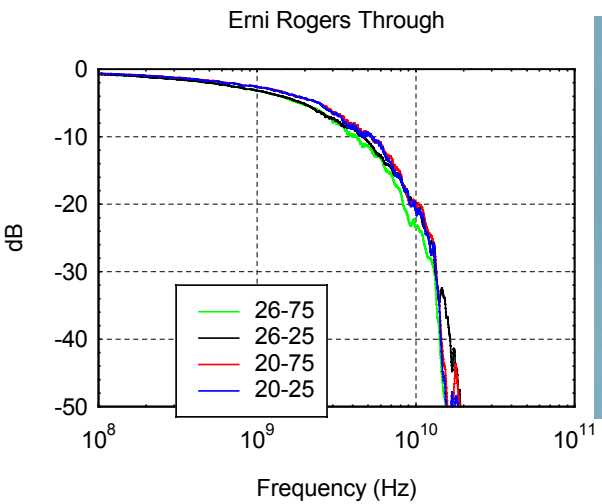
Stat Eye Signal + X-Talk
- after DFE Equalizer

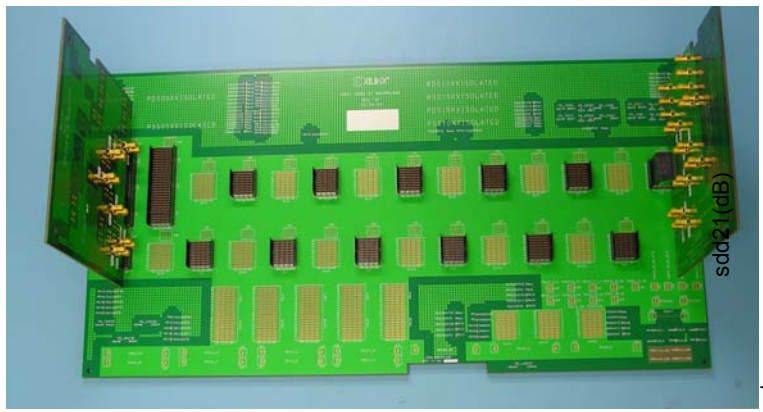
Stat Eye Signal + X-Talk
- after Linear Equalizer

# BP-ER (Xilinx/0XT) Configuration

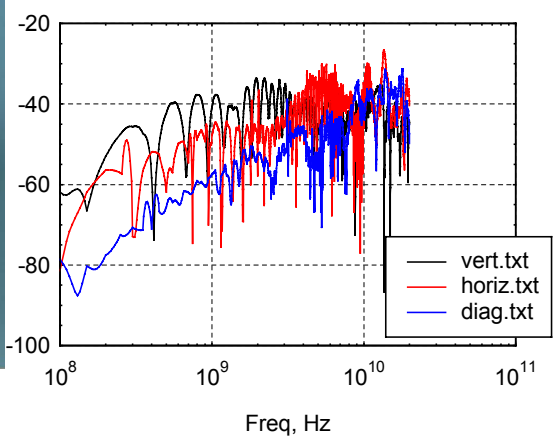
| Backplane | Config | Connector | Backplane Material | Lengths Inches | Traces | Vias |
|---|---|---|---|---|---|---|
| **BP-ER Xilinx** | Concept Full Mesh and Star | ERNI 0XT | Rogers BP FR4 Line | 3+21+3 =27 inch | W=8mil / S=8mil, 8 signal layers, High Density, Full Route | Thru vias, Backdrilled |

Through



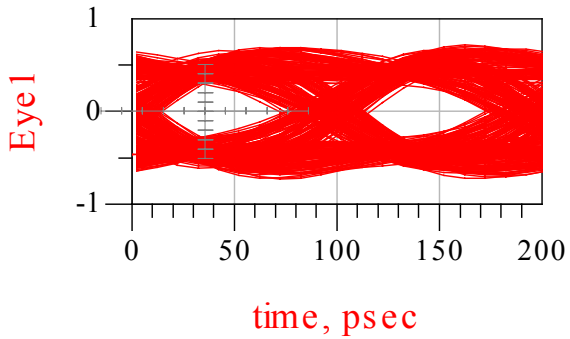




Crosstalk



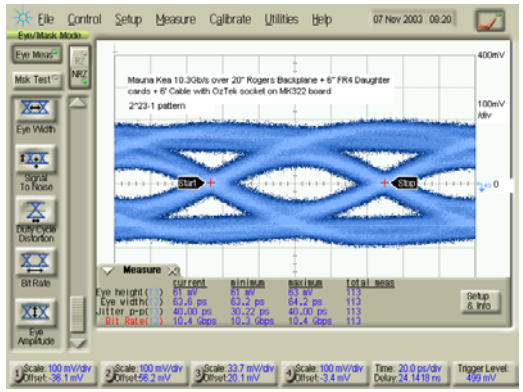
# BP-ER (Xilinx/0XT) Results

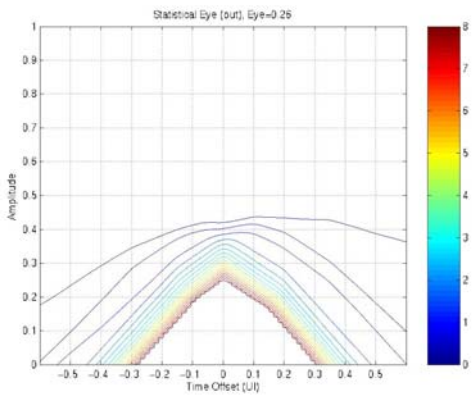
Simulated Signal + X-Talk
- after Linear Equalizer



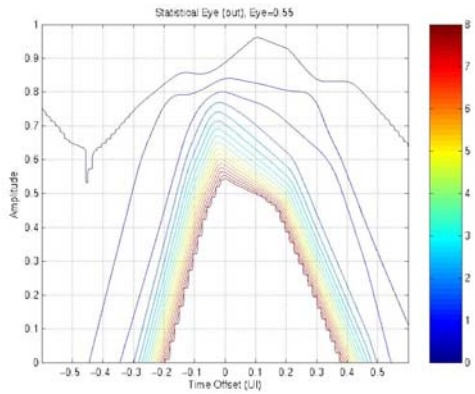

H-UI=.55
V-UI=.55

10Gbps Signal from Xilinx Virtex-II Pro-X FPGA
Measured Eye @ Channel Output , No Equalization




Stat Eye Signal + X-Talk
- after DFE Equalizer

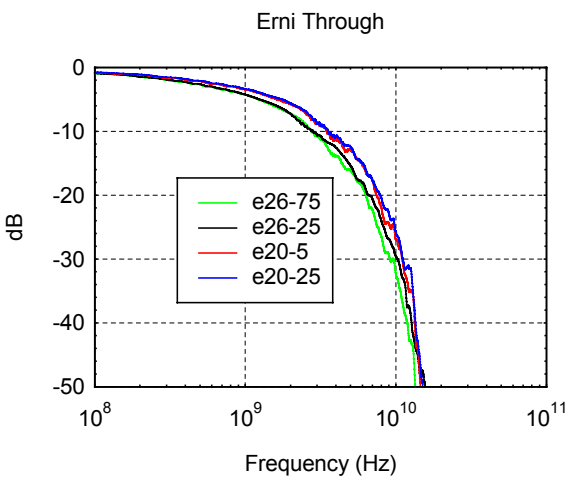


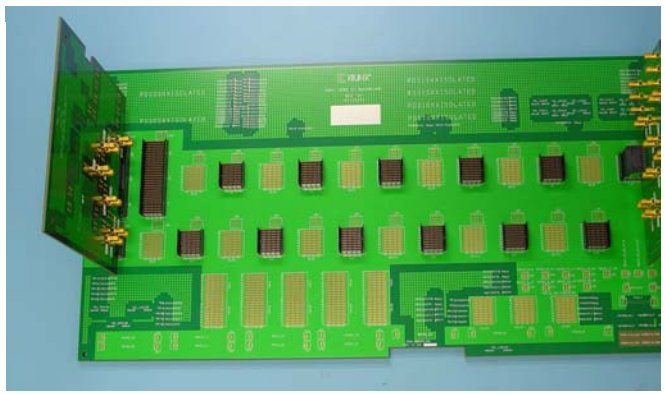

Stat Eye Signal + X-Talk
- after Linear Equalizer

# BP-E (Xilinx/0XT) Configuration

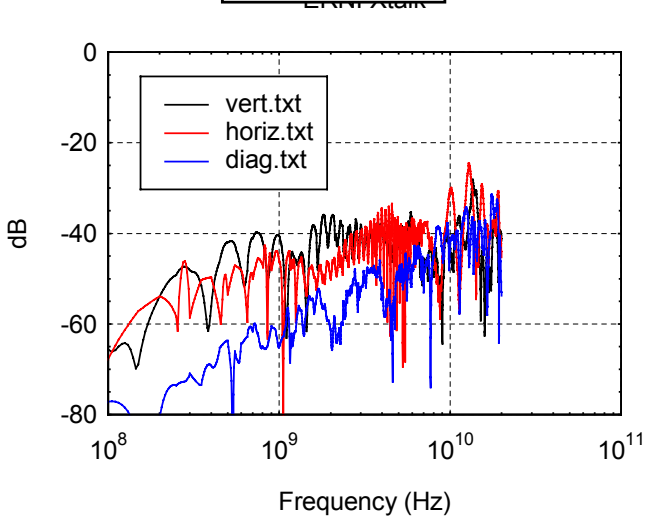
| Backplane | Config | Connector | Backplane Material | Lengths Inches | Traces | Vias |
|---|---|---|---|---|---|---|
| **BP-E Xilinx** | Concept Full Mesh and Star | ERNI 0XT | FR4 (Daughters are FR4) | 3+21+3 =27 inch | W=8mil / S=8mil, 8 signal layers, High Density, Full Route | Thru vias, Backdrilled |

Through



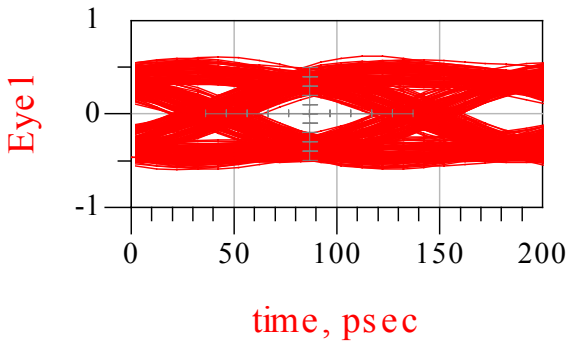



Crosstalk



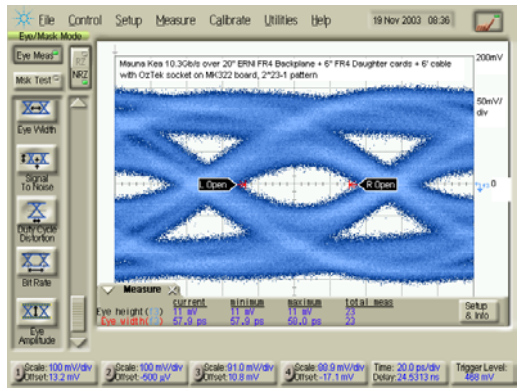
# BP-E (Xilinx/0XT) Results

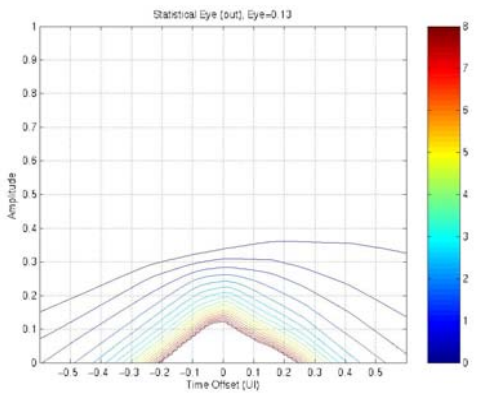
Simulated Signal + X-Talk
- after Linear Equalizer



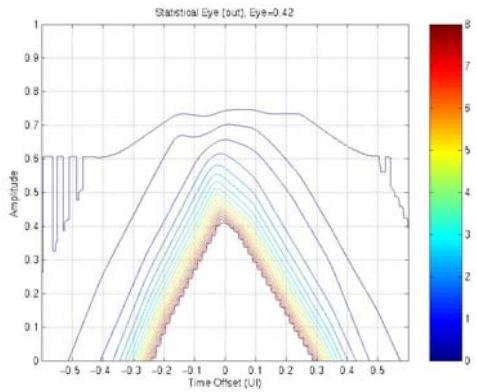

HUI=.50
VUI=.40

10Gbps Signal from Xilinx Virtex-II Pro-X FPGA
Measured Eye @ Channel Output , No Equalization




Stat Eye Signal + X-Talk
- after DFE Equalizer

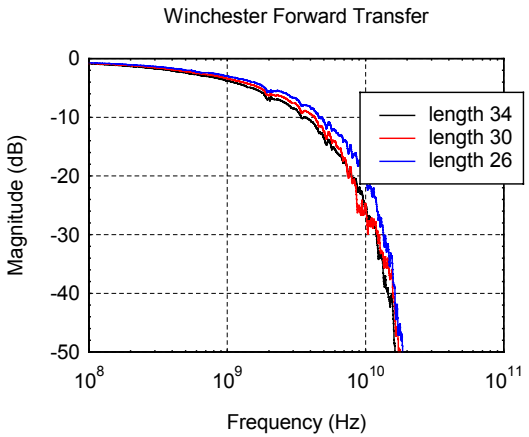


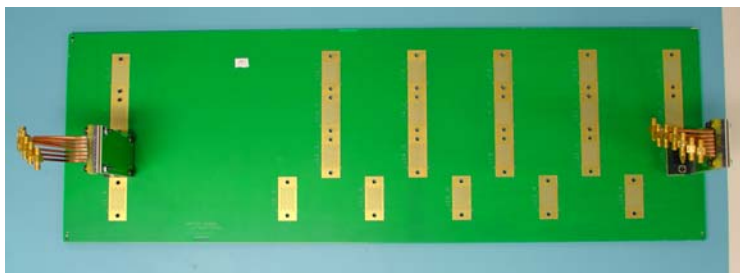

Stat Eye Signal + X-Talk
- after Linear Equalizer

# BP-F (Winchester/SIP) Configuration

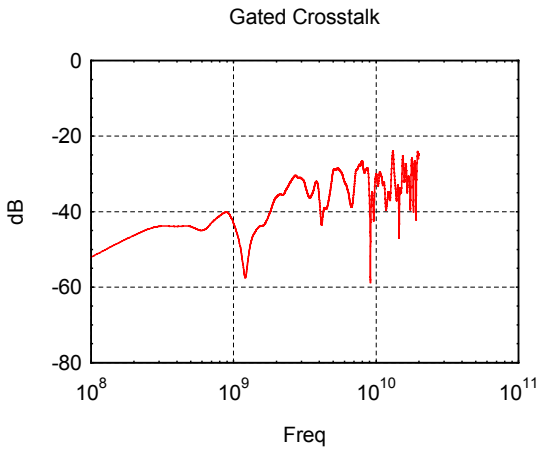
| Backplane | Config | Connector | Backplane Material | Lengths Inches | Traces | Vias |
|---|---|---|---|---|---|---|
| **BP-F Winchester** | Concept Selective Route | Winchester SIP | Rogers Hybrid (Daughters are FR4) | 4+26+4 =34 inch | Low Density, Partial Route | Thru Vias, Backdrilled |

Through



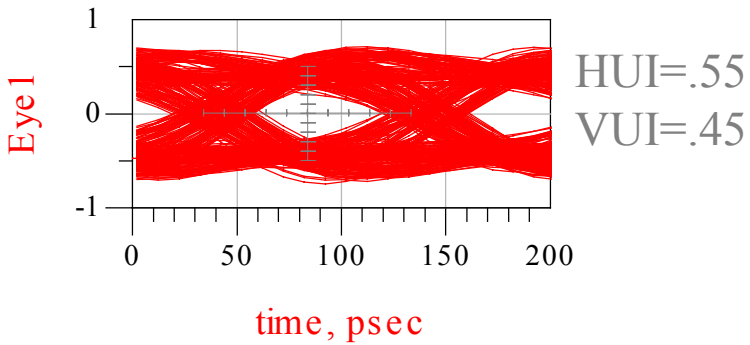



Crosstalk



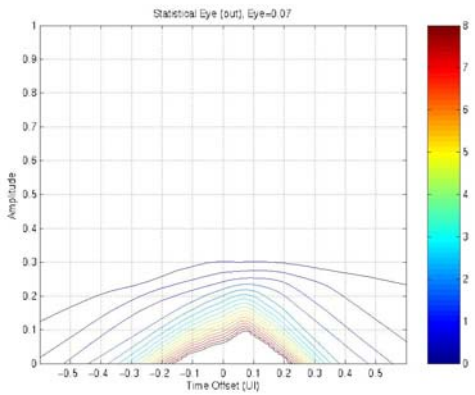
# BP-F (Winchester /SIP) Results

Simulated Signal + X-Talk
- after Linear Equalizer

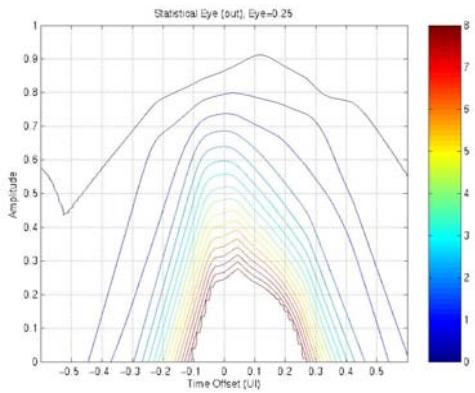



HUI=.55
VUI=.45

10Gbps Signal from Xilinx Virtex-II Pro-X FPGA
Measured Eye @ Channel Output



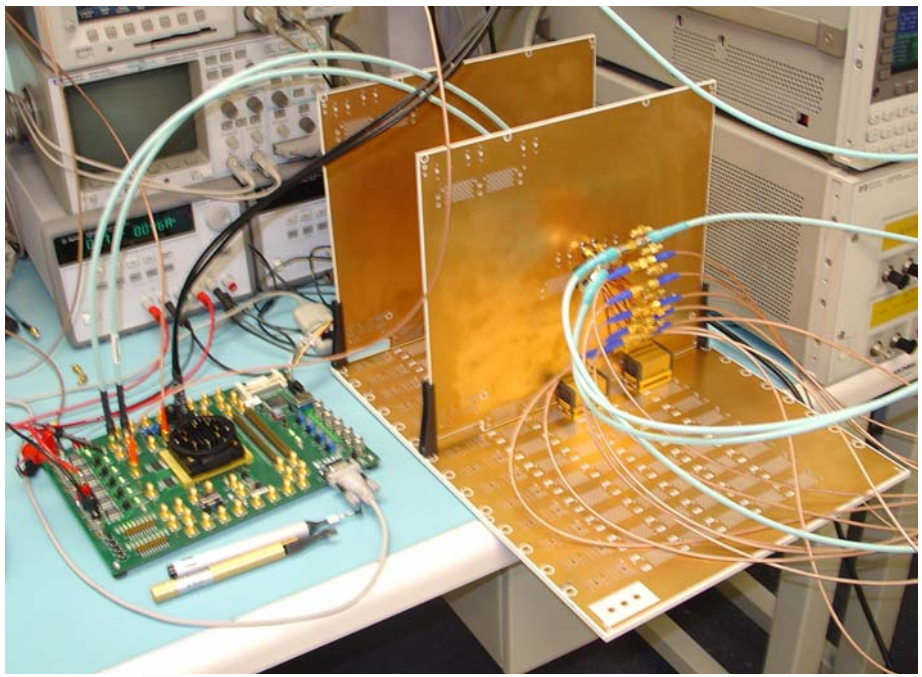

Stat Eye Signal + X-Talk
- after DFE Equalizer

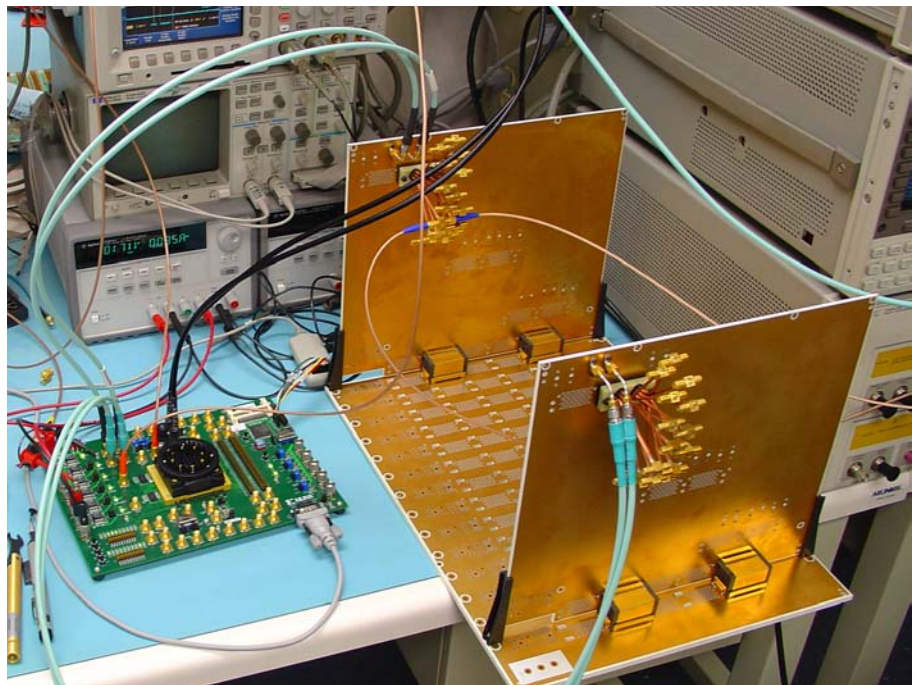



Stat Eye Signal + X-Talk
- after Linear Equalizer

# BP-F20 & F40 (Winchester/SIP) Configuration

| Backplane | Config | Connector | Backplane Material | Lengths Inches | Traces | Vias |
|---|---|---|---|---|---|---|
| **BP-F20 & F40 Winchester** | | Winchester SIP1000-I | Rogers Hybrid | 20 inches And 40 inches | | Thru Vias, Backdrilled |

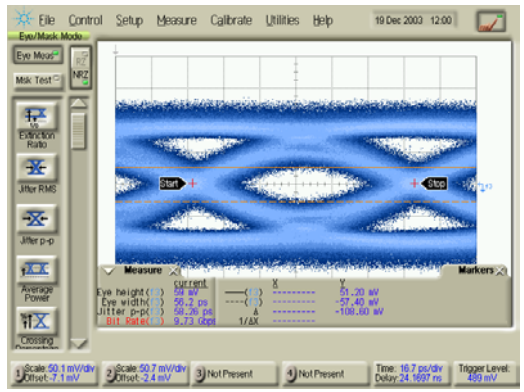


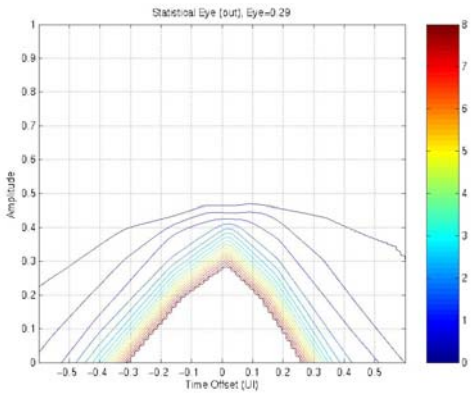


# BP-F20 (Winchester /SIP) Results

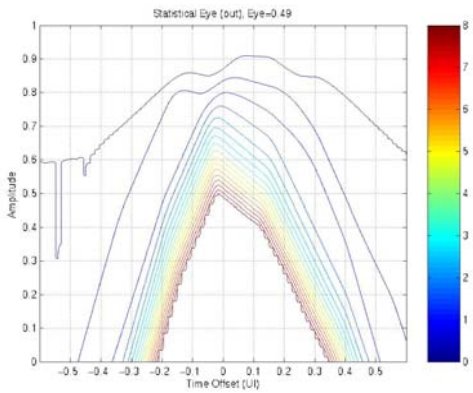
Simulated Signal + X-Talk
- after Linear Equalizer

10Gbps Signal from Xilinx Virtex-II Pro-X FPGA
Measured Eye @ Channel Output, No Equalization
8 Crosstalk Aggressors




Stat Eye Signal + X-Talk
- after DFE Equalizer

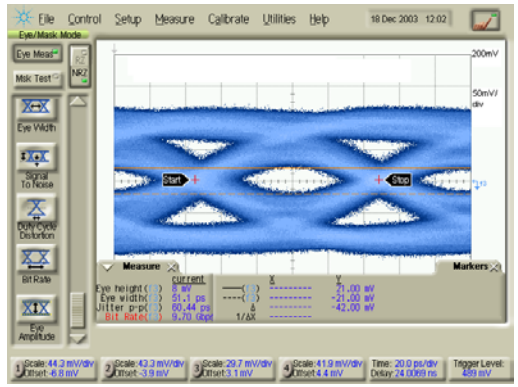


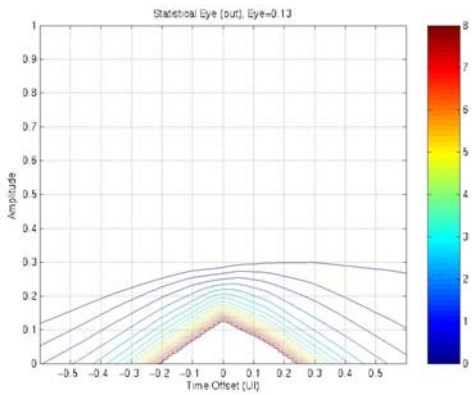

Stat Eye Signal + X-Talk
- after Linear Equalizer

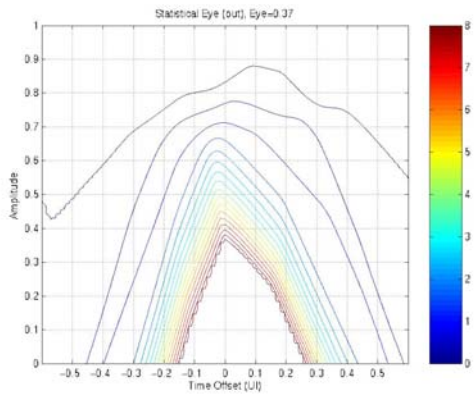
# BP-F40 (Winchester /SIP) Results

Simulated Signal + X-Talk
- after Linear Equalizer

10Gbps Signal from Xilinx Virtex-II Pro-X FPGA
Measured Eye @ Channel Output , No Equalization



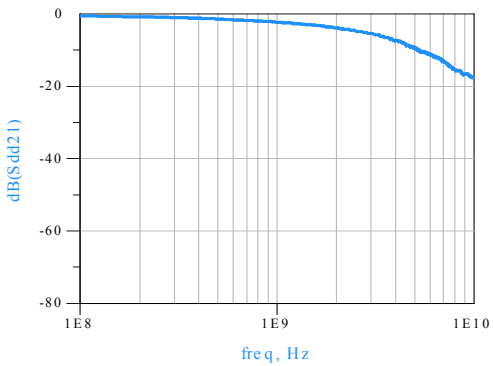

Stat Eye Signal + X-Talk
- after DFE Equalizer

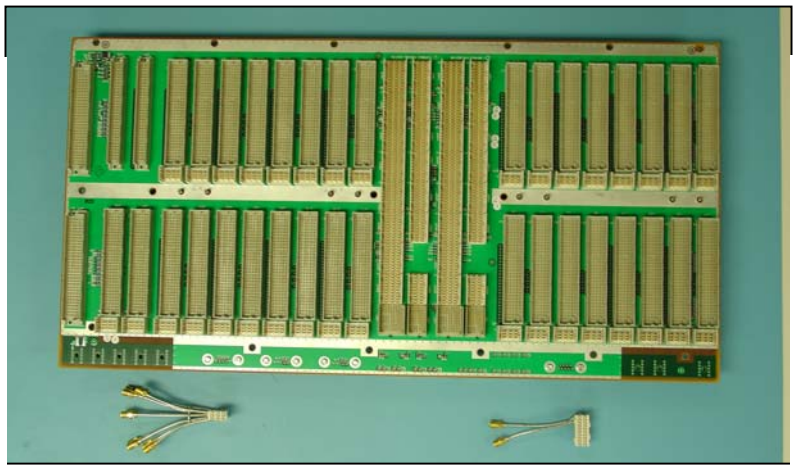
Stat Eye Signal + X-Talk
- after Linear Equalizer

# BP-G (Tier 1 Syst/ERmetZd) Configuration

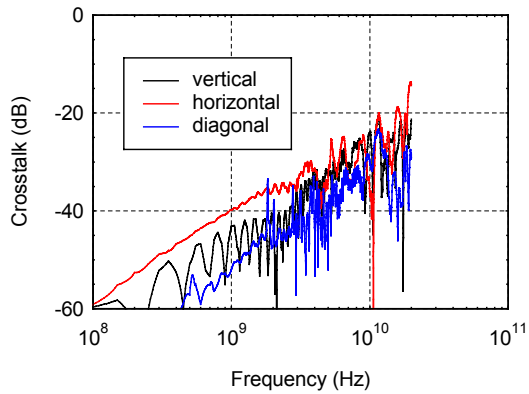
| Backplane | Config | Connector | Backplane Material | Lengths Inches | Traces | Vias |
|---|---|---|---|---|---|---|
| **BP-G**<br>**A "Tier 1" Syst Mfg** | Dual Star | ERNI ERmet-Zd | Rogers Hybrid<br>(Daughters are cable) | 3.5+15.5+3.5 =22.5" | | Thru Vias, Backdrilled |

Through



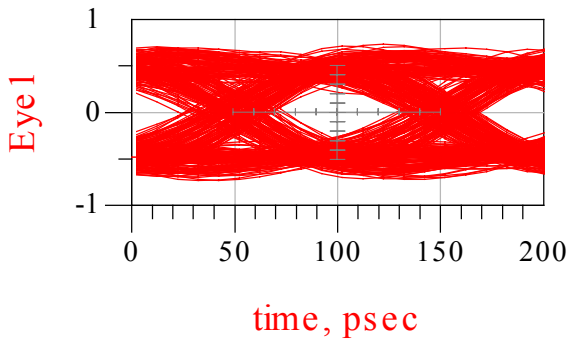



Crosstalk



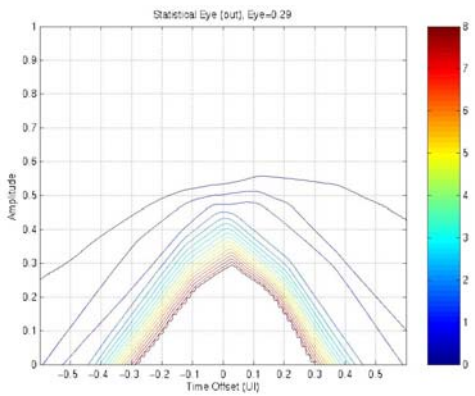
# BP-G (Tier 1/ERmetZd) Results

Simulated Signal + X-Talk
- after Linear Equalizer

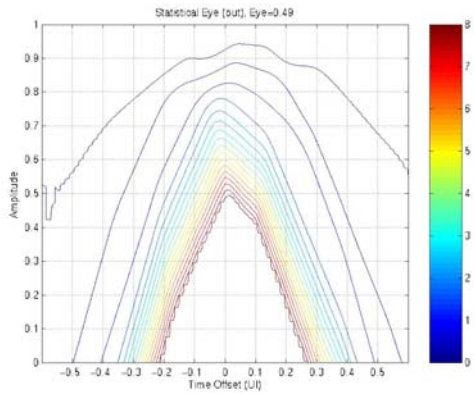



HUI=.55
VUI=.45

10Gbps Signal from Xilinx Virtex-II Pro-X FPGA
Measured Eye @ Channel Output




Stat Eye Signal + X-Talk
- after DFE Equalizer




Stat Eye Signal + X-Talk
- after Linear Equalizer

# Conclusions

- The backplanes shown have been, and can be built using presently available technology
- 10Gbps serial communication is demonstrated over multiple connectors
- Channels are driven with actual production 10Gbps silicon
- Basic 10Gbps NRZ signaling works over the backplanes studied
- Both Linear and DFE equalization work over the backplanes studied