Channel Model Criteria

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Subject : IEEE 802.3 Backplane Ethernet Study Group

Abstract : This presentation examines channel trace lengths in different back plane and mid plane configurations, touches on channel design considerations, and defines acceptable channel BER.

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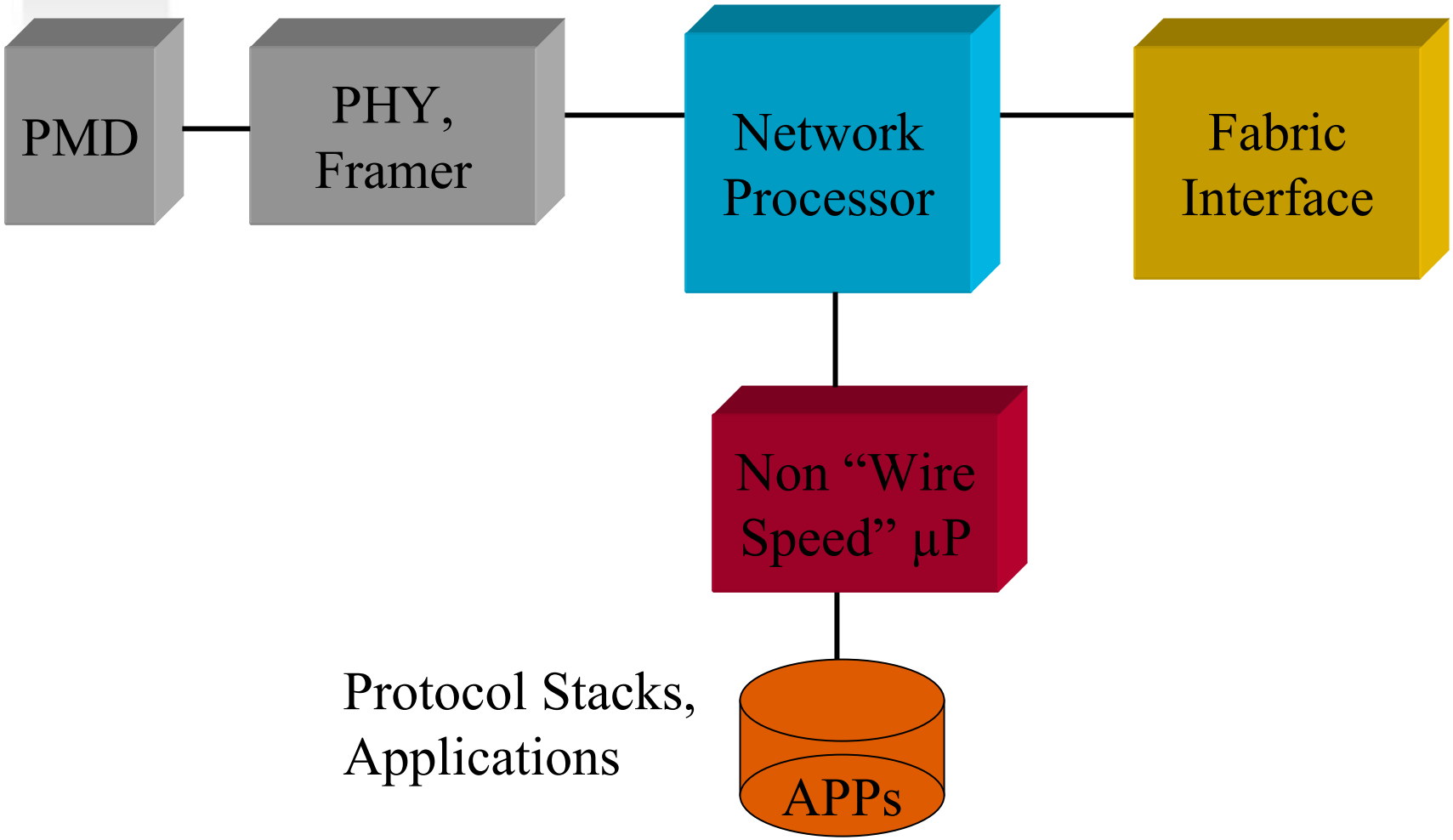
Overview

- Architectural Disclaimers
- Line Card Architecture
- Switch Fabric Architecture
- Trace Length Combinations – Max
- Trace Length Combinations - Min
- Channel Design Considerations
- Acceptable Channel BER

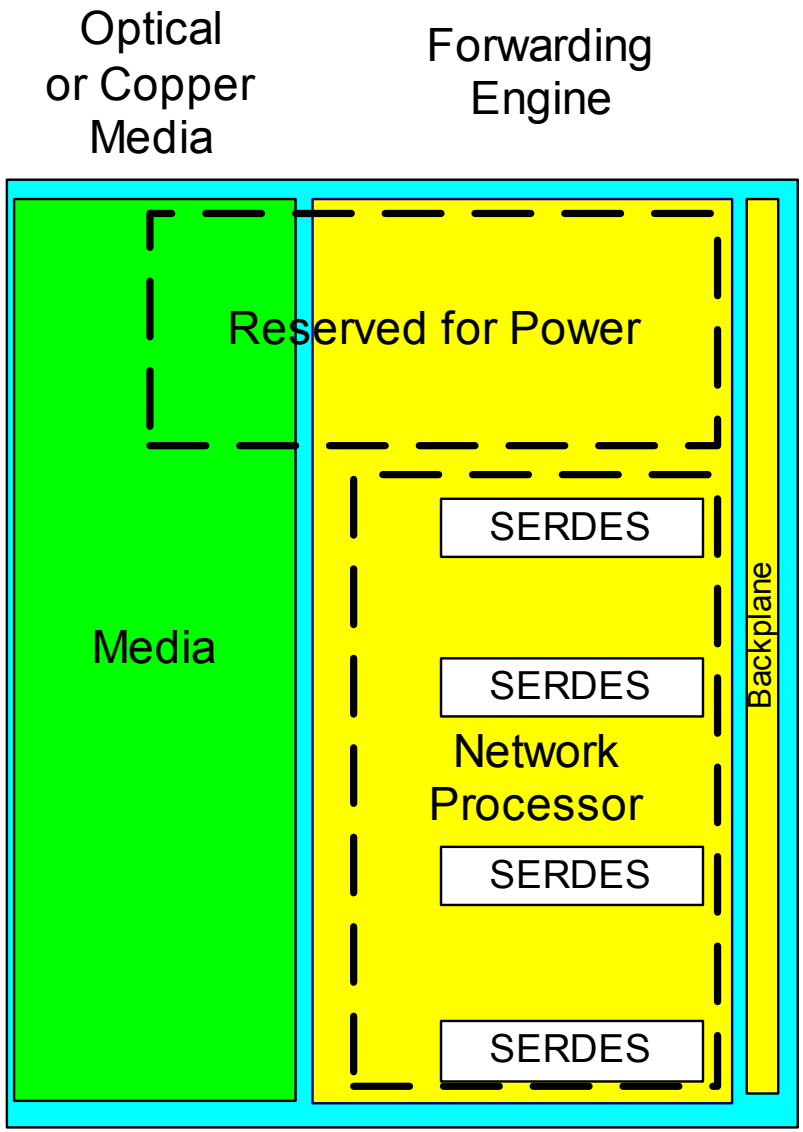
Architectural Disclaimers

- There are many ways to implement a line card - fabric system. This presentation covers only a few types built to date.
- Channel performance is measured using surface mount SMA test assemblies.
- Assume Back Plane and Mid Plane connectors are always on the right side of the line card / switch fabric.
- Two popular chassis heights: 24in to 34in height (2 or 3 per rack), 10in to 14in height (5 to 8 per rack).

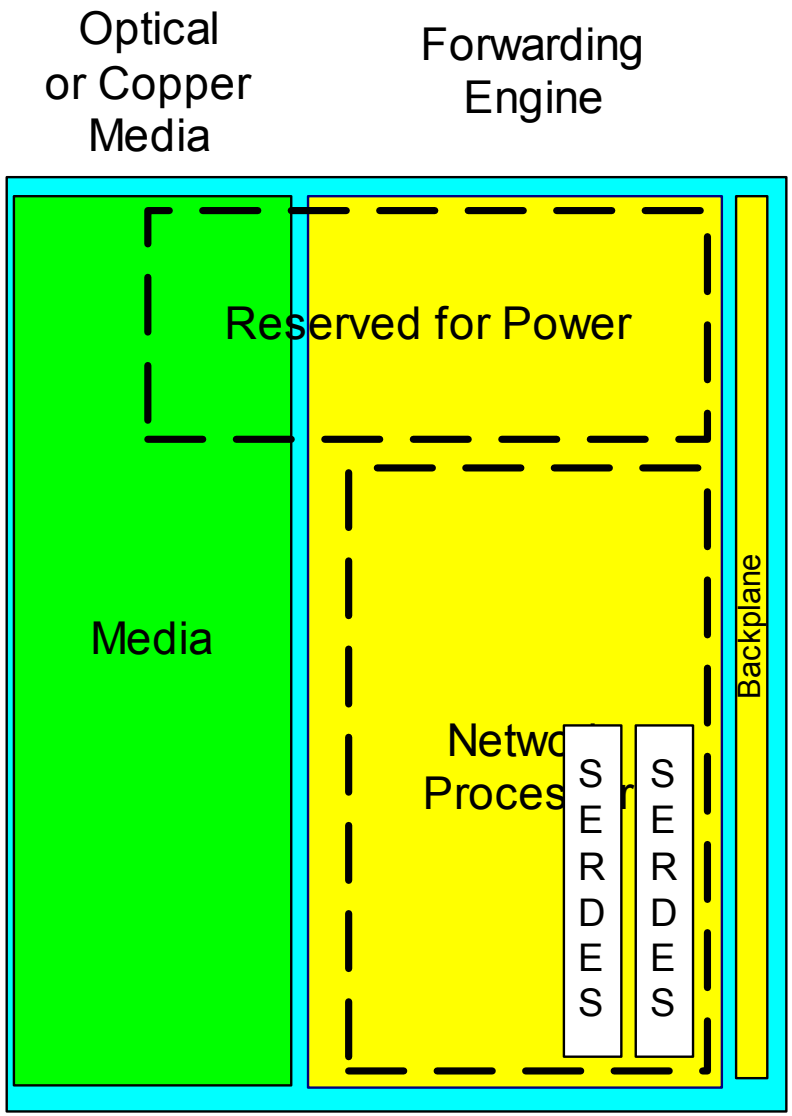
Sample Line Card Architecture



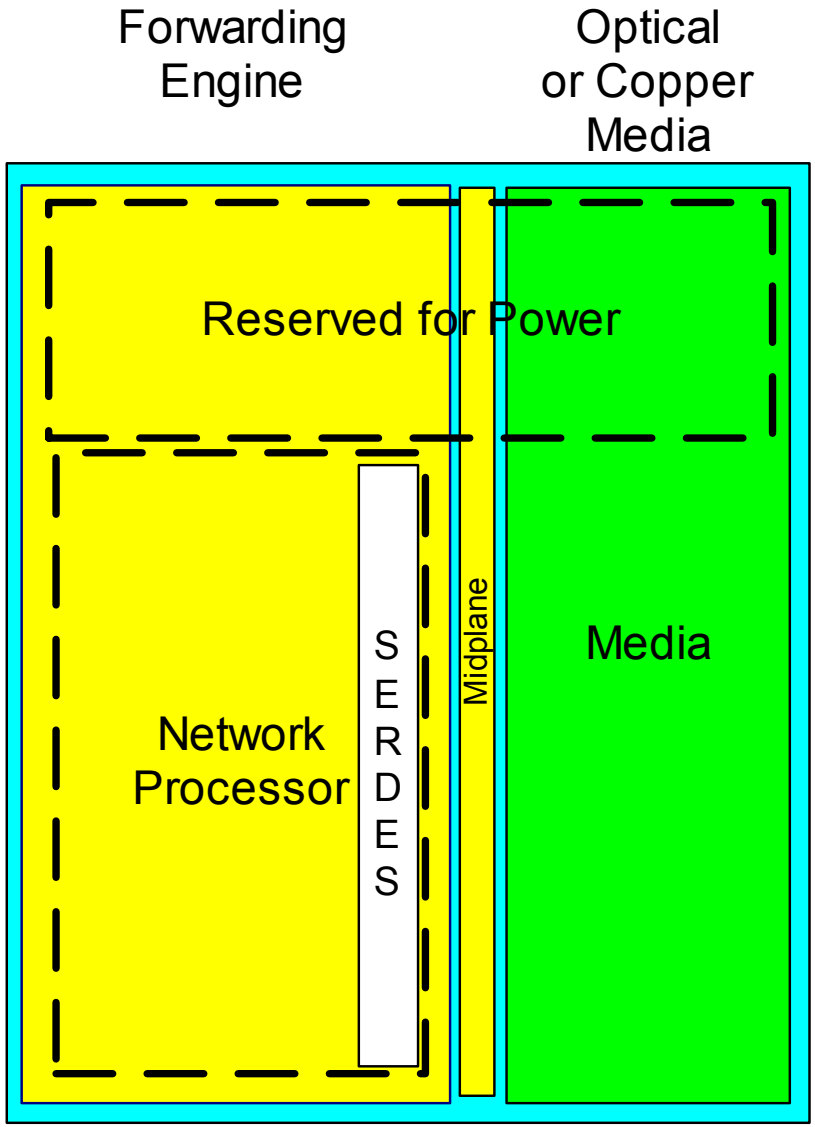
Sample Line Card Architecture 1



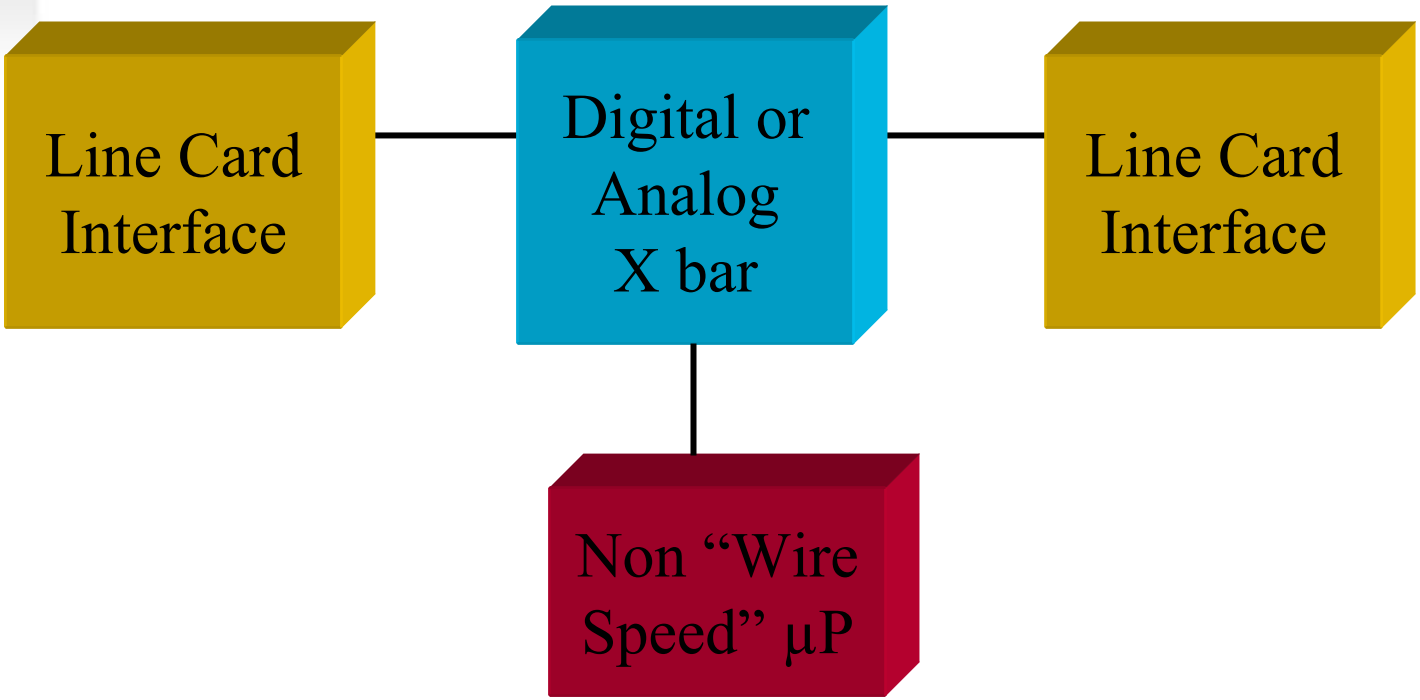
Sample Line Card Architecture 2



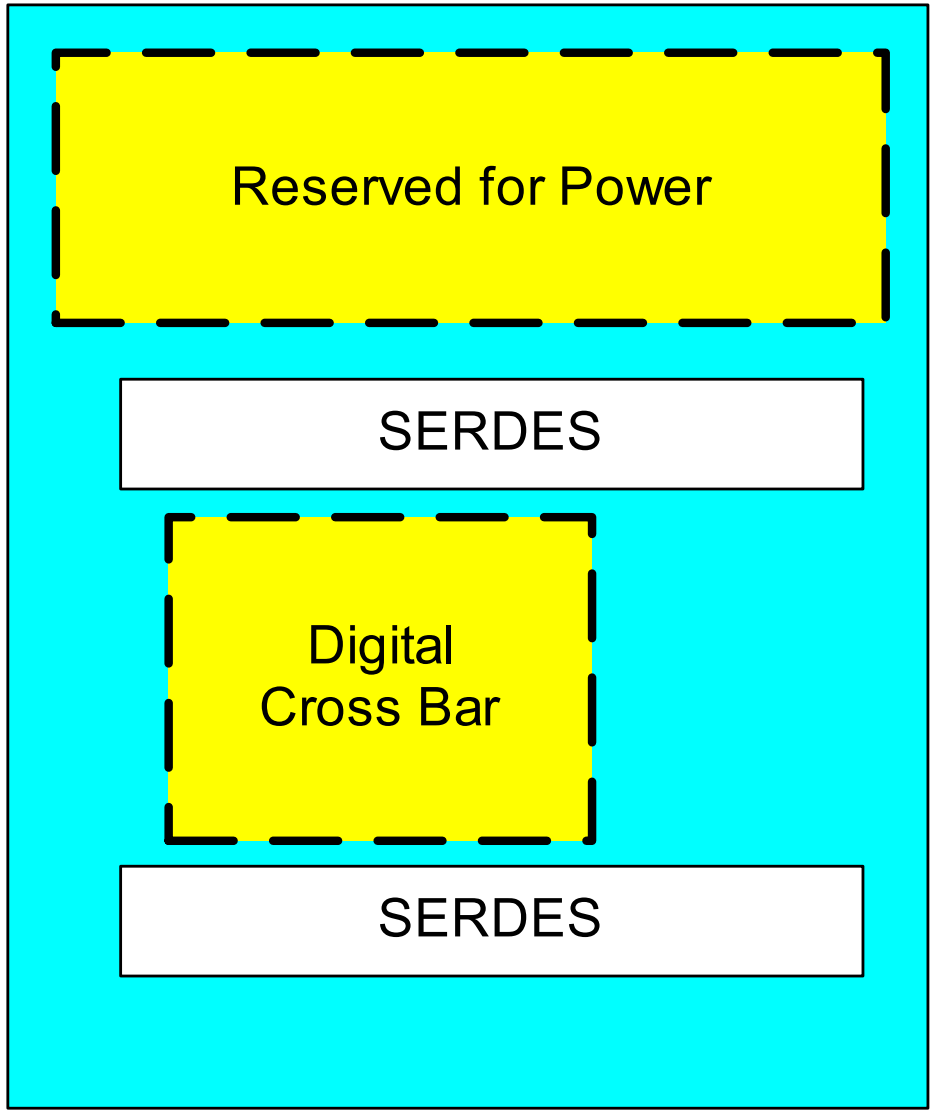
Sample Line Card Architecture 3



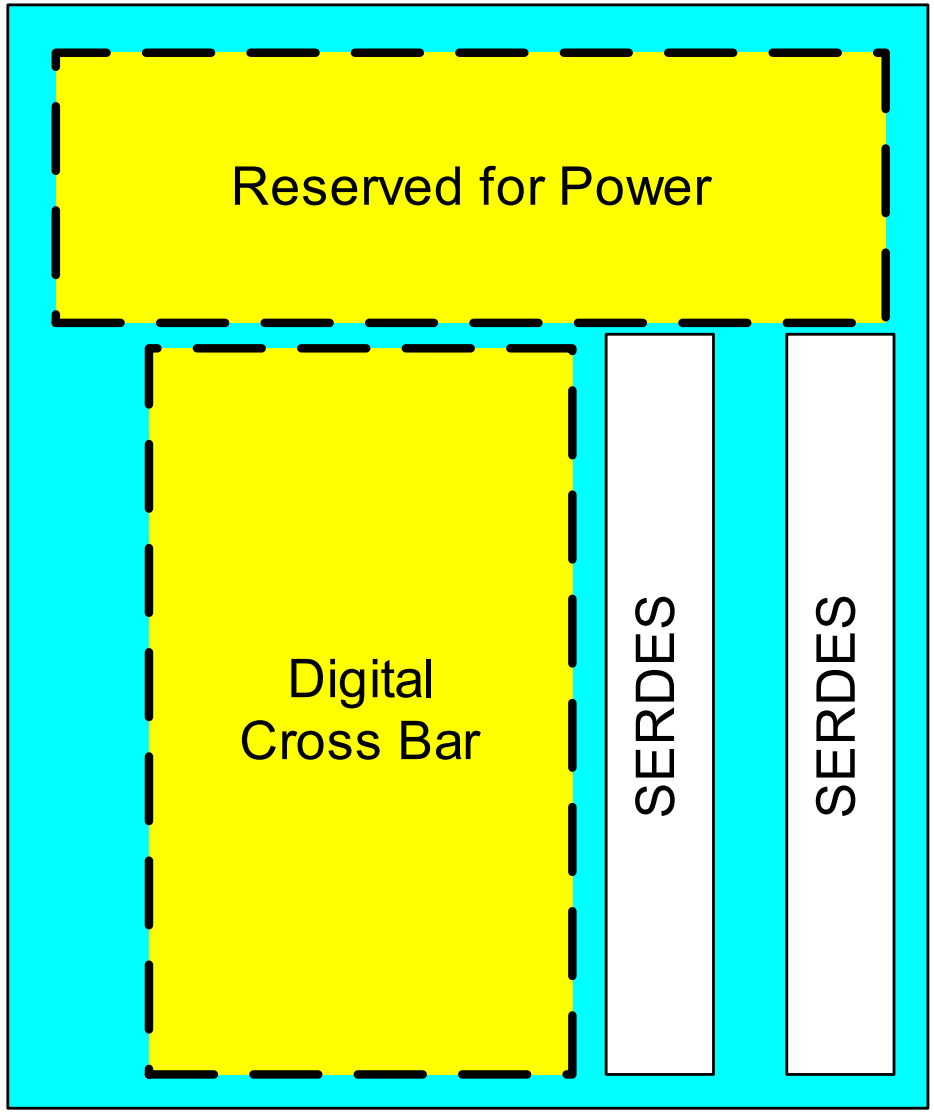
Sample Switch Fabric



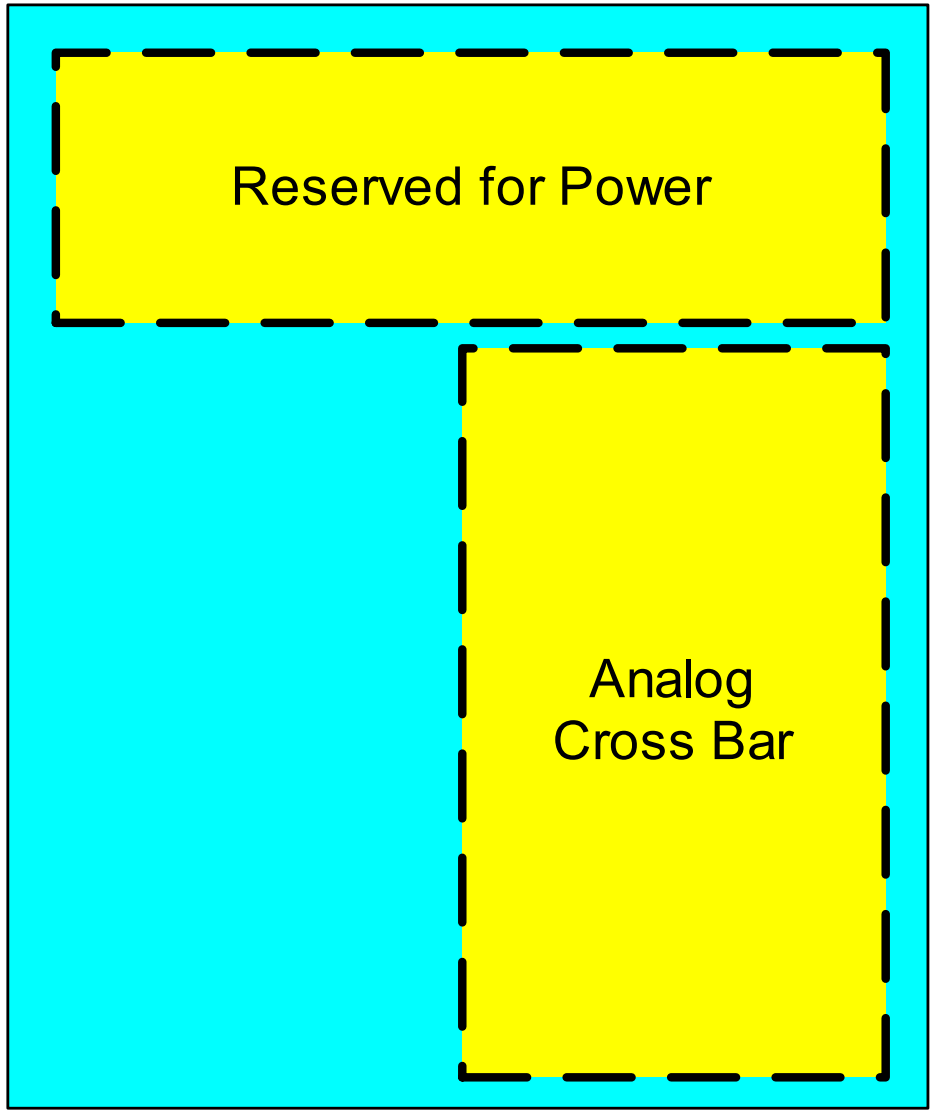
Sample Switch Fabric 1



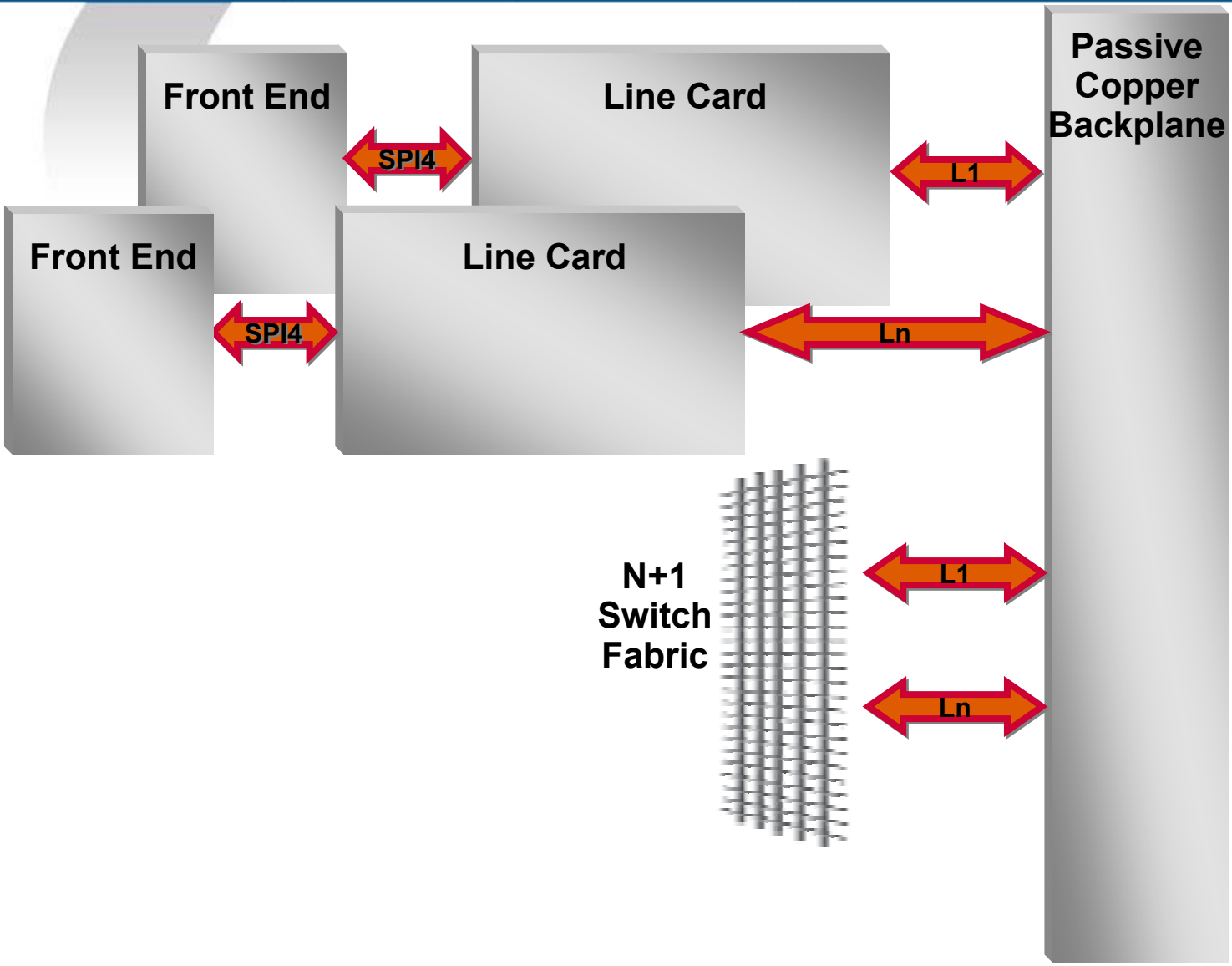
Sample Switch Fabric 2



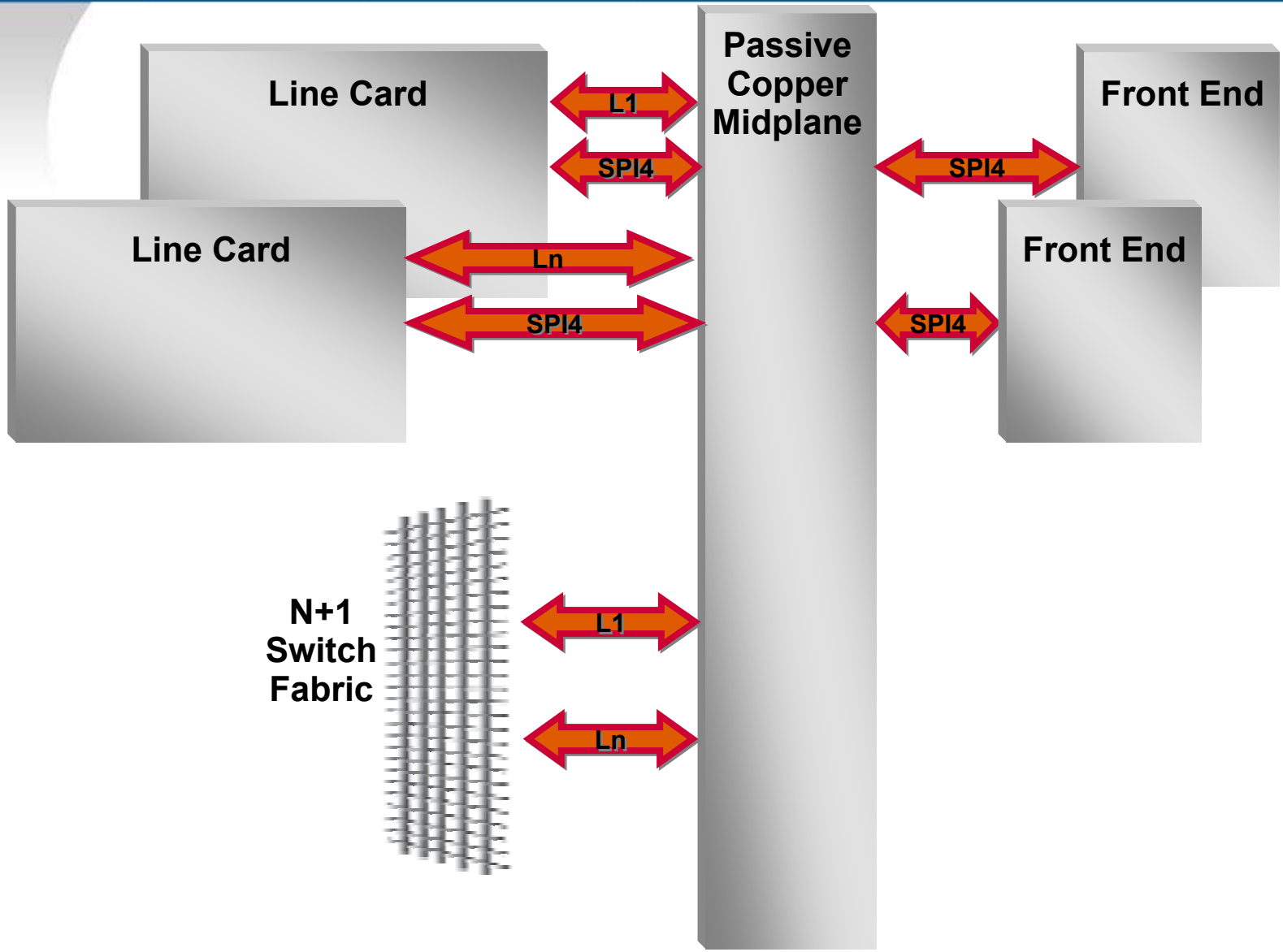
Sample Switch Fabric 3



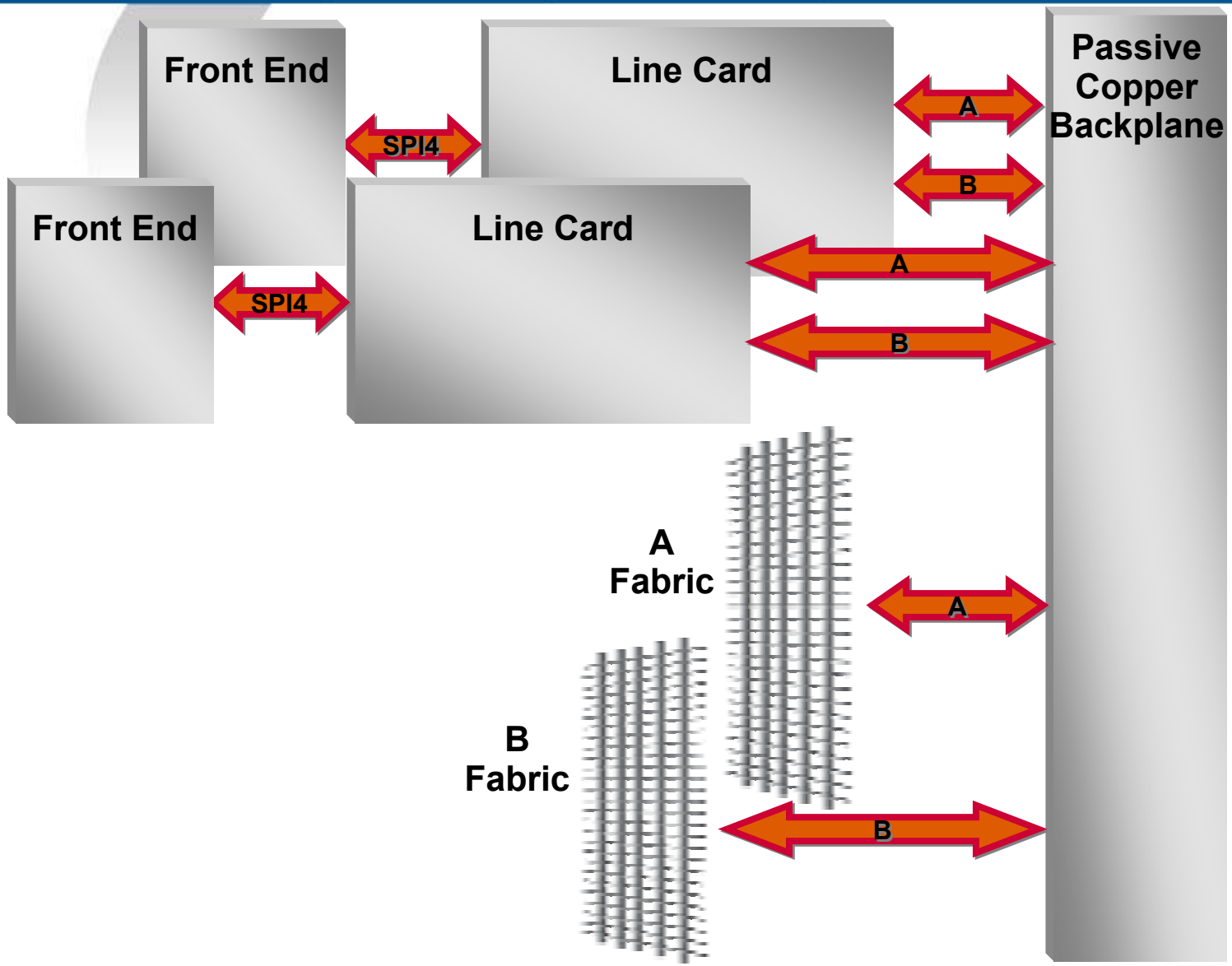
N+1 Redundant Fabric - BP



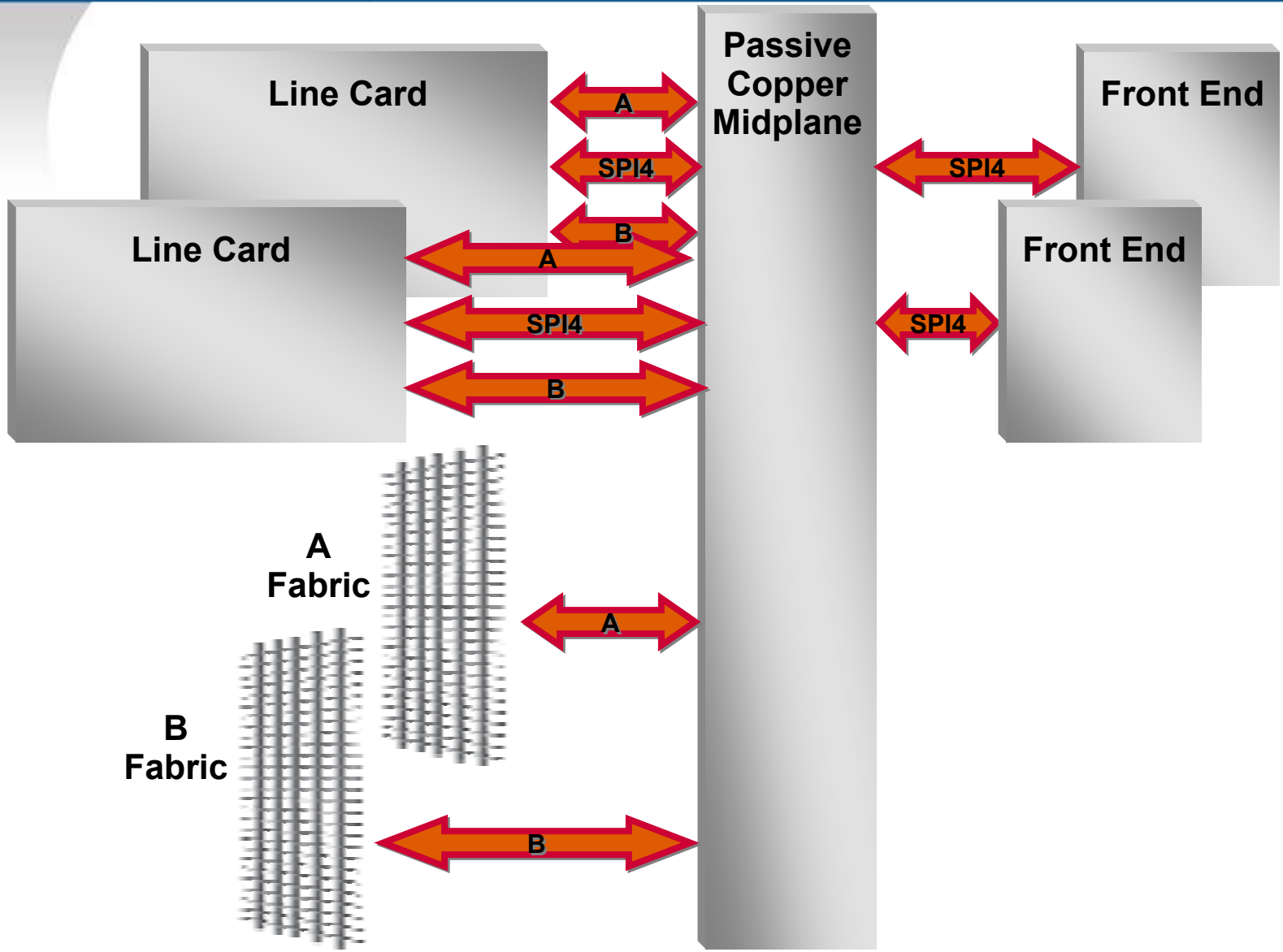
N+1 Redundant Fabric - MP



A/B Redundant Fabric - BP



A/B Redundant Fabric - MP



Trace Length Combinations - Max

24in to 34in height (2 or 3 per rack)

	N+1 Fabric			
	Position: Top or Bottom of Line Cards			
Case		LC -1	LC -2	LC -3
	Trace Length	16	6	4
SF -1	18	56	46	44
SF -2	12	50	40	38
Back Plane	22			

	A/B Fabric			
	Position: Top or Bottom of Line Cards			
Case		LC -1	LC -2	LC -3
	Trace Length	16	6	4
SF -3	14	52	42	40
Back Plane	22			

	N+1 Fabric			
	Position: Middle of Line Cards			
Case		LC -1	LC -2	LC -3
	Trace Length	16	6	4
SF -1	18	52	42	40
SF -2	12	46	36	34
Back Plane	18			

	A/B Fabric			
	Position: Middle of line cards			
Case		LC -1	LC -2	LC -3
	Trace Length	16	6	4
SF -3	14	48	38	36
Back Plane	18			

Note: All dimensions in inches

Trace Length Combinations - Min

24in to 34in height (2 or 3 per rack)

	N+1 Fabric			
	Position: Top or Bottom of Line Cards			
Case		LC -1	LC -2	LC -3
	Trace Length	16	6	4
SF -1	18	39	29	27
SF -2	12	33	23	21
Back Plane	5			

	A/B Fabric			
	Position: Top or Bottom of Line Cards			
Case		LC -1	LC -2	LC -3
	Trace Length	16	6	4
SF -3	14	35	25	23
Back Plane	5			

	N+1 Fabric			
	Position: Middle of Line Cards			
Case		LC -1	LC -2	LC -3
	Trace Length	16	6	4
SF -1	18	36	26	24
SF -2	12	30	20	18
Back Plane	2			

	A/B Fabric			
	Position: Middle of line cards			
Case		LC -1	LC -2	LC -3
	Trace Length	16	6	4
SF -3	14	32	22	20
Back Plane	2			

Note: All dimensions in inches

Trace Length Combinations - Max

10in to 14in height (5 to 8 per rack)

	N+1 Fabric			
	Position: Top or Bottom of Line Cards			
Case		LC -1	LC -2	LC -3
	Trace Length	9	5	n/a
SF -1	15	41	37	n/a
SF -2	9	35	31	n/a
Back Plane	17			

	A/B Fabric			
	Position: Top or Bottom of Line Cards			
Case		LC -1	LC -2	LC -3
	Trace Length	9	5	n/a
SF -3	n/a	n/a	n/a	n/a
Back Plane	17			

	N+1 Fabric			
	Position: Middle of Line Cards			
Case		LC -1	LC -2	LC -3
	Trace Length	9	5	n/a
SF -1	15	38	34	n/a
SF -2	9	32	28	n/a
Back Plane	14			

	A/B Fabric			
	Position: Middle of line cards			
Case		LC -1	LC -2	LC -3
	Trace Length	9	5	n/a
SF -3	n/a	n/a	n/a	n/a
Back Plane	14			

Note: All dimensions in inches

Trace Length Combinations - Min

10in to 14in height (5 to 8 per rack)

	N+1 Fabric			
	Position: Top or Bottom of Line Cards			
Case		LC -1	LC -2	LC -3
	Trace Length	9	5	n/a
SF -1	15	26	22	n/a
SF -2	9	20	16	n/a
Back Plane	2			

	A/B Fabric			
	Position: Top or Bottom of Line Cards			
Case		LC -1	LC -2	LC -3
	Trace Length	9	5	n/a
SF -3	n/a	n/a	n/a	n/a
Back Plane	2			

	N+1 Fabric			
	Position: Middle of Line Cards			
Case		LC -1	LC -2	LC -3
	Trace Length	9	5	n/a
SF -1	15	26	22	n/a
SF -2	9	20	16	n/a
Back Plane	2			

	A/B Fabric			
	Position: Middle of line cards			
Case		LC -1	LC -2	LC -3
	Trace Length	9	5	n/a
SF -3	n/a	n/a	n/a	n/a
Back Plane	2			

Note: All dimensions in inches

Basic Design Issues

- Material Selection Impacted by:
  - Temperature and Humidity effects on Df/Dk.
  - Required mounting holes for mother-card mounting, as well as shock and vibration requirements.
  - Required number of times a chip can be replaced on a mother-card.
  - Required number of times a pin can be replaced on a back plane.
  - Aspect ratio.
  - Power plane copper weight.

Channel Design Considerations

- Do we support legacy implementations?
  - We start with the XAUI/CX-4 channel characteristics.
  - We refine S21.
  - We discuss the margin required for NEXT/FEXT.
  - We discuss the addition of a margin for thru-hole reflections.
  - We select a coding scheme that works to 6.25Gps with hope of getting to 11+Gps.
  - We discuss additions of DFE, FEC, and/or Pre-emphasis, etc. We also have to examine latency.
  - We wrap up lose ends.

Channel Design Considerations

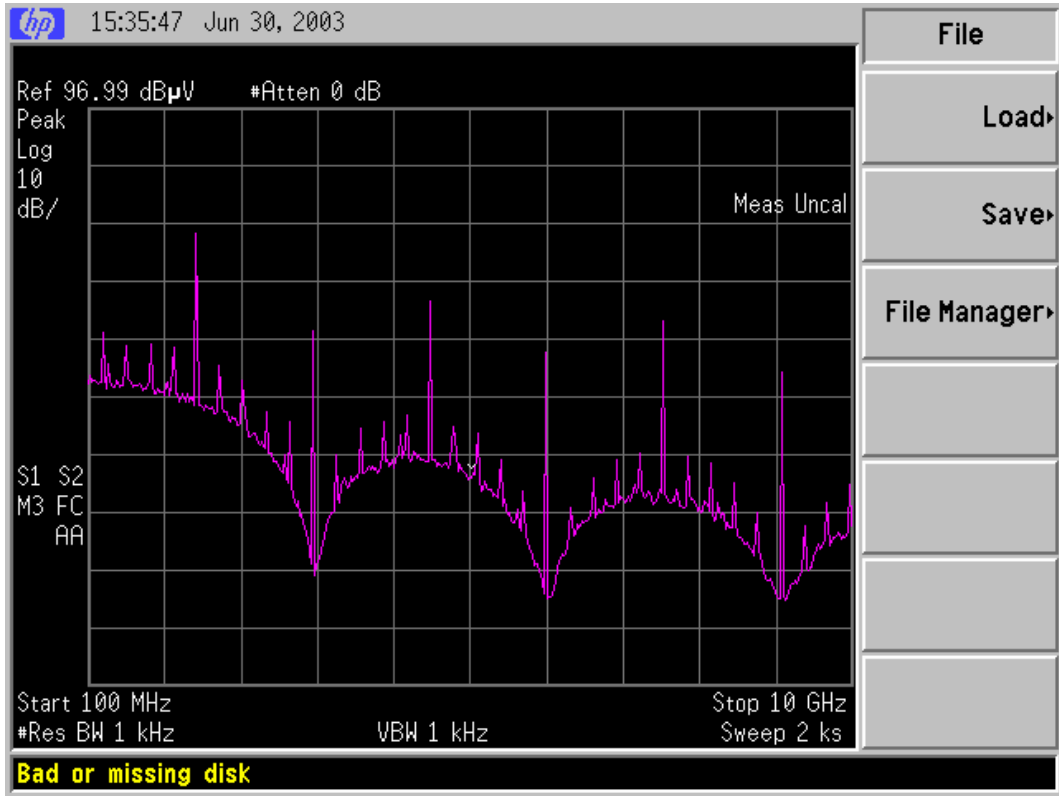
- Do we give up on legacy and define a Channel we are all happy with (ha-ha) to support 6.25/11+/25?
  - We don't just define a simple model, we define a budget.
  - We define margins for all aspects of the channel including:
    - S11
    - S21 based on material category
    - Define coding and baud rate based on material category
    - Thru-hole reflections
    - Routing reflections
    - Connector X-tlk
    - Trace X-tlk
    - DC blocking
    - Temperature and Humidity losses/expectations based on material category
  - Doing so allows the systems designer to control cost-performance-manufacturing-power risks.
  - Doing so allows the systems designer to debug each part of the channel when the SERDES TX/RX path fails.

Channel Design Considerations

- Or ……Do we give up on Legacy and ???
  - Define some type of model based on the Statistical Eye Method used in OIF's CEI implementation agreement … or other alternative.

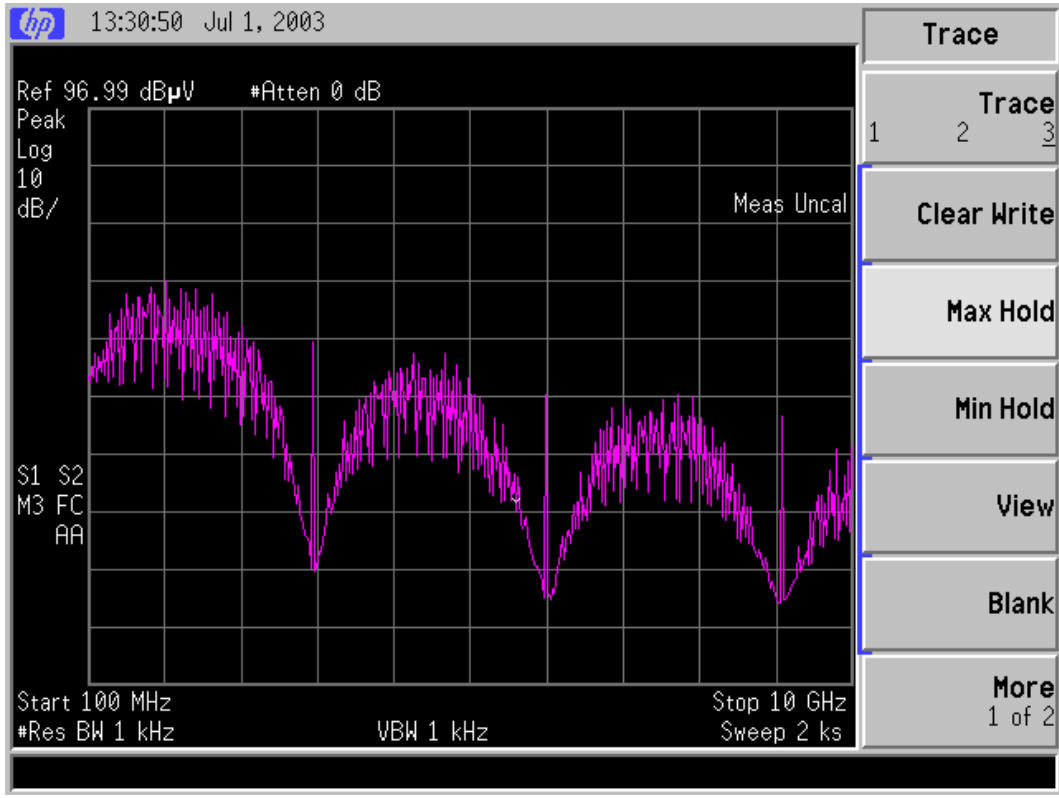
Channel Design Considerations

- Let's try not to use a coding method that has this much spectral peaking (such as 2^7).



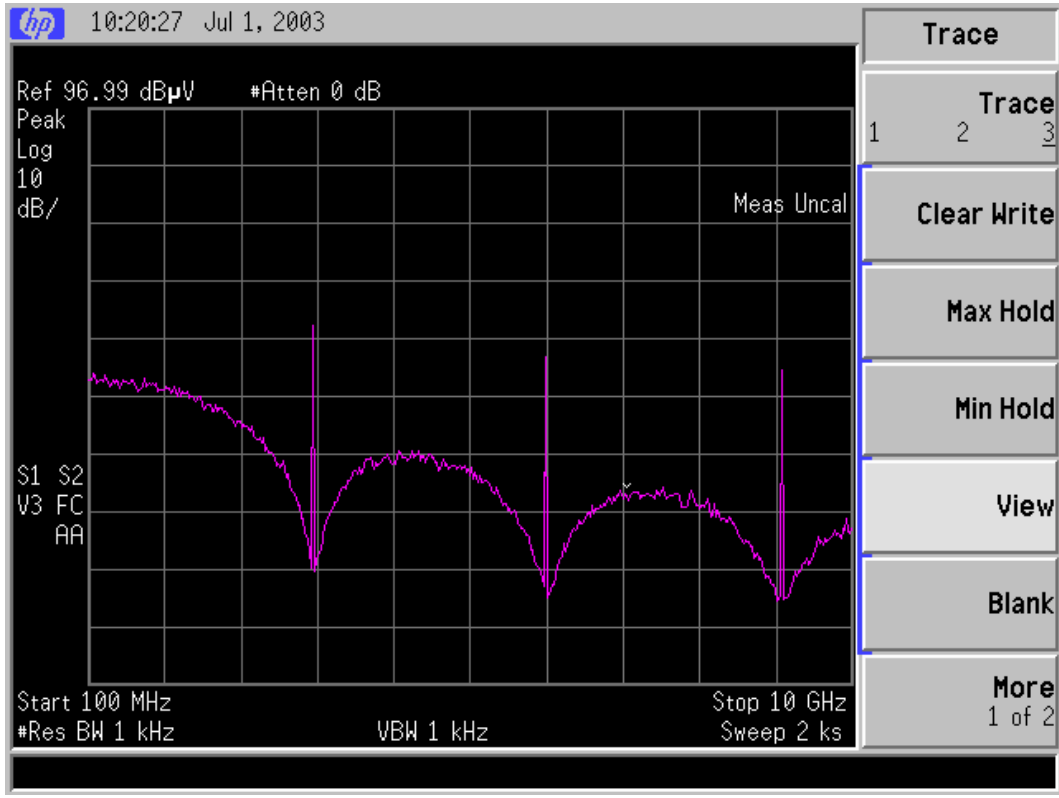
Channel Design Considerations

- Let's try not to use a coding method that has this much spectral peaking (64B66B).

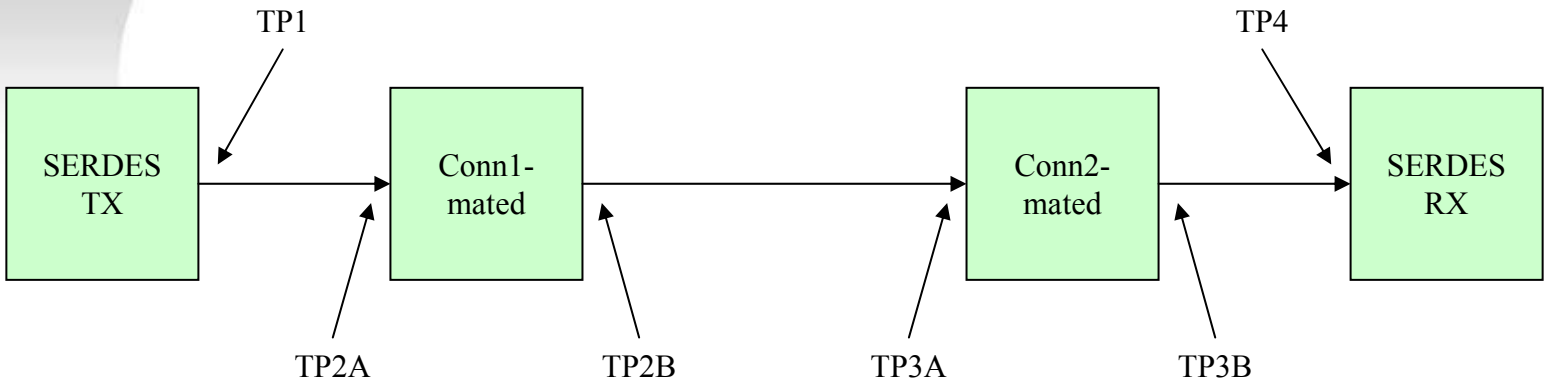


Channel Design Considerations

- Let's pick a coding method that has similar spectral peaking to 8B10B.



Channel Model Description



- I prefer a Channel breakout as defined above, rather then defined below. The above isolates channel components for individual measurement and conformance.

Acceptable Channel BER in a System

- Data transmitted across the back plane channel is usually done in a frame with header and payload.
- The frame size can be anywhere from a few hundred bytes to 16Kbytes, typical.
  - Customers are asking for 64Kbytes by 2007.
- The larger frame size is to support jumbo frames currently in use across the PHY.
  - A typical frame contains many PHY-layer packets.
- BER of 10E-12 will result in a frame error of 10E-7 or less, depending on distribution.
  - That is a lot of frame loss.

Acceptable Channel BER in a System

- Customers want to see a frame loss of zero.
- Systems architects want to see a frame loss of zero.
- Zero error is difficult to test and verify … none of us will live that long.
- The BER goal should be 10E-15.
  - It can be tested and verified at the system design level.
  - Simulate to 10E-17.
  - Any frame loss beyond that will have minimal effect on current packet handling/processing algorithms.

Summary

- The channel model needs to be effective for cost, power, and performance. This single model should support two ranges of lengths: 1) 18in to 40in, and 2) 16in to 32in.
- The channel model should be defined as a table of margins if possible. It will allow system and chip vendors more design control.
- The channel breakout should be defined to allow access to each major channel component.
- BER 10E-15. Ask your architects and customers before you settle for 10E-12.
- The code and channel need to support large frame sizes.
- It will be beneficial to all if we decide on a connector (SMA, etc) type for interface to our test equipment/boards as an informative Annex. It will make channel evaluation easier and more uniform.